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Power Converters and Control Systems for DC Smart Grids and Smart Transformers Applications

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ELECTRICAL MACHINES AND DRIVES

**Final Dissertation**

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# Power Converters and Control Systems for DC Smart Grids and Smart Transformers Applications

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by

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## **Preface**

This Ph.D. study has been carried out at the Department of Electrical and Information Engineering of the Polytechnic of Bari from November 2014 to October 2017. The theoretical development, the implementation and testing activity has been performed in the Power Electronic Laboratory of the Polytechnic of Bari. Part of the study and testing activity has been carried out during the visiting period in Kiel at the Chair of Power Electronics at the Institute of Electrical Engineering and Information Technology (EE&IT) CAU Kiel from October 2016 to June 2017.

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# Introduction

In the last years a growing interest towards DC Smart Grids has been registered due to high penetration of distributed generation systems with embedded storage. Trying to foresee the possible future scenarios of the power systems, it can be noticed that DC Smart Grids can be even preferable to AC Smart Grids in terms of flexibility and redundancy since they are compatible with the achievement of a DC Multibus working at different voltage levels.

The actual power system is AC-based. The reasons of this choice are several, among them there are the flexible connection to transformers and induction motors and the need to transfer high power for long distances. DC transmission is adopted just for a limited number of applications such as electric traction and submarine transmission. As a consequence, also in the field of Distributed Power Generation Systems (DPGS), AC Smart Grids have experienced a wider spread than DC ones. However also DC Smart Grids contain a great potential to be exploited and their study can be considered the preliminary step towards the development of a future DC power system.

At high power levels the advantages of the High Voltage Direct Current (HVDC) transmission are well known in case of submarine or overhead lines used to cover long distances since DC lines are more competitive, from an economical point of view, than AC lines as line length increases.

In low power system, different advantages are verified in case of Smart Grids applications: the first one relies on the nature of some renewable sources which are intrinsically DC sources. As a consequence, a DC/AC power conversion stage is required in order to connect the system to the main grid or to feed the loads. Differently, many domestic loads require DC supply; hence the double power conversion stage implies additional losses (around 10-40%). Starting from these considerations, DC Smart Grids can provide higher efficiency reducing the number of power conversion stages [1]-[4].

A second important issue is flexibility due to coupling various DC renewable sources which operate at different voltage levels. Connection to the main AC grid can be guaranteed by means of a bidirectional AC/DC converter with bidirectional power flow capability or to a DC electrical distribution network, as shown in Fig. 1. The bidirectional AC/DC multilevel converter is connected to the Point of Common Coupling (PCC) with the AC grid, by an  $L_g$  filter. It feeds on the DC side, some bidirectional DC/DC converters in order to provide different voltage levels. The third important issue is the continuous operation in case of faults on the AC side due to embedded storage systems; the last advantage is the absence of synchronization since phase control is not required.

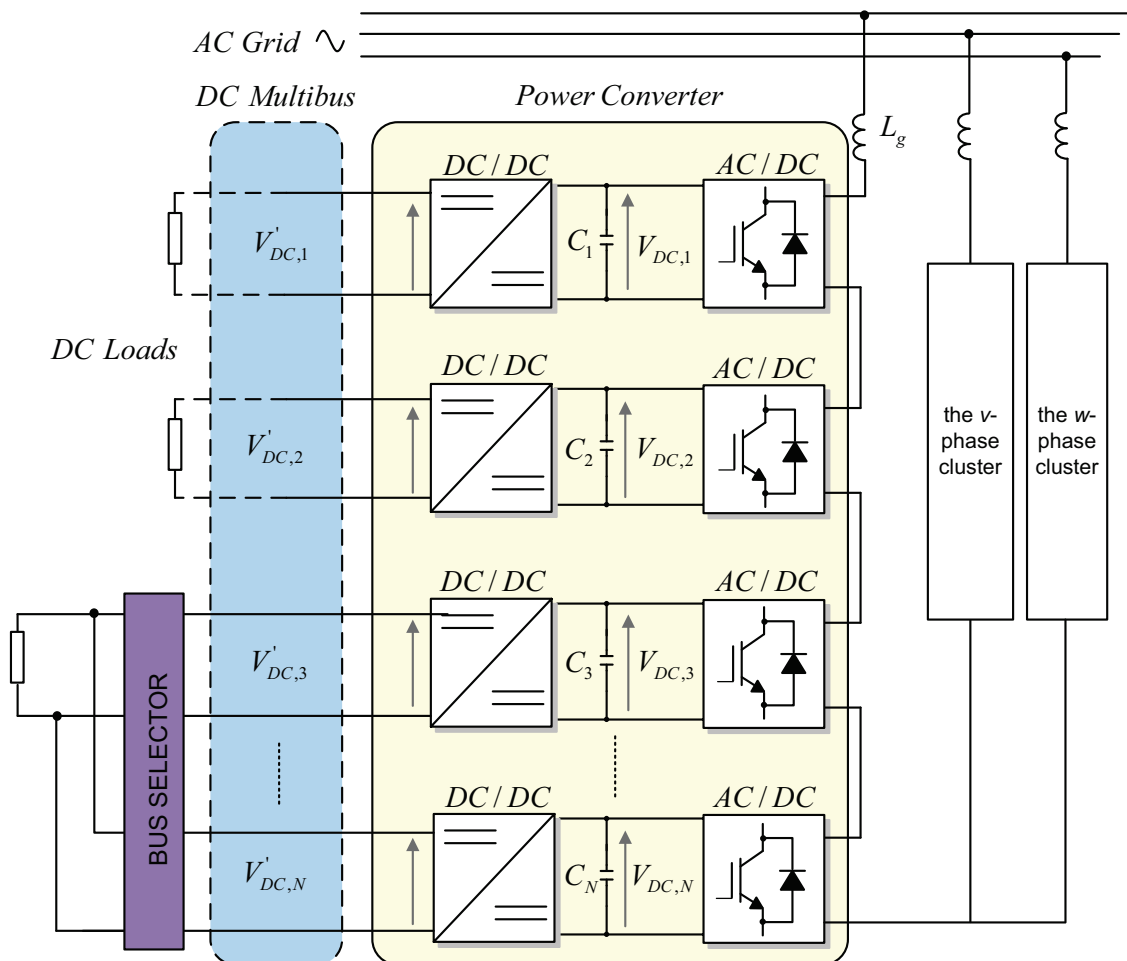


Fig.1: Multi-DC-bus solutions for DC Smart Grids.

The advantages of DC Smart Grids are summarized as follows [5]:

1. High system efficiency due to single-stage power conversion;
2. Synchronization with the main grid is not needed (frequency and/or phase control are unnecessary);
3. Continuous operation mode in case of AC faults due to the storage energy systems included in the DC Smart Grid;
4. Better integration of energy storage and renewable and alternative power sources because almost all of them are inherently DC (modern electronic loads, such as computers and servers in data centers, require DC power).

On the other hand the drawbacks of DC Smart Grids are [5]:

1. Need to create new DC distribution lines;
2. Protections circuit complexity since their action cannot be based on zero-crossing detection;

Since DC Smart Grids require different voltage levels due to integration of different renewable sources, loads, and energy storage devices, the multi-DC-bus system can provide a viable solution. The DC Multibus concept derives from naval applications [1], [4] and it can be successfully applied to the DC Smart Grids characterized by the coexistence of different voltage levels, different storage systems and different load supplies. The DC Multibus can contribute to the system redundancy since a single load can be supplied by a single DC bus, by more buses simultaneously or sequentially. Besides DC Smart Grids are particularly suitable when loads are sensitive electronic equipment. However, DC Smart Grids are not exempt from issues stability. Stability issues depend on requirement of power electronic converters achieving different voltage levels. Reliable operation of the system is also crucial, it is important to have a well-functioning protection system [5].

A DC Multibus can be achieved by means of a Modular Multilevel Cascade Converter (MMCC) (which can operate both with equal and different voltages at the DC-links of the power conversion modules). MMCCs have been recently classified by Hakagi in

[6], and among them, the Single-Star Bridge Cells (SSBC) MMCC is particularly proper for battery energy storage systems based on one-converter-to-one-battery modules [7]-[8].)

In this thesis a SSBC MMCC combined with isolated bidirectional DC/DC Dual Active Bridges (DABs) is applied to a DC Smart Grid with the aim to create a flexible DC Multibus. DABs converters provide galvanic isolation to the system extending the operating voltage range. The possibility to operate at different voltage levels can provide flexibility and redundancy to the DC Smart Grid.

The same power stage is applied also to a new More Electrical Aircraft (MEA), whose power distribution system is in DC. Indeed a MEA can be considered as an example of DC Smart Grid [9]. Besides the same topologies can be applied for the development of a new Smart Transformer (ST), which in the future could replace the traditional power distribution transformer, providing additional control functionalities [10]-[11].

The thesis has been structured as follows:

The *First* and the *Second Chapter* are devoted respectively to the modeling and control design of the SSBC MMCC and the DABs for Smart Grids applications. The performances of the overall system have been verified in numerous operation conditions confirming the validity of the proposed solution also in case of a wide range of loads variations.

The *Third Chapter* treats of the same power converters in a MEA system. The performances are analyzed considering the strict power quality requirements of MEA and in case of variable frequency operation. In the same chapter a feasibility study of a 270V/28V Silicon Carbide (SiC) MOSFET Dual Active Bridge (DAB) converter for MEA is also presented.

Finally, in *Fourth Chapter*, a possible three stages ST is developed based on a SSBC MMCC converter in the Medium Voltage (MV) side and several DABs converters in the isolation stage. On the basis the thermal monitoring information of the power conversion cells, a power routing techniques can be used in order to increase the

reliability of the ST. In this scenario a new voltage balancing control is proposed and located in the isolation stage instead of the MV side.

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# Chapter I

## SSBC MMCC for DC Smart Grids: Modeling and Control

With the advancement of power electronics and maturity of the modular and multilevel converter technologies, it is now possible to cover power and voltage ranges beyond the limits related to the semiconductor devices. The multilevel converters achieve high-voltage switching by means of a series of voltage steps within the ratings of the individual power devices [1]. Among the multilevel converters, the SSBC MMCC is particularly attractive in high-voltage applications since, due to its modular structure, the hardware implementation is rather simple and the maintenance operation is easier than alternative multilevel converters. Different applications for the MMCC converters have been proposed in the literature [2]-[4]. In [2], a MMCC has been investigated as a static VAR compensator. It has also been utilized as an active front-end rectifier in electric trains [3]-[4] and in application to the Solid State Transformer (SST) in the distribution system [5]-[8]. This method allows the elimination of the heavy and bulky line transformer, thus reducing encumbrance and cost.

The proposed power conversion stage for DC Smart Grids application is based on a SSBC MMCC creating a DC Multibus as shown in Fig. 1. The MMCCs family is one of the most famous multilevel topologies, particularly used for Medium Voltage (MV) applications. The performances of a MMCC depends on the number of voltage levels denoted as  $L$ .  $L$  is defined on the basis of the power conversion cells number  $N$  used for each phase:

$$L = 2N + 1 \tag{1.1}$$

The main advantages obtained increasing the number of cells (and consequently the number of levels) are:

1. Reduction of the  $dV/dt$ , that occurs during each switch transition, produces a reduction of electromagnetic interference (EMI);
2. Reduction of the output filter, because the grid current PWM harmonic components are shifted towards the high frequency range;
3. Increase of the output voltage state redundancies, resulting in more flexibility in modulation techniques and less switching losses.

In practice, the number of power cells in a SSBC MMCC is mainly determined by its operating voltage and manufacturing cost. The use of identical power cells leads to a modular structure which is an effective means for cost reduction. The main advantages of the modular approach include:

- improvement in reliability by introducing desired level of redundancy;
- standardization of components leading to reduction in manufacturing cost and time;
- power system can be easily reconfigured to support varying input-output specifications and fault conditions.

The most important features of the SSBC MMCC can be summarized in: modularity, possibility of fault-tolerance implementation, multilevel operation, reduced  $dV/dt$  and filter size.

The drawbacks deriving from the increasing of the number of levels are the increase of the number of the semiconductor components, and consequently the difficulty in the control of a complex structure.

## 1.1 SSBC MMCC Switching Function

Each phase of a SSBC MMCC consists in  $N$  units of single phase H-Bridges power cells, normally connected in series on their AC side, to achieve medium-voltage operation and low harmonic distortion, as shown in Fig. 1.1. The operation of a SSBC MMCC can be easily understood deriving the switching function. With reference to the H-Bridge in Fig. 1.1, the top and bottom switch in each leg must be switched ON and OFF complementary. The three possible output-voltage levels of each H-bridge

converter and their corresponding switch combinations are illustrated in Tab. 1.1, where “0” represents that the switch is ON and “1” represents that the switch is OFF.

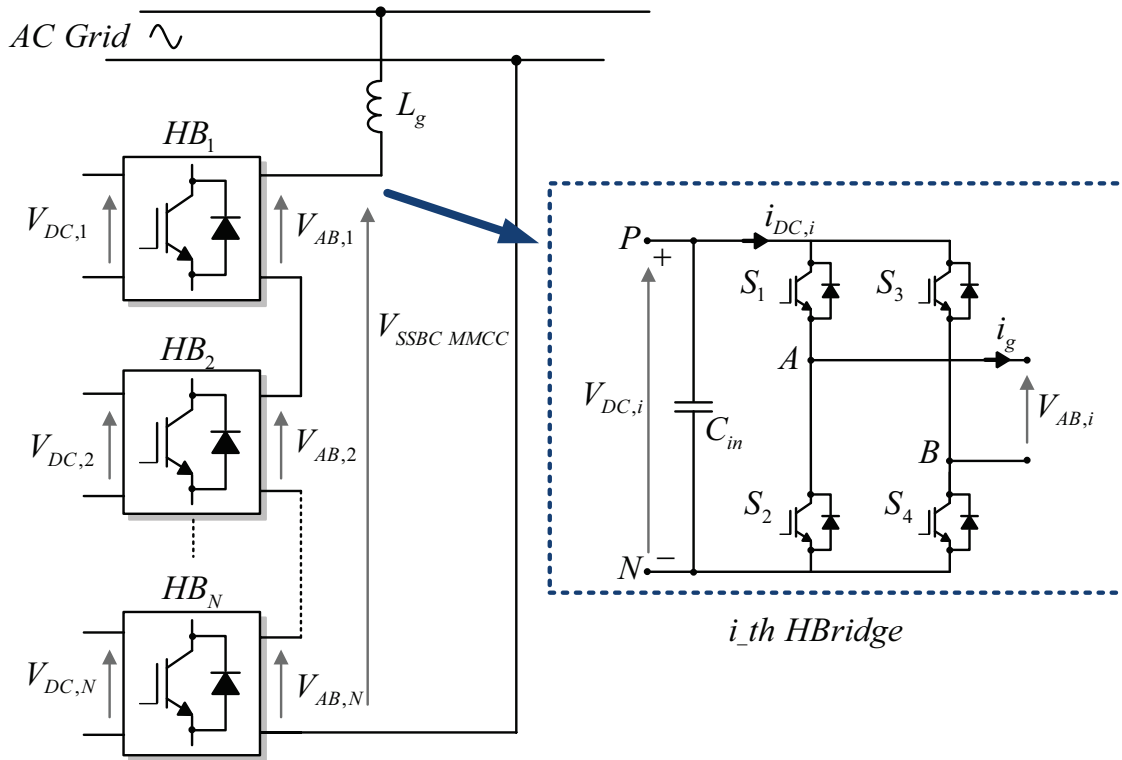


Fig. 1.1: 2N+1 levels SSBC MMCC.

Tab. 1.1: H-Bridge cell switching table.

$S_1$	$S_2$	$S_3$	$S_4$	$V_{AB}$	$i_{DC}$
1	0	0	1	$V_{DC}$	$i_g$
1	0	1	0	0	0
0	1	0	1	0	0
0	1	1	0	$-V_{DC}$	$-i_g$

Therefore, the top switch variables  $S_1$  and  $S_3$  can be used to represent the switching status of phase leg A and B respectively. The instantaneous model of each leg can be defined as follow:

$$V_{AN} = S_1 \cdot V_{DC} \quad (1.2)$$

$$V_{BN} = S_3 \cdot V_{DC} \quad (1.3)$$

where  $V_{DC}$  is the DC-bus voltage. The relationship between the input voltage,  $V_{DC}$ , and the output voltage,  $V_{AB}$ , is derived from equations (1.2) and (1.3) as follow:

$$V_{AB} = V_{AN} - V_{BN} = (S_1 - S_3)V_{DC} \quad (1.4)$$

Similarly the relationship between the input DC current  $i_{DC}$ , and output current  $i_g$ , is derived:

$$i_{DC} = (S_1 - S_3)i_g \quad (1.5)$$

Denoting:

$$H = (S_1 - S_3) \quad H \in \{-1, 0, 1\} \quad (1.6)$$

thus:

$$V_{AB} = H \cdot V_{DC}; \quad i_{DC} = H \cdot i_g; \quad H \in \{-1, 0, 1\} \quad (1.7)$$

The instantaneous model of the H-bridge converter is derived in (1.7), as a function of the switching variable  $H$ , which describes the output voltage state of the H-Bridge. In the same way, the switching model of sole phase of the a  $2N+1$  levels SSBC MMCC can be totally described by the following equations:

$$V_{AB,i} = H_i V_{DC,i} \quad \text{with} \quad H_i \in \{-1, 0, 1\} \quad i = 1, 2, \dots, N \quad (1.8)$$

$$i_{DC,i} = H_i i_g \quad \text{with} \quad H_i \in \{-1, 0, 1\} \quad i = 1, 2, \dots, N \quad (1.9)$$

where  $N$  is the number of in series H-Bridges. The relationship between each DC-Link and the SSBC MMCC total output voltage,  $V_{SSBC\_MMCC}$ , can be derived from (1.8) as follow:

$$V_{SSBC\_MMCC} = \sum_{i=1}^N V_{AB,i} = \sum_{i=1}^N H_i V_{DC,i} \quad \text{with} \quad H_i \in \{-1, 0, 1\} \quad (1.10)$$

The instantaneous model of the SSBC MMCC has been derived in (1.10), as function of the variable  $H_i$ , which represents the output switching function of the  $i$ -th H-Bridge. Assuming an equal voltage distribution in each DC-Link and considering the case of  $N=2$ , the 5-levels SSBC MMCC switching table is derived (Tab. 1.2.).

Tab. 1.2: 5-levels SSBC MMCC switching table.

$H_1$	$H_2$	$V_{SSBC}$ $MMCC$	$H_1$	$H_2$	$V_{SSBC}$ $MMCC$	$H_1$	$H_2$	$V_{SSBC}$ $MMCC$	
1	1	$2V_{DC}$	0	1	$V_{DC}$	-1	1	0	
	0	$V_{DC}$		0	0		0	-1	$-V_{DC}$
	-1	0		-1	$-V_{DC}$		-1	$-2V_{DC}$	

From Tab. 1.2 it can be noticed that the voltage levels  $\pm V_{DC}$  have been obtained with two different redundant switching states, while the state 0 with three redundant states. Redundancy due to switching stages is a common phenomenon in multilevel converter and it provides a high degree of flexibility for designing the switching model.

## 1.2 SSBC MMCC Average Model

For a complex power conversion topology, such as the SSBC MMCC, the development of an average model is indispensable for the control system design.

The average voltage of the SSBC MMCC in a switching period  $T$  is denoted as  $V_{SSBC\_MMCC,avg}$ :

$$V_{SSBC\_MMCC,avg} = \frac{1}{T} \int_t^{t+T} \sum_{i=1}^N H_i(\tau) V_{DC,i}(\tau) d\tau \quad (1.11)$$

Assuming  $V_{DC,i}$  constant in a switching period and substituting the expression of  $H_i$ :

$$V_{SSBC\_MMCC,avg} = \sum_{i=1}^N \left( V_{DC,i} \frac{1}{T} \int_t^{t+T} S_{A,i}(\tau) - S_{B,i}(\tau) d\tau \right) \quad (1.12)$$

$$v_{SSBC\ MMCC,avg} = \sum_{i=1}^N V_{DC,i} (\rho_{A,i} - \rho_{B,i}) \quad (1.13)$$

where  $\rho_{A,i}$  is the duty cycle of leg A in the  $i$ -th H-Bridge, while  $\rho_{B,i}$  for the leg B. The duty cycle is defined as the turn ON duration of the switch in a switching period  $T$ .

The relation between the duty cycle and the modulation index in a single phase H-Bridge is:

$$m_i = (\rho_{A,i} - \rho_{B,i}) \quad (1.14)$$

Substituting (1.14) in (1.13):

$$v_{SSBC\ MMCC,avg} = \sum_{i=1}^N m_i V_{DC,i} \quad (1.15)$$

The previous equation represents the model of the output SSBC MMCC voltage averaged in a switching period  $T$ , as function of the modulation index and function of the DC-link voltage of each single H-Bridge cell.

Similarly as previously, equation (1.9) results in the following averaged model:

$$i_{DC,i,avg} = m_i i_g \quad \text{with} \quad i = 1, 2, \dots, N \quad (1.16)$$

The previous equation represents the current of the  $i$ -th DC-link averaged in a switching period  $T$ , as function of the modulation index and the AC grid current,  $i_g$ .

To simplify the average model, the following assumptions are made: all the DC voltages and the modulation indexes are equal. These assumptions result in:

$$V_{DC} = V_{DC,i} \quad m = m_i \quad i = 1, 2, \dots, N \quad (1.17)$$

Substituting (1.17) in (1.15) and in (1.16), it results in:

$$v_{SSBC\ MMCC,avg} = N(mV_{DC}) \quad (1.18)$$

$$i_{DC,avg} = m i_g \quad (1.19)$$

In the time-domain, considering the fundamental-frequency component of  $v_{SSBC\_MMCC}$ , the equation (1.18) is rewritten considering the following expression for the modulating signal:

$$m = M \sin(\omega t) \quad \text{with} \quad 0 \leq M \leq 1 \quad (1.20)$$

where  $\omega$  is the fundamental frequency,  $M$  is the amplitude of the sinusoidal modulating signal. Substituting (1.20) in (1.18),  $v_{SSBC\_MMCC,avg}$  is the following:

$$v_{SSBC\_MMCC,avg} = N(MV_{DC} \sin(\omega t)) \quad (1.21)$$

while the grid current can be written as:

$$i_g = I_g \sin(\omega t - \mathcal{G}) \quad (1.22)$$

where  $\mathcal{G}$  is the shifting angle between the grid current and the SSBC MMCC output voltage and  $I_g$  is the grid current amplitude. Substituting (1.20) and (1.22) in (1.19), the expression of the average DC current is derived:

$$i_{DC,avg} = M \sin(\omega t) I_g \sin(\omega t - \mathcal{G}) \quad (1.23)$$

which results in the sum of two terms:

$$i_{DC,avg} = \frac{MI_g}{2} \cos \mathcal{G} - \frac{MI_g}{2} I_g \cos(2\omega t - \mathcal{G}) \quad (1.24)$$

Eq. (1.21) and (1.24) show that the AC voltage,  $v_{SSBC\_MMCC,avg}$ , and the DC current,  $i_{DC,avg}$ , depend both on the value of modulating signal.

The DC current consists of its average value and a sinusoidal component with double line frequency, which is typical of single-phase systems.

The AC voltage fundamental component is equal to reference modulation signal multiplied by the DC-link voltage. Depending on the value of  $\mathcal{G}$ , it is possible to define the operation as inverter ( $\cos \mathcal{G} \approx 1$ ) or rectifier ( $\cos \mathcal{G} \approx -1$ ), when a unit power factor condition is required. The average model of the SSBC MMCC is represented in Fig. 1.2. All the quantities shown in Fig. 1.2 are defined in the following:

$$e = E \sin(\omega t) \quad (1.25)$$

$$v_{SSBC\ MMCC} = \sum_{i=1}^N v_{AB,i} = M \sum_{i=1}^N V_{DC,i} \sin(\omega t + \psi) \quad (1.26)$$

$$i_g = I_g \sin(\omega t - (\vartheta - \psi)) \quad (1.27)$$

$$i_{DC,i} = \frac{MI_g}{2} \cos(\vartheta - \psi) \quad (1.28)$$

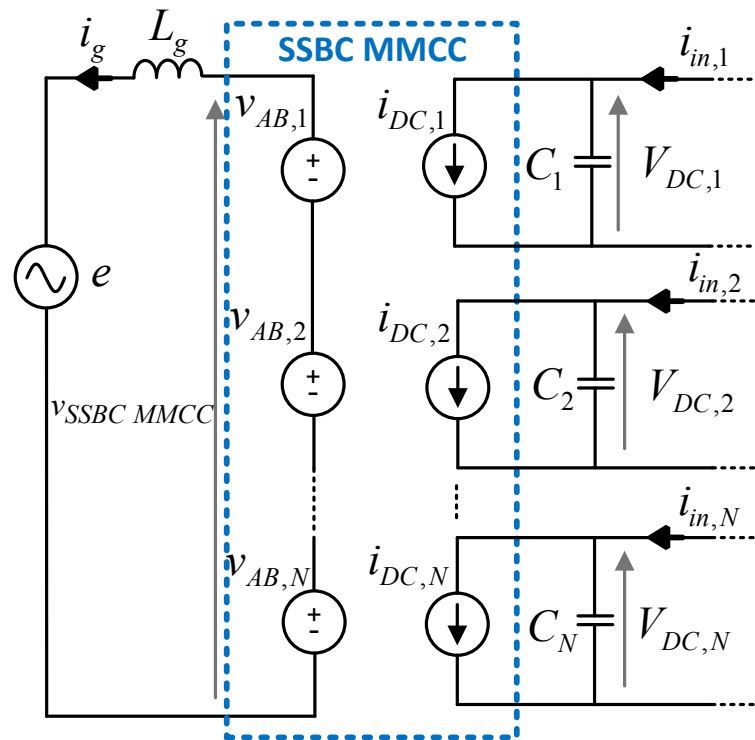


Fig. 1.2: Average model of a sole phase of the  $2N+1$  levels SSBC MMCC.

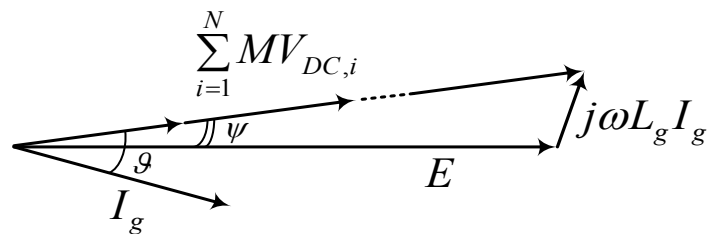


Fig. 1.3: Phasor - Diagram of a phase of the SSBC MMCC.

Looking at Fig. 1.2 and Fig. 1.3, the average model is described by the following equations in both the AC and DC side:

$$L_g \frac{di_g}{dt} = v_{SSBC\ MMCC} - e \quad (1.29)$$

$$C_i \frac{dV_{DC,i}}{dt} = i_{in,i} - \frac{MI_g}{2} \cos(\vartheta - \psi) \quad \text{with } i=1,2,\dots,N \quad (1.30)$$

### 1.3 SSBC MMCC Overall Control Structure

The control system may guarantee synchronization with the main grid and full control of the DC voltage. In this thesis each power conversion cell is controlled as shown in Fig. 1.4 where the voltage  $v_{SSBC\ MMCC}^*$  denotes the output of the cascaded multi loop control system; it is provided as voltage reference to the PWM modulator establishing the switching function  $h_1, h_2, \dots, h_N$  of each cell.

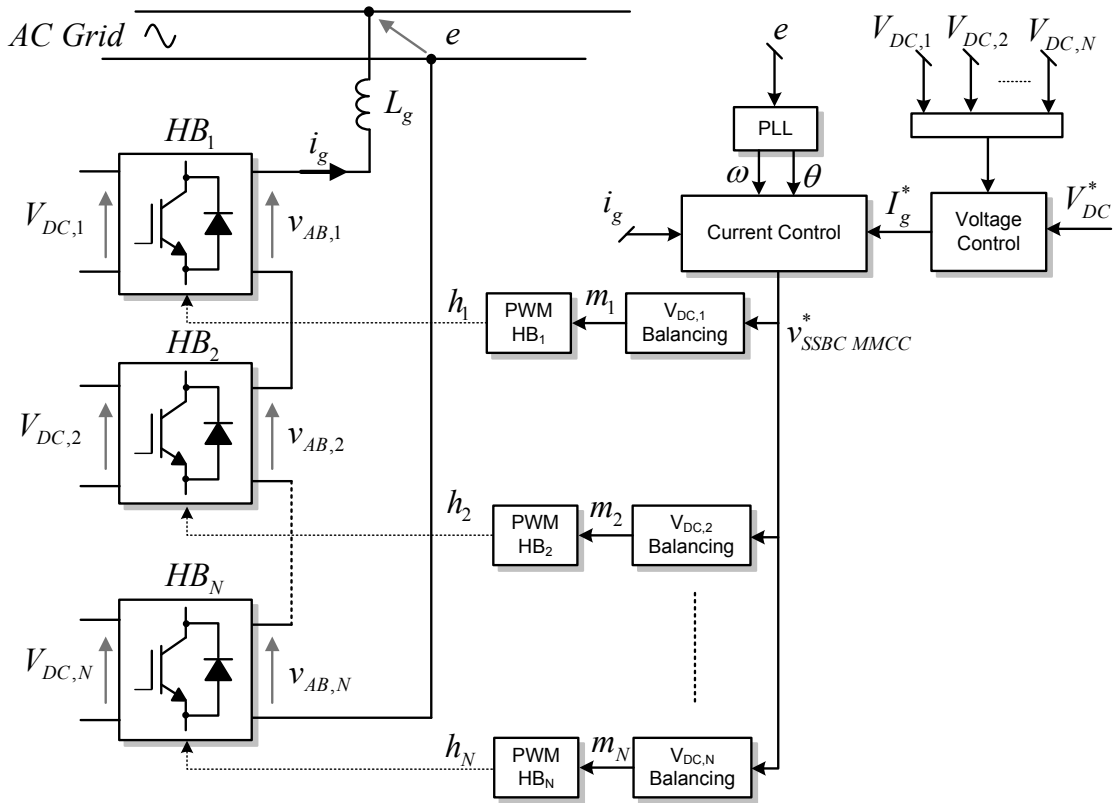


Fig. 1.4: Control scheme of SSBC MMCC.

The outer loop controls directly the overall DC voltage and indirectly the power exchanged with the main AC grid since it generates the current reference for the inner loop. The voltage loop operates as in the following: the DC voltages, available at each

DC-link, are summed and the average value is calculated; then the average value is firstly filtered in order to cut-off the second order harmonic, typical of the single-phase H-Bridge, and later this value is compared with the voltage reference  $V_{DC}^*$ . The voltage control is based on a PI regulator. A Phase-Locked-Loop (PLL) circuit provides a single-phase sinusoidal waveform perfectly synchronized with the main grid voltage.

The sinusoidal current reference is obtained multiplying the unitary sinusoidal signal by  $I_g^*$  (provided in output by the voltage control). The current loop is based on a P+Resonant controller [9]. The output  $v_{SBCC\_MMCC}^*$  is the average voltage which may be generated by the overall power stage in order to annul the current error. The voltage reference  $v_{SBCC\_MMCC}^*$  is shared among the different units.

A corrective action is introduced by means of an offset calculated in order to take into account the difference between the real voltage of each cell  $V_{DC,i}$  and the reference value. This unbalanced condition is the result of differences in the power delivered by each cell.  $m_1, m_2, \dots, m_N$ , denote the output PWM modulating signal of each cell.

## 1.4 SSBC MMCC Current Control Loop

In order to guarantee a good decoupling, the inner current loop has to be designed faster than the outer voltage loop and it is analyzed as first. Two different approaches to the current control have been presented in the following sections: the first one based on PI controllers and the second one based on P + Resonant controllers [9].

The grid voltage distortion as well as other nonlinear effects on the current spectrum can be compensated by additional resonant harmonic compensator. Since the proposed system basic function is to exchange active power, the unity power factor (PF) is considered for the fundamental current component.

### 1.4.1 PI Current Controller in a $d$ - $q$ rotating frame

In order to control the single-phase SSBC MMCC with PI regulator in the  $d$ - $q$  rotating reference frame, an Imaginary Orthogonal Converter (IOC) must be introduced. The IOC has the same components of the real power stage, moreover the state variables and

control references are assumed  $90^\circ$  phase-shifted compared with their counterparts in the real power stage, as in Fig. 1.5. In order to determine its related variables, the average model of this fictitious circuit has been derived, where  $\alpha$  denotes the real component while  $\beta$  denotes the imaginary component averaged in a sampling period.

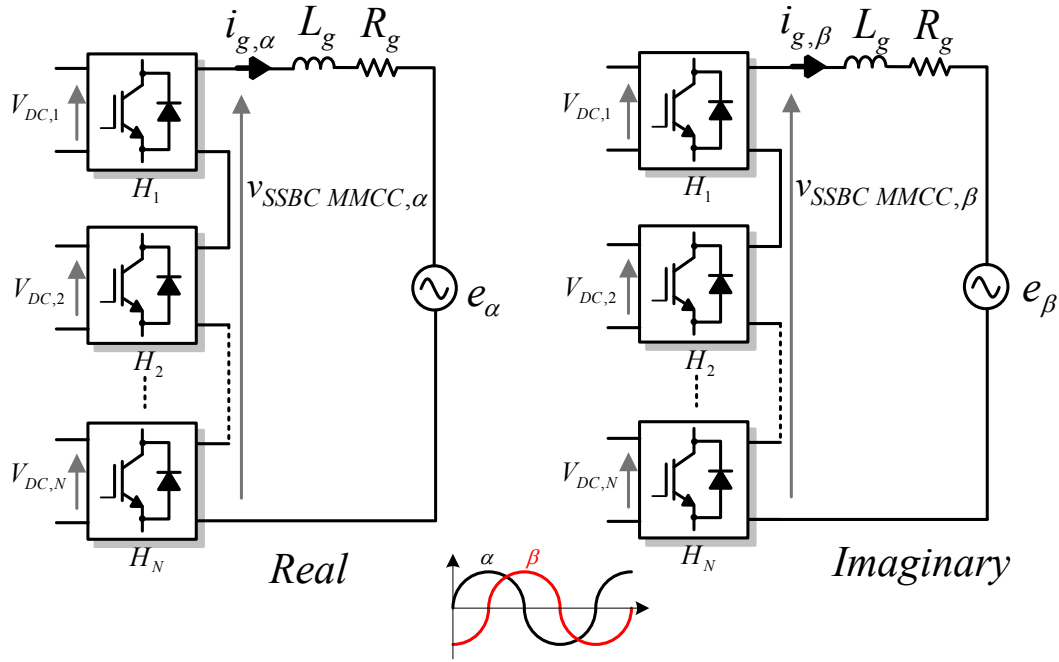


Fig. 1.5: Real and imaginary SSBC MMCC stages.

The AC voltage equations expressed in the  $d$ - $q$  frame, synchronous with the grid voltage vector, are:

$$L_g \frac{dI_{g,d}}{dt} + R_g I_{g,d} = V_{SSBC\ MMCC,d} - E_d + \omega L_g I_{g,q} \quad (1.31)$$

$$L_g \frac{dI_{g,q}}{dt} + R_g I_{g,q} = V_{SSBC\ MMCC,q} - E_q - \omega L_g I_{g,d} \quad (1.32)$$

To overcome the limit of the PI in dealing with sinusoidal reference and harmonic disturbances, the PI control is implemented in a  $d$ - $q$  frame rotating with angular speed  $\omega$ , where  $\omega = 2\pi f$  and  $f$  is the grid frequency.

The scheme of the classical control in a rotating frame is reported in Fig. 1.6 and the rotating frame is defined as synchronous, as already pointed out. If the  $d$ - $q$  frame is

oriented such that the  $d$  axis is aligned on the grid voltage vector the control is called voltage oriented control (VOC).

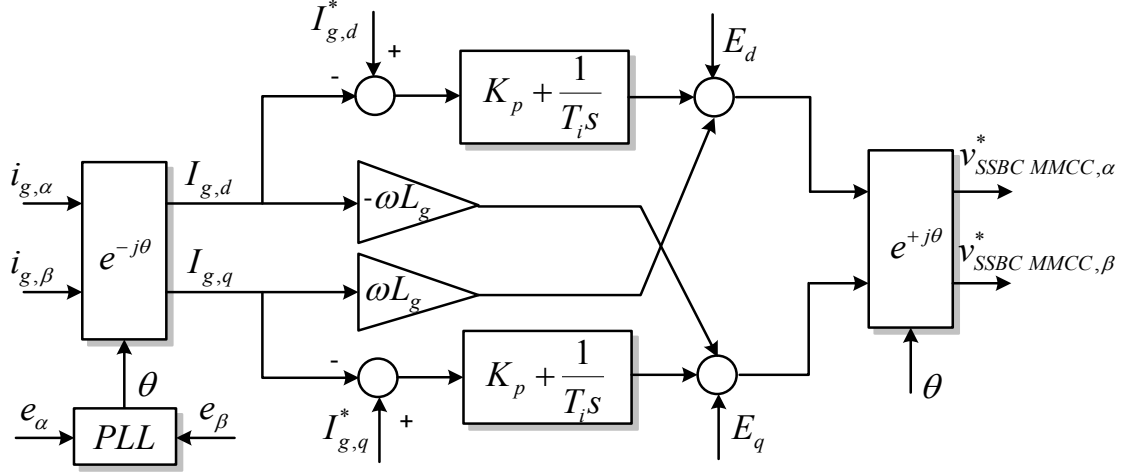


Fig. 1.6: Current control scheme in VOC

#### 1.4.2 PI Current Controller Design

The design procedure for the PI controller is here described. Considering the perfect decoupling of the mutual coupling terms in Fig. 1.6, the total control structure in the  $d$ - $q$  frame, results in a closed current loop as in Fig. 1.7.

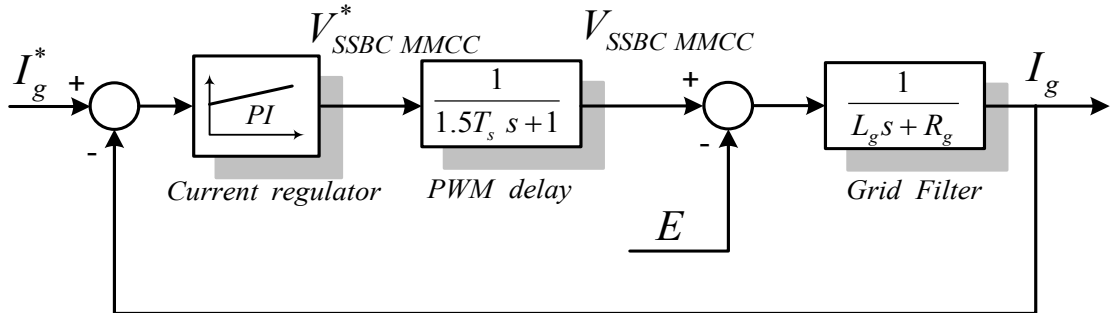


Fig. 1.7: Closed current loop with a PI controller

The PI current regulator is defined in Laplace domain with the following transfer function  $G_{PI}(s)$ :

$$G_{PI}(s) = K_p + \frac{1}{T_i s} \quad (1.33)$$

where  $K_p$  is the proportional gain, while  $T_i$  is the integral time constant. The PWM delay block represents the sum of two contributes: the delay due to the computation time  $T_s$

and the delay of the PWM  $0.5T_s$ , indicating with  $T_s$  the sampling period [10]. The converter is represented with a delay transfer function:

$$G_d(s) = \frac{1}{\frac{3}{2}T_s s + 1} \quad (1.34)$$

The plant is represented by the grid inductance  $L_g$  with its own resistance  $R_g$ .  $G_f(s)$  denotes the transfer function of the plant:

$$G_f(s) = \frac{1}{L_g s + R_g} \quad (1.35)$$

Choosing the PI integrator time constant  $T_i$  equal to the plant time constant  $T$ :

$$T_i = T = \frac{L_g}{R_g} \quad (1.36)$$

with the aim to delete the slower plant pole and supposing a perfect pole-zero cancellation, the current closed-loop transfer function in the s-Laplace domain is:

$$H_{I_g}(s) = \frac{\frac{2K_P}{3T_s L_g}}{s^2 + \frac{2}{3T_s}s + \frac{2K_P}{3T_s L_g}} \quad \omega_n^2 = \frac{2K_P}{3T_s L_g} \quad 2\xi\omega_n = \frac{2}{3T_s} \quad (1.37)$$

Choosing to have a system optimally damped (i.e. with a 5% overshoot) leads to  $\zeta = 0.707$  and thus to:

$$K_P = \frac{L_g}{3T_s} \quad (1.38)$$

Finally the closed loop transfer function results in:

$$H_{I_g}(s) = \frac{\frac{2}{(3T_s)^2}}{s^2 + \frac{2}{3T_s}s + \frac{2}{(3T_s)^2}} \quad (1.39)$$

The step response of the current loop with a  $T_s = 10 \text{ kHz}$ ,  $L_g = 5 \text{ mH}$  and  $R_g = 1 \text{ m}\Omega$  is depicted in Fig. 1.8, showing a fast dynamic in terms of settling time  $T_{\text{settling}(2\%)} = 0.00126 \text{ s}$  and an overshoot of 4.32% as specification. The value of the controller parameters have been chosen with respect to (1.36) and (1.38), resulting in  $K_p = 16.7$  and  $T_i = 5$ .

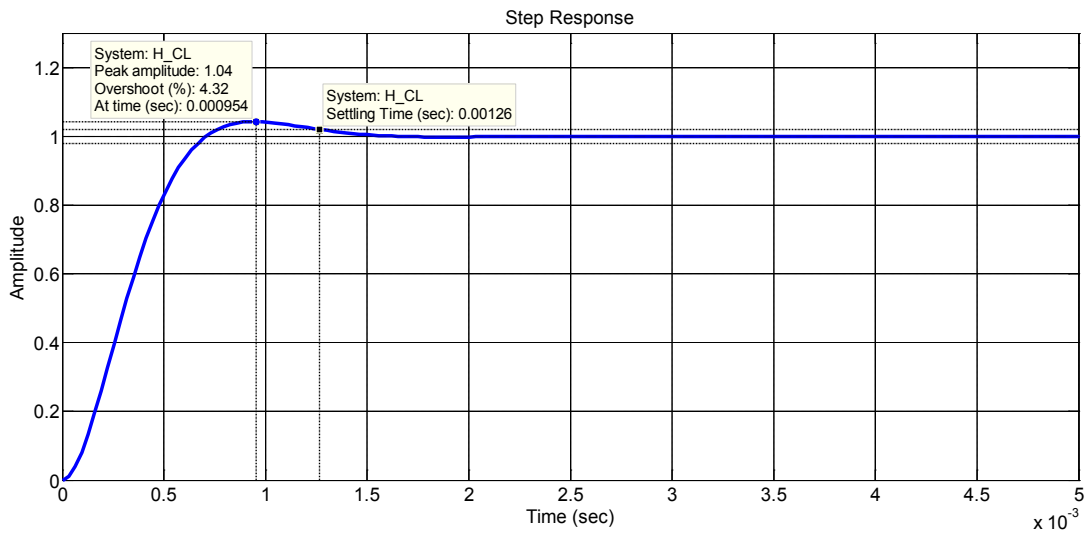


Fig. 1.8: Step response - Optimally damped current loop.

### 1.4.3 $P + Resonant$ Current Controller

When the control is developed in the  $d$ - $q$  reference frame, PI controllers provide optimal performances since they process direct quantities. On the contrary PI controllers cannot ensure tracking capability for single-phase systems because the current reference is sinusoidal [9]. The implementation of current control based on a  $P + Resonant$  (PR) controller is shown in Fig. 1.9. In it, the inverter transfer function takes into consideration the process delay which is  $T_s$  and the PWM modulation delay, which is  $0.5T_s$ .

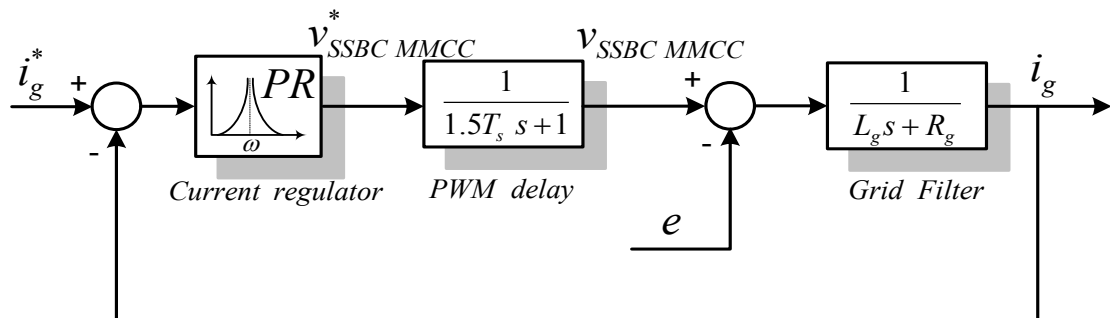


Fig. 1.9: Current loop based on a PR controller.

The PR current regulators guarantee optimal tracking capability of sinusoidal references since they are based on the internal model principle theory; it is defined in s-Laplace domain with the following transfer function  $G_{PR}(s)$  [9]:

$$G_{PR}(s) = K_P + \frac{K_i s}{s^2 + \omega^2} \quad (1.40)$$

where  $\omega$  is the resonant frequency of the PR controller accorded to the grid fundamental frequency. The resonant control (PR) obtains a theoretical infinite gain at the frequency of interest  $\omega$ . This frequency is also called resonance frequency and hence the name of this control. Several works [11-12] have described the resonant control as a displacement of the frequency spectrum of an ideal integrator. The Bode diagram of PR controller is shown in Fig. 1.10, with the value of  $K_p$  defined as in (1.38) and  $K_i = 1000$ .

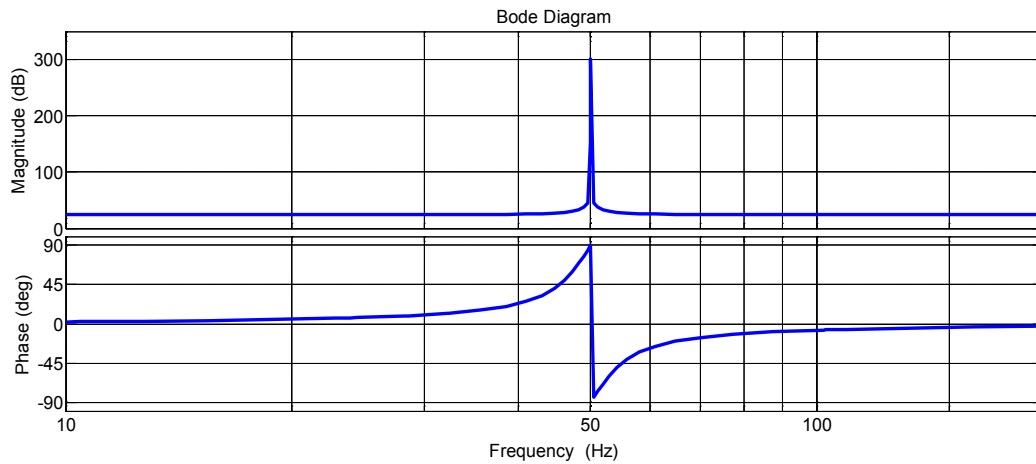


Fig. 1.10: Bode diagram of the resonant controller considering a resonance frequency of 50Hz.

Many researchers have worked on the design and improvement of different techniques for implementing resonant controllers capable of guaranteeing the stability of the system, even under distorted and unbalanced operating conditions. These techniques can be divided into three categories according to their characteristics at the resonant frequency:

- Resonant control with infinite gain and no phase control at the resonant frequency;
- Resonant control with finite gain and no phase control at the resonant frequency;
- Resonant control with infinite gain and phase control at the resonant frequency.

In the first category, there is the Second Order Generalized Integrator (SOGI) [13-14]. It has an excellent selectivity but in applications where several harmonics have to be compensated, such as an Active Power Filter (APF), the fact of adding more SOGIs in parallel may endanger the system stability.

In the second category, the Second Order Generalized Integrator for Quadrature-Signal Generation (SOGI-QSG) can be found [15]. Its main characteristic is the finite gain at the resonant frequency. This ensures the control stability at the expense of having a very poor performance when it comes to harmonic compensation. In the end, the third category can be found the Second Order Generalized Integrator with Lead-Lag Network (SOGI-LLN) [16-17]. It allows controlling the phase of the open-loop system at the resonant frequency and the phase margin.

These controller present different characteristics, but the common goal is to achieve the maximum gain at the resonant frequency while ensuring the system stability. In the considered case study resonant controllers based on SOGI technique are used.

These controllers present different characteristics, but the common goal is to achieve the maximum gain at the resonant frequency while ensuring the system stability. In the considered case study resonant controllers based on SOGI technique are used.

The transfer function of the SOGI exhibits two poles placed at  $\pm j\omega$  and one zero placed in the origin. Its continuous block diagram is shown in Fig. 1.11

$$G_{SOGI}(s) = \frac{s}{s^2 + \omega^2} \quad (1.41)$$

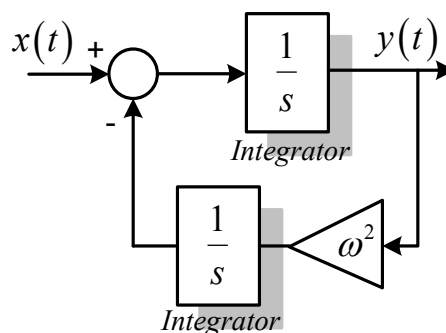


Fig. 1.11: Block diagram of the continuous time SOGI.

The Bode diagram of the SOGI in Fig. 1.12 shows an infinite gain at  $f = 50 \text{ Hz}$  and an inversion of the phase from  $90^\circ$  to  $-90^\circ$  in correspondence of the resonance frequency.

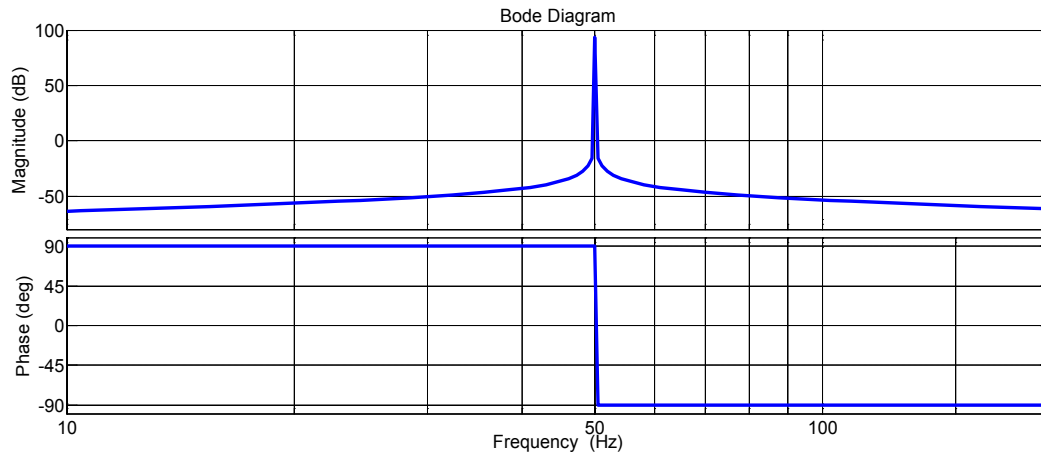


Fig. 1.12: Bode diagram of the continuous time SOGI

One of the main characteristics of the SOGI is that it presents a very narrow bandwidth around the resonant frequency in order to introduce high selectivity. In addition, it also rejects a DC component because it has a zero placed at  $s = 0$  leading an infinite attenuation at  $f = 0$ .

#### 1.4.4 $P + Resonant Current Controller Design$

The second term in (1.40) is a Generalized Integrator (GI) [18]. Thus a PR controller has much in common with a common PI controller. The difference consists only in the way the integration action takes part. The integrator integrates frequencies very close to the resonance frequency without stationary error or phase shift. The proportional gain  $K_p$  is tuned in the same way as for the PI controller, as in eq.(1.38). For harmonic compensation, it determines the order of harmonics that can be regulated without violating the stability limit.

In Fig. 1.13, the Bode diagrams of the current open loop  $G_{OL}(s)$  with Proportional and with  $P + Resonant$  controller are compared, using as value for the proportional parameter  $K_p$  that it is defined in (1.38), while  $K_i = 1000$ . In Fig. 1.13, it can be noticed that only  $K_p$  influences the dynamics of the system since the generalized integrator influences the Bode diagrams only around the resonance frequency.

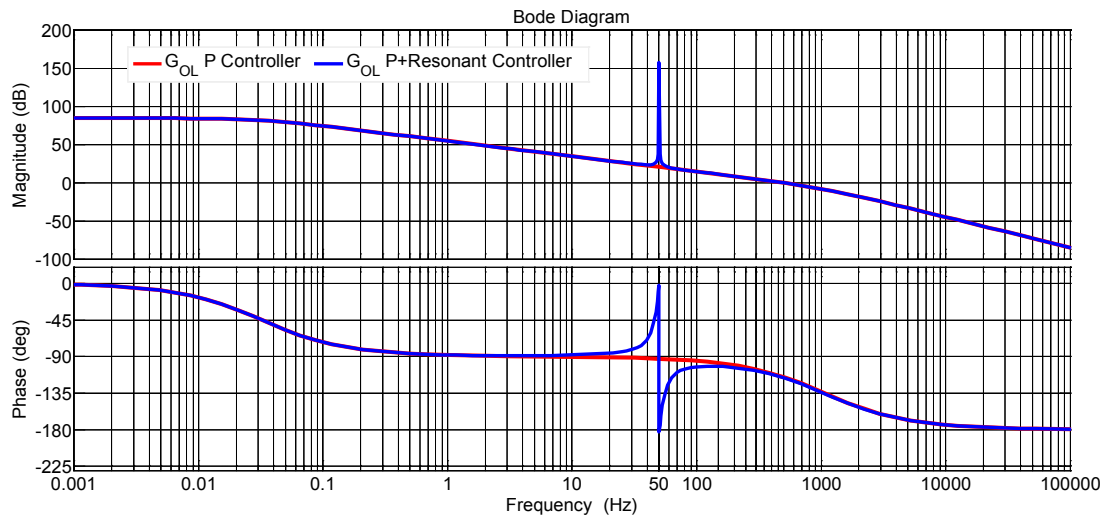


Fig. 1.13: Current open loop Bode diagrams with P and PR controller.

In order to verify the P + Resonant current control performances, a 5-levels SSBC MMCC has been assembled based on IGBT Danfoss modules DP25H1200T101616 and controlled with a dSPACE SCALEXIO platform based on DS2655 FPGA baseboards; each board is programmed through the FPGA Xilinx Blockset Toolbox. The power stage parameters are summarized in Tab. 1.3.

A complete model of the 5-level SSBC MMCC in inverter operation has been developed through the PLECS Toolbox integrated in the Simulink environment. The same control system has been used for simulation and experimental tests in order to compare the results. The power parameters are the same reported in Tab. 1.3 and a constant DC voltage source has been assumed as input to each DC-Link.

Tab. 1.3: Power Stage Parameters 5-levels SSBC MMCC.

<i>Symbol</i>	<i>Description</i>	<i>Value</i>
$E$ (RMS)	RMS grid Voltage	230 V (RMS)
$L_g$	AC Inductor filter	3.8 mH
$R_g$	AC Grid Impedance	1 m $\Omega$
$V_{DC,1} \sim V_{DC,2}$	DC Voltage in each cell	250 V
$C_{Cell,1} \sim C_{Cell,2}$	MV Capacitor	420 $\mu$ F
$f_{sw}$ SSBC MMCC	Switching Frequency	10 kHz

Due to the presence of a thermal monitoring based on an Infrared Camera, the IGBT modules are opened and without the insulating gel; therefore experimental and simulation results have been made under low voltage condition. A reference voltage ( $V_{DC,1} + V_{DC,2}$ ) of  $500V$  is set, representing a tradeoff between low voltage and the minimum value for grid parallel operation. The sinusoidal current reference is obtained multiplying the unitary sinusoidal signal (output of the PLL and signal in phase with the grid voltage) by  $I_g^*$ . In Fig. 1.14, the grid current is reported in case the current reference steps from,  $I_g^*=1A$  to  $I_g^*=8A$ . It is possible to observe how perfectly the grid voltage and the current are synchronized. The grid current tracks the reference waveform in approximately one period, confirming the goodness of current control tuning. The same results are obtained experimentally as shown in Fig. 1.15.

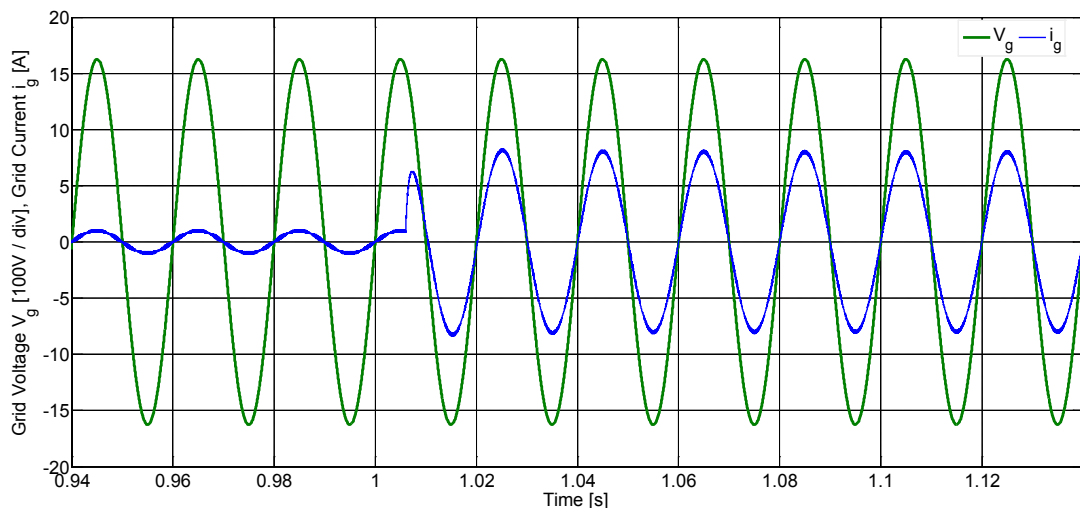


Fig. 1.14: Simulation - Grid voltage and current in case of step reference form 1 A to 8 A.

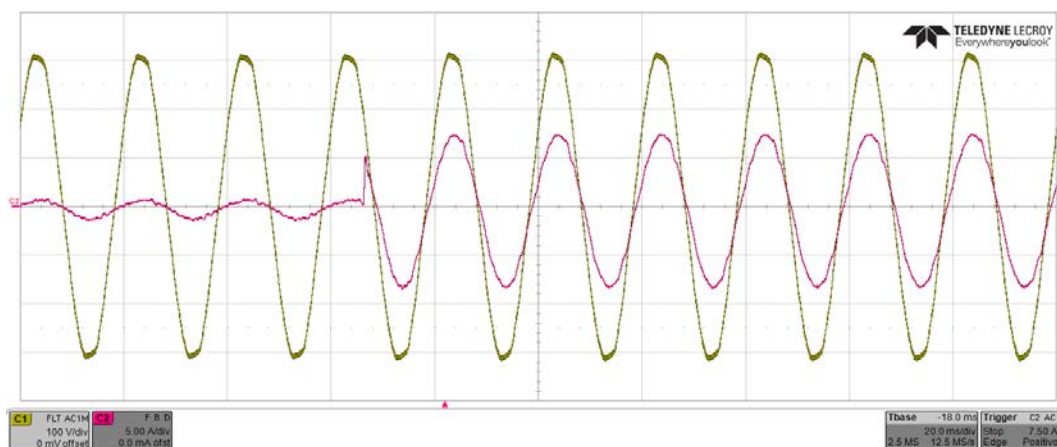


Fig. 1.15: Prototype - Grid voltage and current in case of step reference form 1 A to 8 A.

Differently from the inverter operation, in the active rectifier operation a DC voltage control is needed to guarantee a constant  $V_{DC,i}$  voltage value. In the proposed cascaded control structure, the inner current loop has been tuned at least ten times faster than the outer DC voltage loop, in order to decouple their dynamics. In this case, it is possible to consider that the current loop is already in the steady-state when the voltage loop is in the transient state.

In Fig. 1.16, the acquired dSPACE Control Desk DC-Link voltages signals are represented in start-up rectifier operation. At  $t=1s$  the voltage control starts and the DC-Link voltages  $V_{DC,1}$  and  $V_{DC,2}$  vary from the rectified grid value to the reference of  $250V$  in each SSBC MMCC cell.

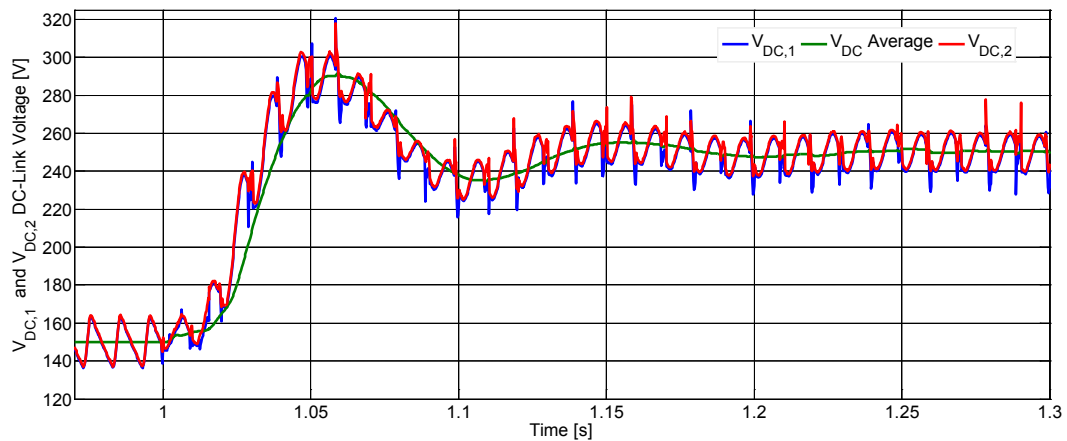


Fig. 1.16: Prototype -  $V_{DC,1}$  and  $V_{DC,2}$  DC Link voltages in start-up operation.

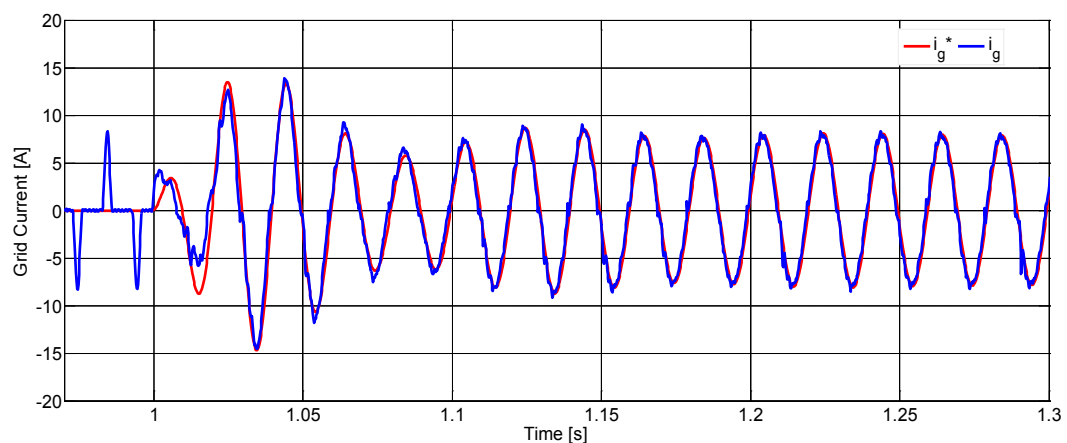


Fig. 1.17: Prototype - Grid current (blue) and grid current reference (red) in start-up operation.

In Fig. 1.17 the grid current reference generated by the voltage loop and the measured grid current during the start-up operation are shown. At  $t=1s$  the current reference vary from zero to a certain value as depicted by the red line in Fig. 1.17; before  $t=1s$  the measured current assumes the typical distorted waveform of a passive rectifier, while after  $t=1s$  it catches the reference waveform in less than one period.

#### 1.4.5 Harmonic Current Compensation

In order to compensate the harmonics present into the main grid, GI tuned to resonate at the desired frequency [19], can be added in the current control. Thanks to the high selectivity, the harmonic compensators play an important role in this operation. The transfer function of the harmonic compensator designed to compensate the 3rd, 5th and 7th harmonics (as they are the most prominent harmonics) is:

$$G_h(s) = \sum_{h=3,5,7} \left( \frac{K_{i,h} s}{s^2 + (h\omega)^2} \right) \quad (1.42)$$

where  $h$  is the harmonic order to be compensated and  $K_{i,h}$  represents the individual resonant gain, which must be tuned relatively high (but within the stability limit) in order to minimize the steady-state error. An interesting feature of the harmonic compensator is that it does not affect the dynamics of the fundamental PR controller, as it compensates only frequencies that are very close to the selected resonant frequencies [10]. Fig. 1.17 and Fig. 1.18 show the resonant controller plus harmonic compensators and the Bode diagrams of the current control loop.

IEEE 1547 and IEC 61727 defined the harmonic level accepted in terms of power quality, through the percentage Total Harmonic Distortion (THD %) index; the level fixed for the THD is  $< 5\%$ . The THD is calculated as shown in (1.43), where  $h$  is the harmonic order and  $X_h$  is the RMS value of the signal evaluated at the harmonic  $h^{th}$ .

$$THD_X = \frac{\sqrt{\sum_{h=2}^{40} X_h^2}}{X_1} \quad (1.43)$$

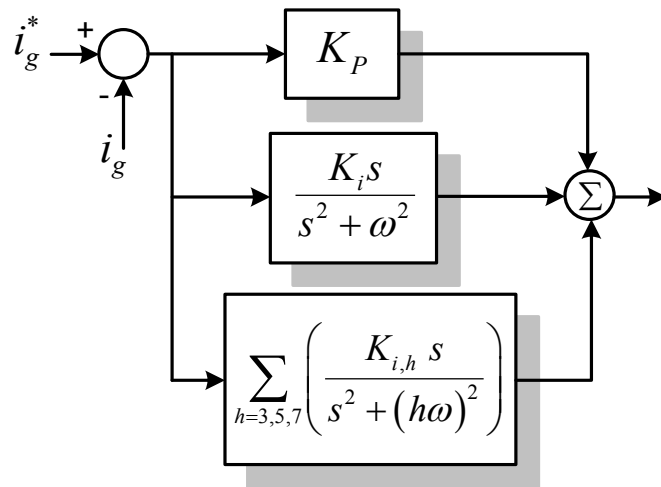


Fig.1.17: Block scheme of current control added with resonant compensator of 3<sup>rd</sup>, 5<sup>th</sup> and 7<sup>th</sup> harmonics.

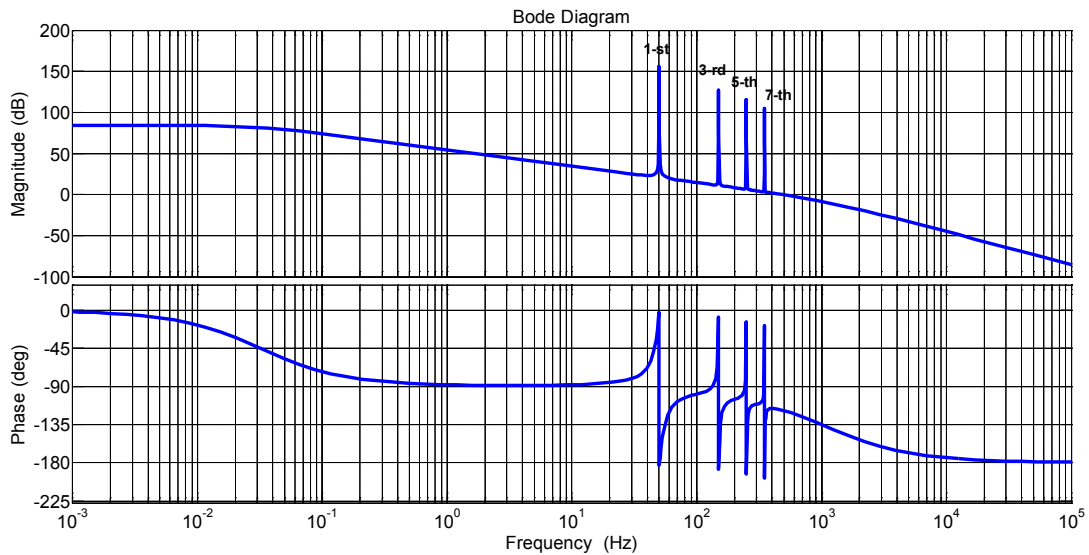


Fig. 1.18: Bode diagrams of resonant compensator of 3<sup>rd</sup>, 5<sup>th</sup> and 7<sup>th</sup> harmonics in current loop.

The harmonic spectrum of the grid current is shown in Fig. 1.20 where it can be seen that the THD decreases in function of the insertion of the resonant compensators. In fact, without harmonic compensators the THD(%) = 6.2% which is over the standard limit. Differently in Fig. 1.22, with all harmonic compensators enabled the THD(%) = 3%, which is under the standard limit. Fig. 1.19 and Fig. 1.21 show the grid current with and without the harmonic compensators effect respectively.

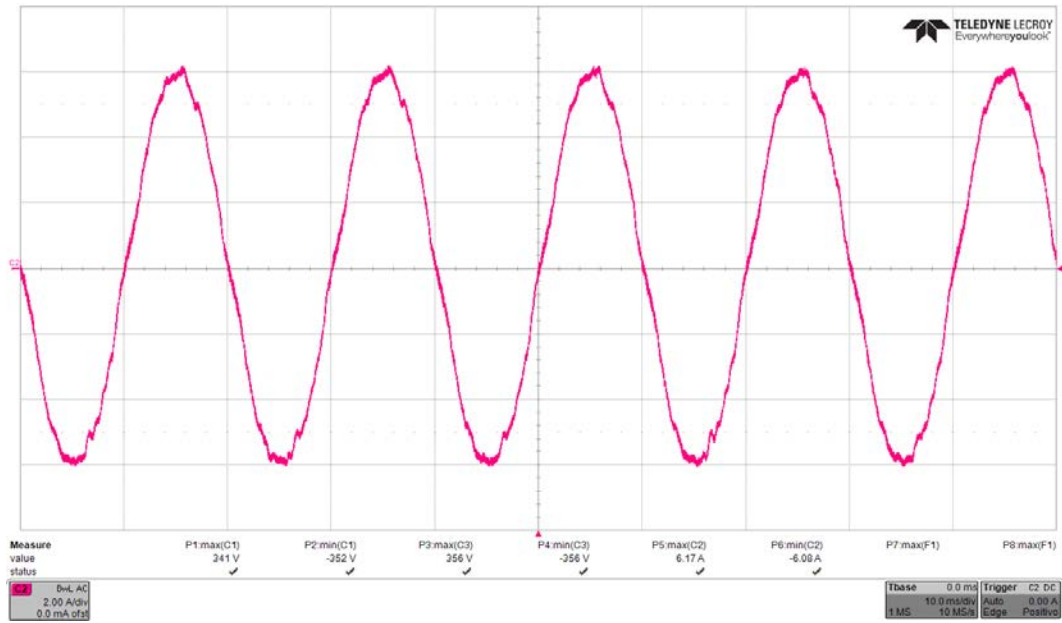


Fig. 1.19: Grid Current without harmonics compensation in current loop, THD(%) = 6.2%.

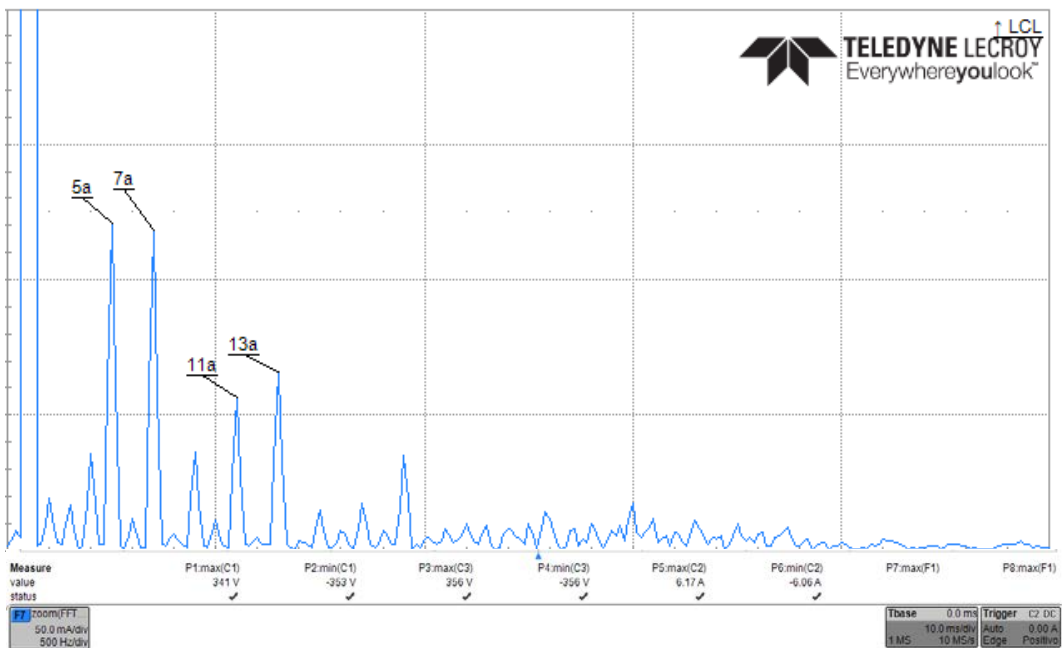


Fig. 1.20: FFT of grid current without harmonics compensation, THD(%) = 6.2%.

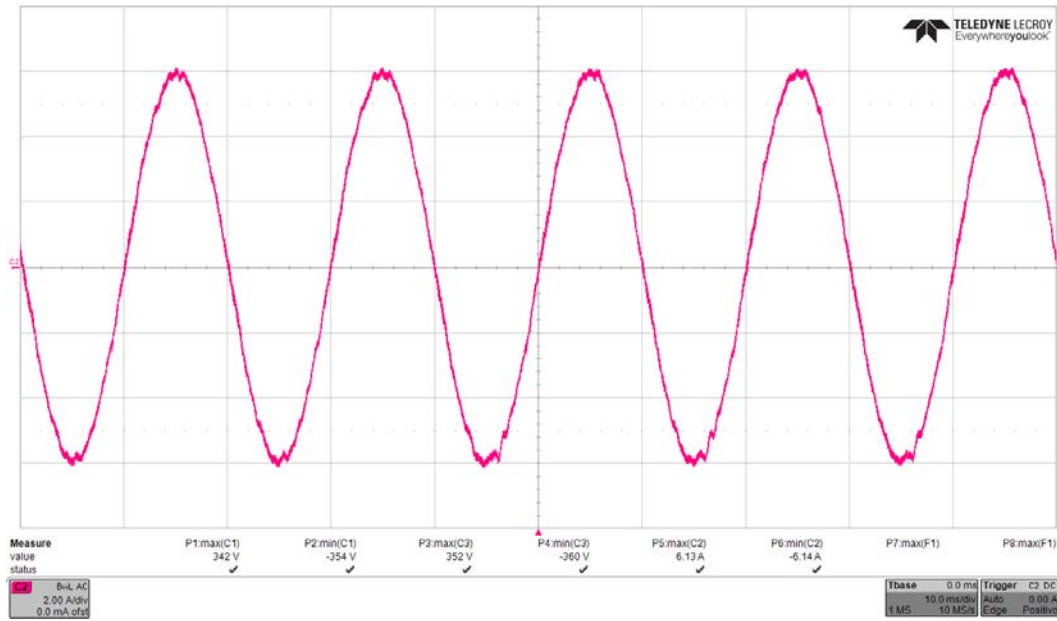


Fig. 1.21: Grid Current with harmonics compensation in current loop, THD(%) = 3%.

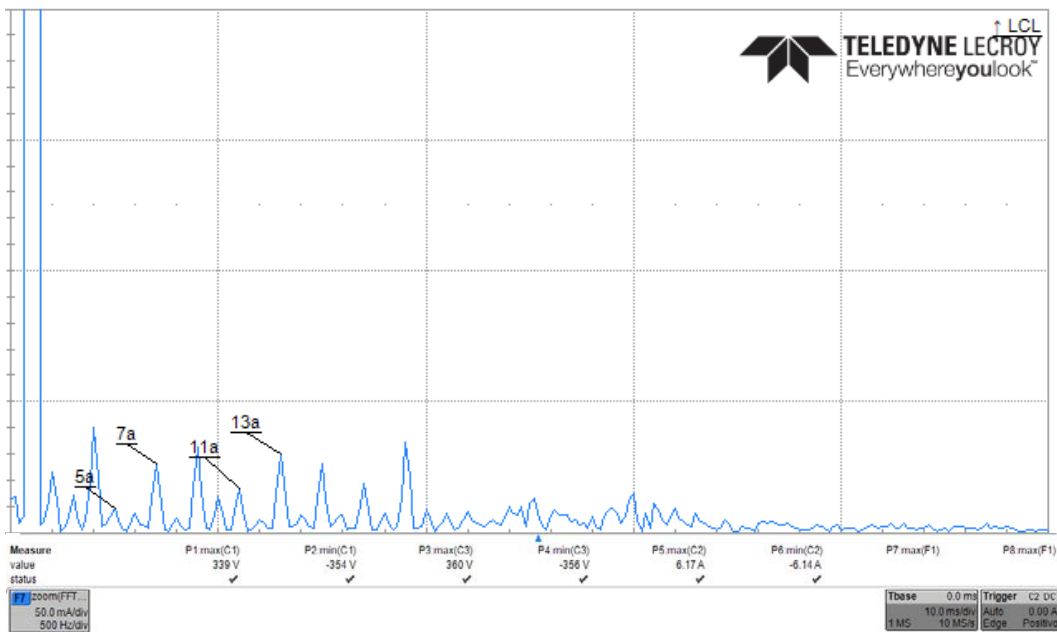


Fig. 1.22: FFT of grid current with harmonics compensation, THD(%) = 3%.

## 1.5 SSBC MMCC Small Signal Model

Starting from the average model of the SSBC MMCC described by equations (1.29) - (1.30) and applying the appropriate transformations, that allow to move from a stationary to a rotating system, the following direct equations for the SSBC MMCC can be derived, for both the AC and DC side:

$$L_g \frac{dI_g(t)}{dt} = N(M(t)V_{DC}(t)) - E(t) \quad (1.44)$$

$$C_i \frac{dV_{DC,i}(t)}{dt} = \frac{1}{2}M(t)I_g(t) - I_{o,i}(t) \quad V_{DC,i} = V_{DC} \quad i=1,2,\dots,N \quad (1.45)$$

where  $I_{o,i}$  is the DC output of the  $i$ -th H-Bridge,  $V_{DC,i}$  is the DC voltage on the single H-Bridge,  $E$  is the direct component of the grid voltage,  $I_g$  is the direct component of the grid current,  $M$  is the direct component of the modulating signal. With perfectly balanced loads and therefore without voltage unbalancing, each cell is driven with the same modulating signal.

Because of the non linear term  $M(t)V_{DC}(t)$  in equation (1.44), and  $\frac{1}{2}M(t)I_g(t)$  in equation (1.45), in order to derive the linear model of SSBC MMCC in the s-Laplace domain, the small signal linearization around the equilibrium point at the rated conditions is necessary.

$$L_g \frac{d(\tilde{I}_g + \bar{I}_g)}{dt} = N(\tilde{M} + \bar{M})(\tilde{V}_{DC} + \bar{V}_{DC}) - (\tilde{E} + \bar{E}) \quad (1.46)$$

$$C_i \frac{d(\tilde{V}_{DC,i} + \bar{V}_{DC,i})}{dt} = \frac{1}{2}(\tilde{M} + \bar{M})(\tilde{I}_g + \bar{I}_g) - (\tilde{I}_{o,i} + \bar{I}_{o,i}) \quad (1.47)$$

where the notation  $(\tilde{X} + \bar{X})$  stays for the small perturbation of signal  $X$  added to the steady-state value. Assuming the second-order signal perturbations to be zero, the small signal linearization of (1.46) and (1.47) leads to:

$$L_g \frac{d\tilde{I}_g}{dt} = N(\tilde{M}\bar{V}_{DC} + \bar{M}\tilde{V}_{DC}) \quad (1.48)$$

$$2C_i \frac{d\tilde{V}_{DC,i}}{dt} = \tilde{M}\bar{I}_g + \bar{M}\tilde{I}_g - 2\tilde{I}_{o,i} \quad (1.49)$$

This two linear equation can be transformed into the s-Laplace domain, resulting in:

$$\tilde{I}_g(s) = \frac{N\bar{V}_{DC}\tilde{M}(s) + N\bar{M}\tilde{V}_{DC}(s)}{L_g s} \quad (1.50)$$

$$\tilde{V}_{DC,i}(s) = \frac{\tilde{M}(s)\bar{I}_g + \bar{M}\tilde{I}_g(s) - 2\tilde{I}_{o,i}(s)}{2C_i s} \quad (1.51)$$

In order to derive the transfer function between the input  $\tilde{I}_g$  and the output  $\tilde{V}_{DC,i}$ , the small signal modulation signal  $\tilde{M}$  has been derived from (1.50) as:

$$\tilde{M}(s) = \frac{L_g \tilde{I}_g(s)s - N\bar{M}\tilde{V}_{DC,i}(s)}{N\bar{V}_{DC,i}} \quad \text{with} \quad \tilde{V}_{DC,i} = \tilde{V}_{DC} \quad i=1,2,\dots,N \quad (1.52)$$

In (1.52) the system is supposed to be balanced, hence, the DC small variations are equal in each cell. With these hypotheses in equation (1.52),  $\tilde{V}_{DC}$  has been replaced with  $\tilde{V}_{DC,i}$  and  $\bar{V}_{DC}$  with  $\bar{V}_{DC,i}$ .

Substituting eq.(1.52) in (1.51):

$$\tilde{V}_{DC,i}(s) = \frac{\left( \frac{L_g \tilde{I}_g(s)s - N\bar{M}\tilde{V}_{DC,i}(s)}{N\bar{V}_{DC,i}} \right) \bar{I}_g + \bar{M}\tilde{I}_g(s) - 2\tilde{I}_{o,i}(s)}{2C_i s} \quad (1.53)$$

$$\tilde{V}_{DC,i}(s) = \frac{\bar{I}_g L_g \tilde{I}_g(s)s - N\bar{I}_g \bar{M}\tilde{V}_{DC,i}(s) + N\bar{V}_{DC,i} \bar{M}\tilde{I}_g(s) - 2N\bar{V}_{DC,i} \tilde{I}_{o,i}(s)}{2N\bar{V}_{DC,i} C_i s} \quad (1.54)$$

$$\tilde{V}_{DC,i}(s) = \frac{(\bar{I}_g L_g s + N\bar{V}_{DC,i} \bar{M})}{(2N\bar{V}_{DC,i} C_i s + N\bar{I}_g \bar{M})} \tilde{I}_g(s) - \frac{2N\bar{V}_{DC,i}}{(2N\bar{V}_{DC,i} C_i s + N\bar{I}_g \bar{M})} \tilde{I}_{o,i}(s) \quad (1.55)$$

Equation (1.55) indicates that the voltage variation on the DC-Link of each H-Bridges depends on both grid current and DC current variations, respectively indicated with  $\tilde{I}_g$  and  $\tilde{I}_{o,i}$ . In the defined control structure,  $\tilde{I}_{o,i}$  is considered as a disturbance to reject in the voltage loop. The entire DC-link small signal model is depicted in Fig. 1.23.

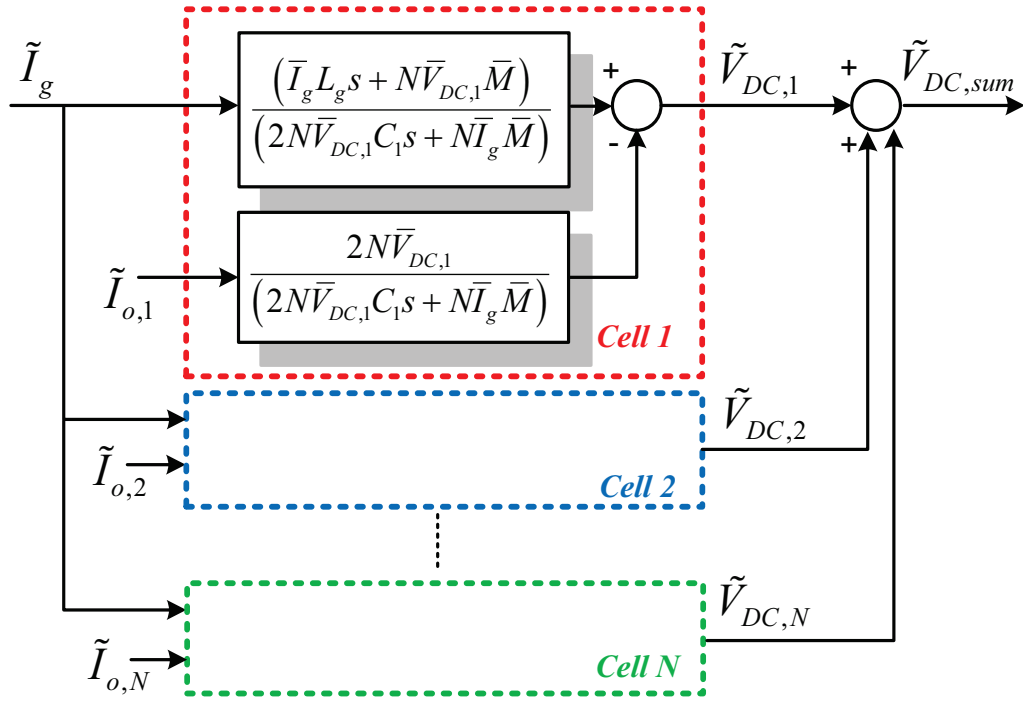


Fig. 1.23: DC-Link small signal model of a 2N+1 level SSBC MMCC.

To control the total voltage  $\tilde{V}_{DC,sum}$  obtained as sum of each DC voltage, the equivalent block model, with integrated the current control loop is depicted in Fig. 1.24. In this equivalent model, for  $i=1,2,\dots,N$ , the DC voltages, the DC currents and DC-link capacitances are assumed all equal.. The model equation is defined as follow:

$$\tilde{V}_{DC,sum}(s) = \frac{(\bar{I}_g L_g s + N\bar{V}_{DC}\bar{M})}{(2\bar{V}_{DC}C s + \bar{I}_g\bar{M})} \tilde{I}_g(s) - \frac{2N\bar{V}_{DC}}{(2\bar{V}_{DC}C s + \bar{I}_g\bar{M})} \tilde{I}_o(s) \quad (1.56)$$

where  $\tilde{V}_{DC,sum}$  is the controlled variable,  $\tilde{I}_g$  is the actuating signal and  $\tilde{I}_o$  is the external disturbance.

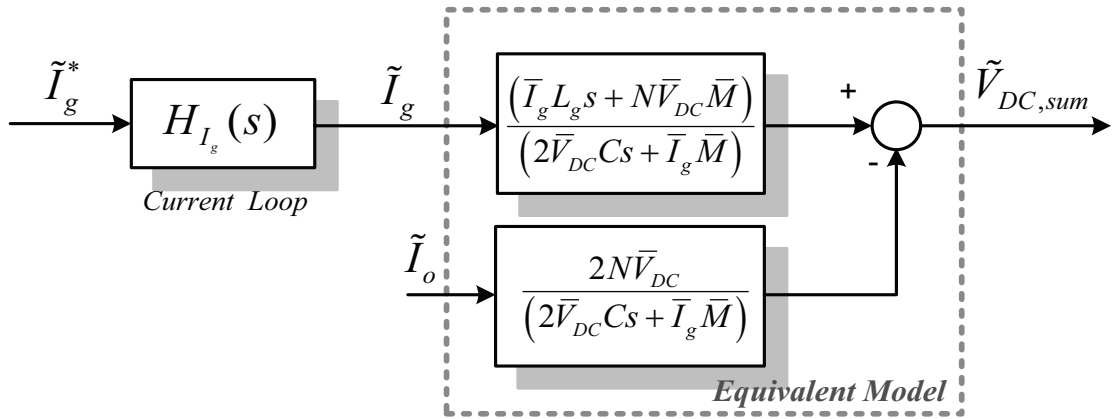


Fig. 1.24: Equivalent small signal model for the total  $V_{DC}$  voltage control.

It has been demonstrated that the same results using PI controllers in a synchronous frame can be obtained using generalized integrators (which offer infinite gain at a certain frequency) in a stationary reference frame. Indeed, a PI controller in a synchronous frame plus a PI controller in a counter-synchronous frame (a frame that rotates in the opposite direction with respect to the VOC  $d$ - $q$  frame) is equivalent to a P + Resonant controller in a stationary frame as demonstrated in [19] and in Appendix of [10]. With this considerations, if the internal current loop is designed to achieve short settling times and it is adjusted to be optimally damped, it can be described by a second-order transfer function as in eq. (1.39). The resulting open loop plant is a third-order system with three poles and one zero located in the real negative side of the Re-Im plan.

## 1.6 SSBC MMCC Voltage Control Loop

The control of the total voltage  $\tilde{V}_{DC, sum}$  is carried out by means of a PI regulator and considering as plant, the transfer function between the input variable, represented by the grid current reference  $\tilde{I}_g^*$ , and the output variable, represented by  $\tilde{V}_{DC, sum}$ .

The disturbance transfer function has the same poles of the controlled plant and consequently the same dynamic behavior; it means that with a PI controller, a good tracking and rejection capability can be achieved at the same time. The complete voltage control loop with a PI controller in the direct branch is represented in Fig. 1.25.

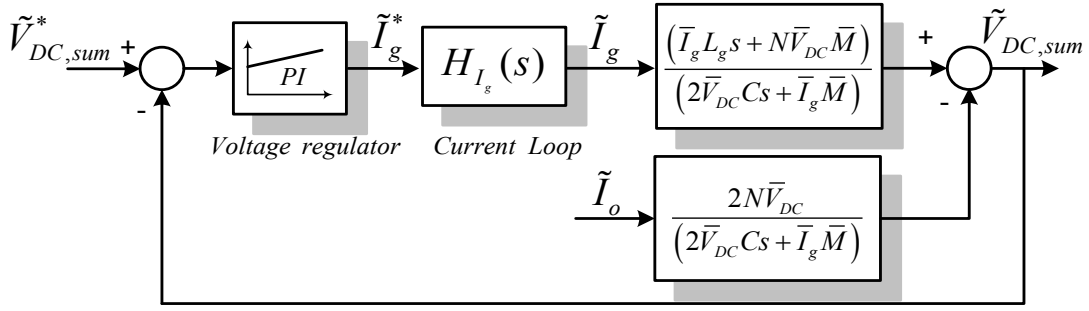


Fig. 1.25: PI Voltage Control loop.

The voltage open loop transfer function is:

$$G_{V_{DC}}(s) = \left( \frac{K_p (T_i s + 1)}{T_i s} \right) \left( \frac{\frac{2}{(3T_s)^2}}{s^2 + \frac{2}{3T_s}s + \frac{2}{(3T_s)^2}} \right) \left( \frac{N\bar{V}_{DC} (T_z s + 1)}{\bar{I}_g (T_p s + 1)} \right) \quad (1.57)$$

where  $K_p$  is the proportional gain,  $T_i$  is the integral time constant and  $T_z$  and  $T_p$  are defined respectively as:

$$T_z = \frac{\bar{I}_g L_g}{N\bar{V}_{DC}\bar{M}} \quad T_p = \frac{2\bar{V}_{DC}C}{\bar{I}_g\bar{M}} \quad (1.58)$$

### 1.6.1 PI Voltage Controller Design

The design of the voltage control loop is operated in order to decouple the internal current loop and the external voltage loop. As first step, the PI integrator time constant  $T_i$  has been chosen equal to the plant time constant  $T_p$ . Considering a perfect pole-zero cancellation, the voltage open-loop transfer function in the s-Laplace domain is:

$$G_{V_{DC}}(s) = \left( \frac{K_p \bar{M} N}{2C} \right) \frac{(T_z s + 1)}{s} \left( \frac{\frac{2}{(3T_s)^2}}{s^2 + \frac{2}{3T_s}s + \frac{2}{(3T_s)^2}} \right) \quad (1.59)$$

The Bode diagram of  $G_{VDC}(s)$  is represented in Fig. 1.26. From the figure it can be noticed that the closed loop system is stable with a phase margin of  $88^\circ$  at 6.44Hz frequency.

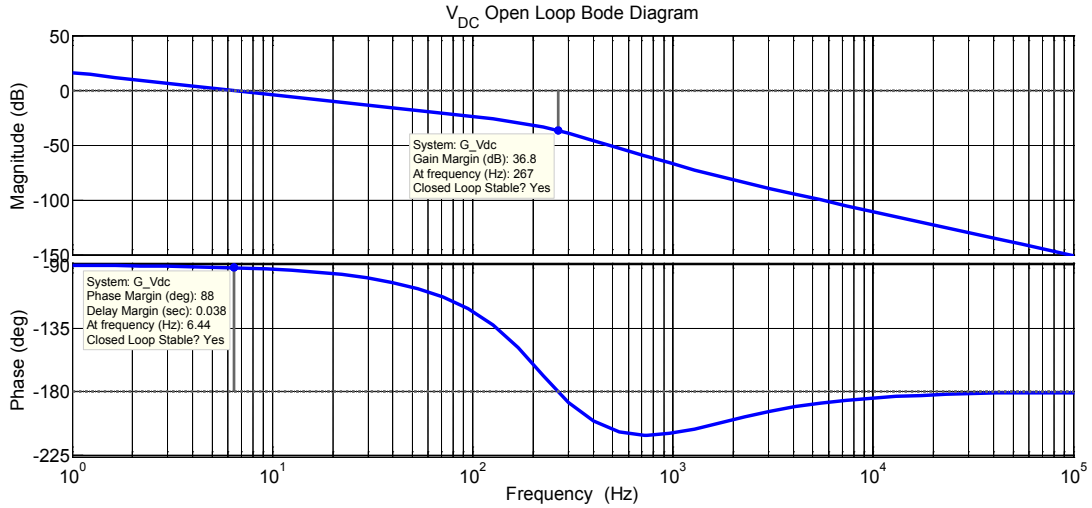


Fig. 1.26:  $V_{DC}$  Open Loop Bode diagram.

If the current control loop is adjusted to be optimally damped the following first-order approximation can be useful when calculating the bandwidth of the system and when designing the voltage loop with a bandwidth smaller than that of the current loop [10]:

$$\tilde{I}_g(s) \approx \frac{1}{(3T_s s + 1)} \tilde{I}_g^*(s) \quad f_{BW\_CL} = \frac{1}{6\pi T_s} \quad (1.60)$$

Substituting the second order current loop of eq.(1.59) with the first order current loop of (1.60), a new simplified open loop transfer function has been derived to describe the model of  $V_{DC}$ .

$$G_{V_{DC}}(s) = \frac{k(T_z s + 1)}{s(3T_s s + 1)} \quad \text{with } k = \frac{K_p \bar{M} N}{2C} \quad (1.61)$$

In Fig. 1.27, the simplified  $V_{DC}$  open loop Bode diagram is represented. From (1.61), the voltage closed-loop transfer function is determined as follow:

$$H_{V_{DC}}(s) = \frac{k(T_z s + 1)}{3T_s s^2 + (k T_z + 1)s + k} \quad (1.62)$$

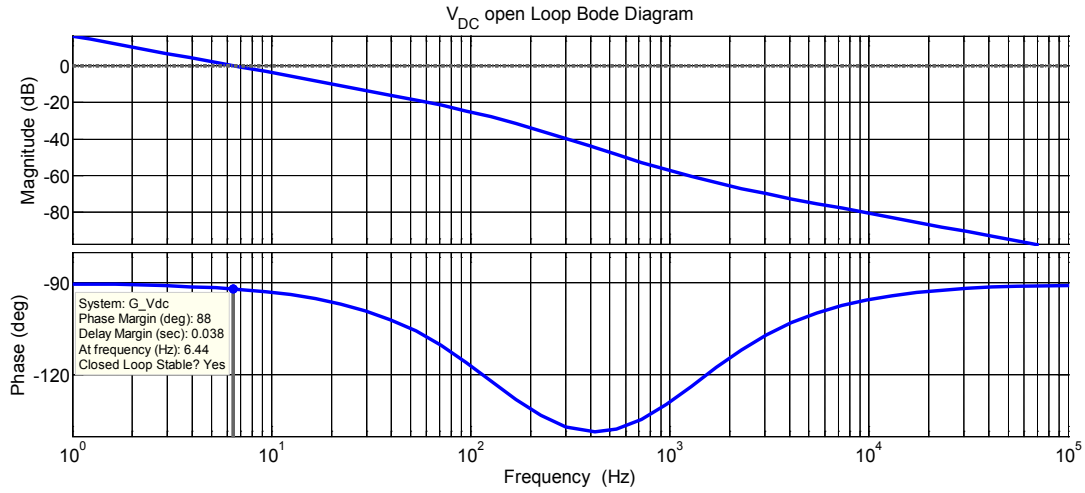


Fig. 1.27: Simplified  $V_{DC}$  Open Loop Bode diagram.

In the tuning procedure, the dynamic of  $T_z$  is neglected, and (1.62) is traced back to a canonical second order transfer function. This approximation is true when  $T_z$  is small in value, and the zero is located in high frequency. According to the mentioned hypothesis, the current closed loop results described by the following transfer function:

$$H_{V_{DC}}(s) = \frac{\frac{k}{3T_s}}{s^2 + \frac{(kT_z + 1)}{3T_s}s + \frac{k}{3T_s}} \quad (1.63)$$

Eq.(1.63) shows that the closed loop function depends on the value of  $K_p$ , which is the only tunable parameter to guarantee a bandwidth at least ten time smaller than that of the current loop. Eq.(1.63), can be reported to the canonic second order transfer function considering that:

$$\omega_n^2 = \frac{k}{3T_s} \quad 2\zeta\omega_n = \frac{(kT_z + 1)}{3T_s} \quad (1.64)$$

where  $\omega_n$  is the natural pulsation of the system and  $\zeta$  is the damping coefficient. Hence  $\omega_n^2$  can be expressed as:

$$\omega_n^2 = \left[ \frac{(kT_z + 1)}{6\zeta T_s} \right]^2 \quad \omega_n^2 = \frac{k}{3T_s} \quad (1.65)$$

A new formulation as function of  $k$  and  $\zeta$  can be obtained:

$$\frac{k}{3T_s} = \left( \frac{k T_z + 1}{6\zeta T_s} \right)^2 \rightarrow T_z k^2 + (2T_z - 12\zeta^2 T_s)k + 1 = 0 \quad (1.66)$$

Eq. (1.66) is satisfied for two  $k$  values and depending on the value of  $\zeta$ , these values can be real or imaginary. Only values of  $\zeta$  that make (1.66) an equation with real solutions can be chosen, and between the real  $k$  values, the smallest that ensures the stability of the system.

The proportional gain of the voltage PI controller  $K_p$  can be tuned as:

$$K_p = \frac{2kC}{\bar{M}N} \quad (1.67)$$

The results of the tuning method for a 5-levels single-phase SSBC MMCC ( $N=2$ ), characterized by a DC voltage of  $250V$  on the single cell and with a rated power  $P_n = 2kW$  (rated power of the entire system), are reported in the following. It is assumed that the system is connected to the main grid (whose amplitude is  $E = 230V_{RMS}$ ) by means of an inductive filter  $L_g = 3.8mH$  and that the capacity of each DC-Link is  $C = 420\mu$ . The sampling period is  $T_s = 1/3000s$ . The system is linearized around the following steady-state point:

$$\bar{I}_g = \frac{2P_n}{\bar{E}} = 12.5 \quad \bar{M} = \frac{\bar{E}}{2\bar{V}_{DC}} = 0.65 \quad (1.68)$$

From the pole-zero cancellation it results:

$$T_i = T_p = \frac{2\bar{V}_{DC}C}{\bar{I}_g\bar{M}} = 0.0263 \quad (1.69)$$

$$T_z = \frac{\bar{I}_g L_g}{N\bar{V}_{DC}\bar{M}} = 1.46 \cdot 10^{-4} \quad (1.70)$$

Solving eq. (1.66) and considering  $\zeta = 2.5$ , the value of  $K_p$  is:

$$K_p = \frac{2kC}{\bar{M}N} = 0.026 \quad (1.71)$$

Choosing  $\zeta = 2.5$  the second order canonical transfer function results in an overdamped system with two real poles in:

$$p_1 = \left(-\zeta + \sqrt{\zeta^2 - 1}\right)\omega_n = -42 \quad p_2 = \left(-\zeta - \sqrt{\zeta^2 - 1}\right)\omega_n = -964 \quad (1.72)$$

Both the poles are real and negative, it means that the closed loop is stable but the dynamic of the pole  $p_2$  is extinguished faster than that of  $p_1$ , hence the total step response of the control loop can be approximated to that of a first order system with the following transfer function:

$$H_1(s) = \frac{|p_1|}{s + |p_1|} \quad (1.73)$$

The settling time can be derived from the first order equivalent system as:

$$T_{setling}(5\%) \approx \frac{3}{|p_1|} = 0.072s \quad T_{setling}(2\%) \approx 100ms \quad (1.74)$$

The voltage step response of the small signal transfer function has been obtained in MATLAB simulation and it is represented in Fig. 1.28. The transient is typical of a first order system with highlighted the value of time settling:  $T_{setling}(5\%) = 0.072$  as specification.

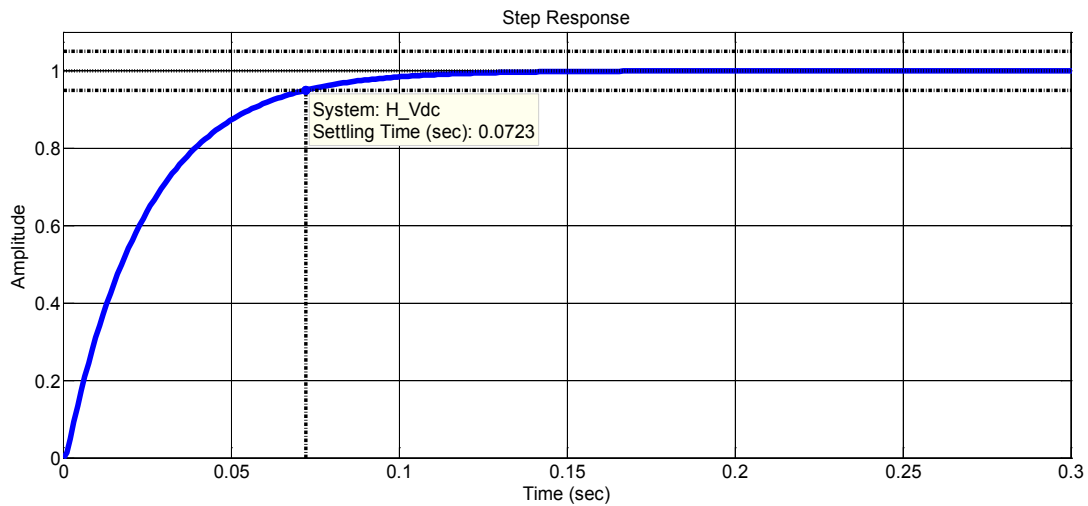


Fig. 1.28: MATLAB Small signal model - Voltage step response.

In Fig. 1.29 are represented two voltage open loop Bode diagrams:  $G_{open1}$  and  $G_{open2}$ .  $G_{open1}$  indicates the voltage open loop when the first order current loop approximation is

considered; while  $G_{open2}$  when the full second order current loop is considered. The aim of the entire cascaded control structure is to decouple both the current and voltage loops, and the comparison of  $G_{open1}$  and  $G_{open2}$  is of particular interest only in low-frequency domain. From the Fig. 1.29 it can be noticed that in low frequency the two systems have the same Bode diagram and this justifies the simplification used in the voltage regulator design.

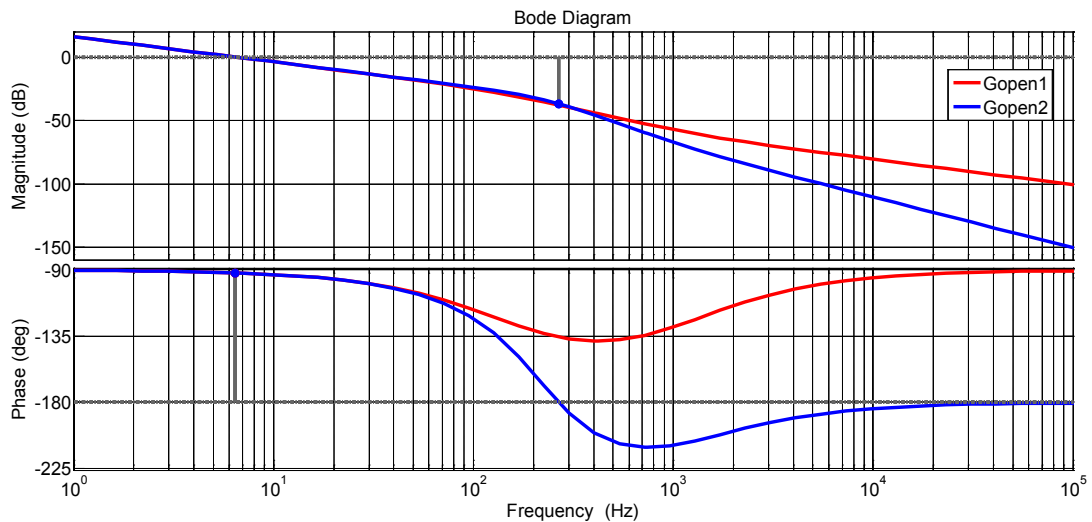


Fig. 1.29: Voltage open loop in two cases: 1) first order current loop 2) second order current loop.

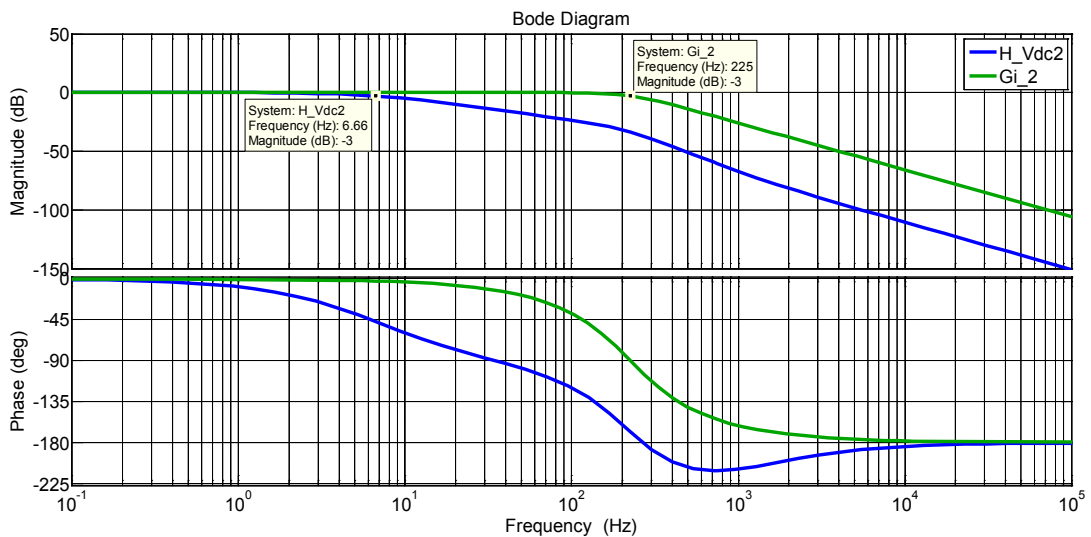


Fig. 1.30: MATLAB - Voltage and current closed loop Bode diagrams.

In Fig. 1.30 are represented both the Bode diagrams of the current closed loop ( $G_{i\_2}$  green line) and the voltage closed loop ( $H\_Vdc2$  blue line). The decoupling condition between the current and voltage dynamics has been verified comparing the bandwidths

of the two systems, and ensuring a distance in frequency of a decade between them;  $f_{BW\_CL} = 225\text{Hz}$  (current loop bandwidth) and  $f_{BW\_VL} = 6.6\text{Hz}$  (voltage loop bandwidth). To validate the SSBC MMCC small signal voltage model, the simulation results obtained through the switching model with those related to the small signal model have been compared, for different damping values (Fig. 1.31 - 1.32).

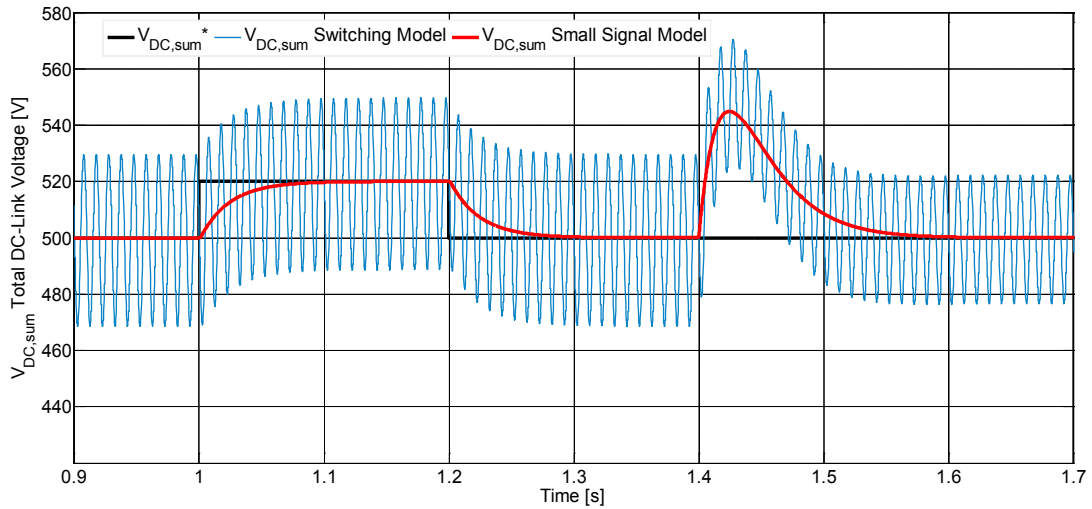


Fig. 1.31: Step response to a small reference and power variations: in case of a  $T_{\text{settling}} = 100\text{ms}$ .

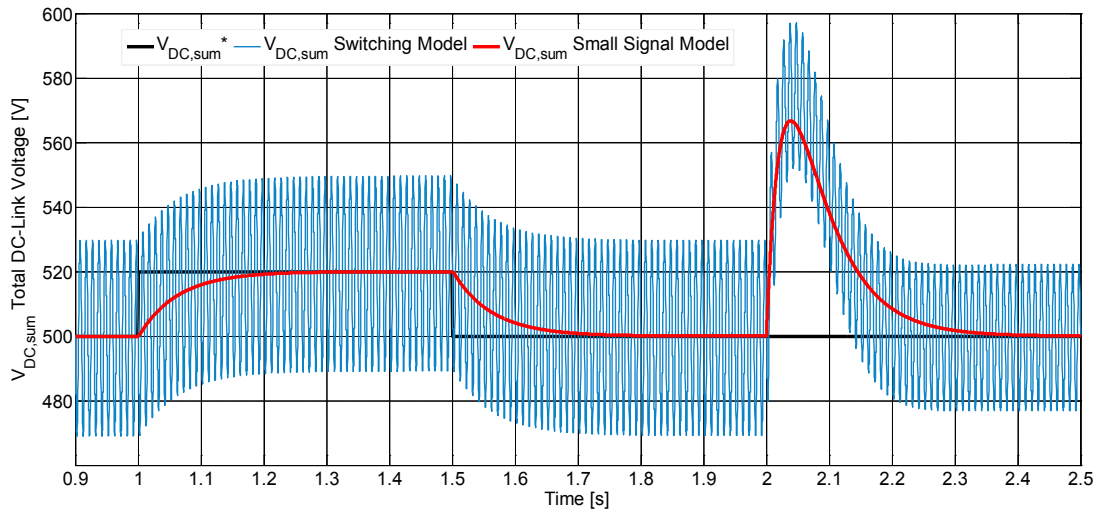


Fig. 1.32: Step response to a small reference and power variations: in case of a  $T_{\text{settling}} = 250\text{ms}$ .

The simulation has been structured in order to validate the model in two cases: 1) variations of  $V_{DC,sum}^*$  reference and 2) variation of the current  $I_o$  (variation of the request DC-Link power). In Fig. 1.31 are depicted the simulation results when the SSBC MMCC is perturbed from a steady-state condition of  $V_{DC,sum}^* = 500\text{V}$  and a

nominal power of  $2kW$ . At  $t_1=1s$ ,  $V_{DC,sum}^*$  changes from  $500V$  to  $520V$  and vice versa at  $t_2=1.2s$ ; at  $t_3=1.4s$  there is a step in the power required by each cell from the value of  $1kW$  to  $750W$ . The simulation results have reported for two different values of settling time,  $T_{settling}(2\%) = 100ms$  (Fig. 1.31) and  $T_{settling}(2\%) = 250ms$  (Fig. 1.32). The results prove that, unless of the second harmonic contribution, the small signal model has the same dynamics of the switching model in terms of tracking and disturbance rejection capability.

## 1.7 DC Multibus Model

In the SSBC MMCC small signal model derived in the previous section there are no reference to a specific active or passive DC stage connected to the each DC-link. The simple case of a balanced DC Multibus obtained with a  $2N+1$  levels SSBC MMCC is reported in Fig. 1.33. In this case the DC-links supplies DC resistive loads.

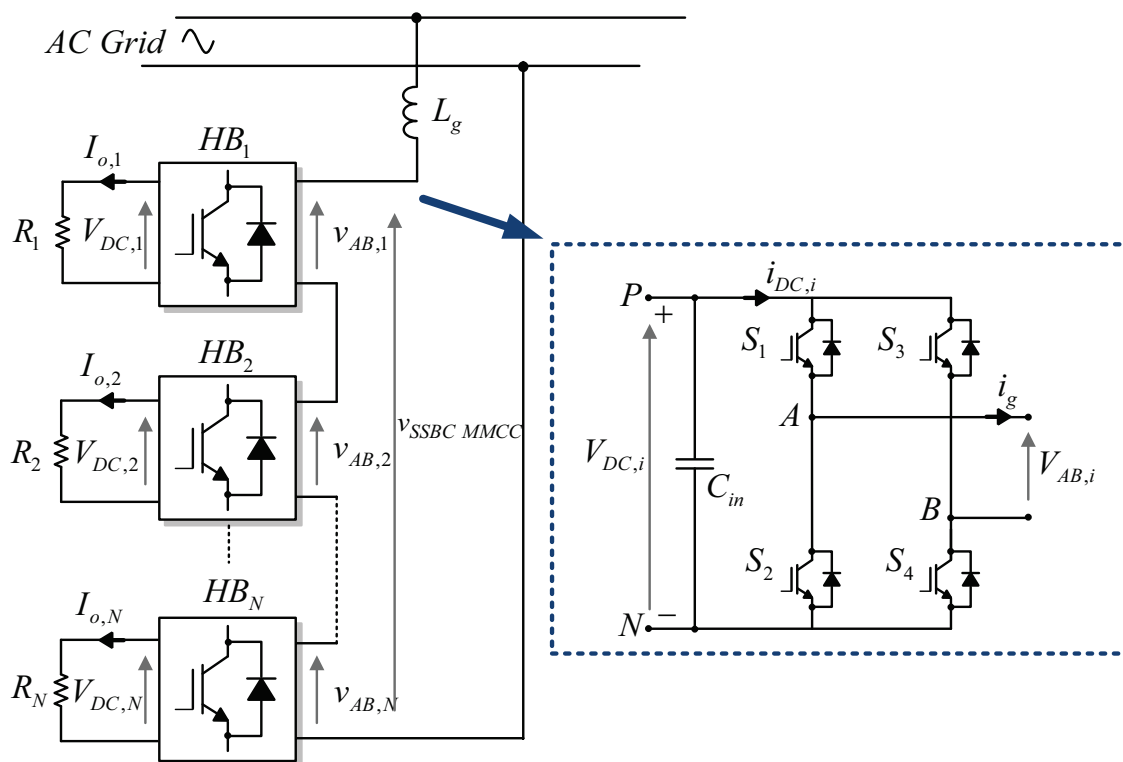


Fig. 1.33: DC Multibus based on a  $2N+1$  level SSBC MMCC converter with resistive loads.

The small signal model of the  $2N+1$  level SSBC MMCC as defined in eq.(1.55) and the model of each resistive linear load  $R_i$  represent the starting point to derive the complete model of the considered DC Multibus:

$$\tilde{V}_{DC,i}(s) = \frac{(\bar{I}_g L_g s + N\bar{V}_{DC,i}\bar{M})}{(2N\bar{V}_{DC,i}C_i s + N\bar{I}_g\bar{M})} \tilde{I}_g(s) - \frac{2N\bar{V}_{DC,i}}{(2N\bar{V}_{DC,i}C_i s + N\bar{I}_g\bar{M})} \tilde{I}_{o,i}(s) \quad (1.75)$$

$$\tilde{I}_{o,i}(s) = \frac{\tilde{V}_{DC,i}(s)}{R_i} \quad \text{with } i = 1, 2, \dots, N \quad (1.76)$$

Substituting eq.(1.76) in eq.(1.75), the following transfer function between the grid current and the  $i$ -th DC-link voltage is obtained:

$$\tilde{V}_{DC,i}(s) = \frac{(\bar{I}_g L_g s + N\bar{V}_{DC,i}\bar{M})}{\left(2N\bar{V}_{DC,i}C_i s + N\bar{I}_g\bar{M} + \frac{2N\bar{V}_{DC,i}}{R_i}\right)} \tilde{I}_g(s) \quad \text{with } i = 1, 2, \dots, N \quad (1.77)$$

The block diagram of the entire DC Multibus is represented in Fig. 1.34, where is depicted the dependence of the total DC-Link voltage  $\tilde{V}_{DC,sum}$  on the grid current  $\tilde{I}_g$ .

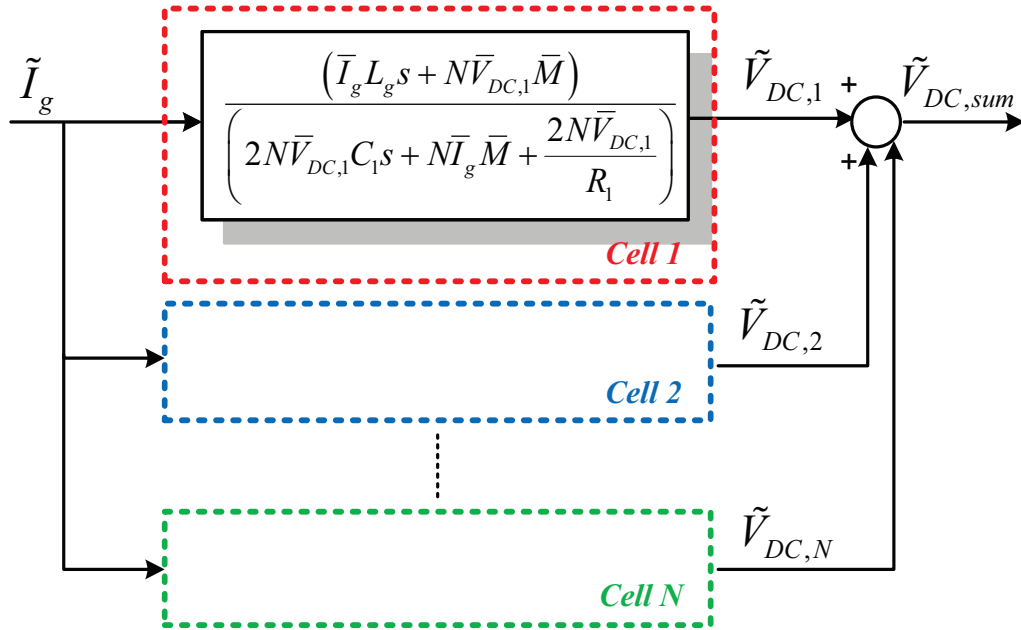


Fig. 1.34: Multi-DC-bus small signal model with a  $2N+1$  levels SSBC MMCC.

To control the total voltage  $\tilde{V}_{DC,sum}$  an equivalent block model is derived. In this equivalent model, for  $i=1,2,\dots,N$ , it results:

$$V_{DC,i} = V_{DC} \quad C_i = C \quad R_i = R \quad i = 1, 2, \dots, N \quad (1.78)$$

Hence the total voltage small signal model equation is:

$$\tilde{V}_{DC,sum}(s) = \frac{(\bar{I}_g L_g s + N\bar{V}_{DC}\bar{M})}{\left(2\bar{V}_{DC}Cs + \bar{I}_g\bar{M} + \frac{2\bar{V}_{DC}}{R}\right)} \tilde{I}_g(s) \quad (1.79)$$

where  $\tilde{V}_{DC,sum}$  is the controlled variable,  $\tilde{I}_g$  is the actuating signal. The internal current loop is designed to achieve a short settling time. If the current control loop is adjusted to be optimally damped a second-order transfer function is derived for the current loop as in eq. (1.39). As a consequence, the voltage open loop function can be defined by:

$$G_{V_{DC}}(s) = \left( \frac{K_p (T_i s + 1)}{T_i s} \right) \left( \frac{\frac{2}{(3T_s)^2}}{s^2 + \frac{2}{3T_s}s + \frac{2}{(3T_s)^2}} \right) \left( \frac{N\bar{V}_{DC}\bar{M}(T_z s + 1)}{\left(\bar{I}_g\bar{M} + \frac{2\bar{V}_{DC}}{R}\right)(T_p s + 1)} \right) \quad (1.80)$$

where  $K_p$  is the proportional gain,  $T_i$  is the integral time constant and

$$T_z = \frac{\bar{I}_g L_g}{N\bar{V}_{DC}\bar{M}} \quad T_p = \frac{2\bar{V}_{DC}C}{\bar{I}_g\bar{M} + \frac{2\bar{V}_{DC}}{R}} \quad (1.81)$$

The tuning procedure follows the same rules shown in the section (1.6.1); the only difference between the model in (1.57) and the model in (1.80) is in the DC-Link plant pole location, which is influenced in (1.80) by the term containing the value of the resistive load,  $R$ .

A 5-levels SSBC MMCC has been assembled based on IGBT Danfoss H- Bridge modules DP25H1200T101616. The system has been controlled with a dSPACE SCALEXIO system. The DC Multibus supplies two perfectly balanced resistive loads. In Tab. 1.4 there are summarized the power stage parameters of the experimental prototype. Based on the same power parameters, a PLECS switching model of the plant

has been developed in MATLAB/Simulink environment with the aim to compare simulation and experimental results in the same operative conditions.

Tab. 1.4: SSBC MMCC Power Stage Parameters

<i>Symbol</i>	<i>Description</i>	<i>Value</i>
$E$ (RMS)	RMS grid Voltage	230 V / 50Hz
$L_g$	AC Inductor filter	3.8 mH
$V_{DC,1} \sim V_{DC,2}$	DC Voltage in each cell	250 V
$C_1 \sim C_2$	DC Capacitor	420 $\mu$ F
$R_1 = R_2$	Passive Loads	62.5 $\Omega$
$f_{sw}$ SSBC MMCC	Switching Frequency	3 kHz

Setting the settling time,  $T_{settling}(2\%) = 100$ ms, the following controllers parameters in Tab. 1.5 have been adopted.

Tab. 1.5: PI Voltage Controller Parameters

<i>Symbol</i>	<i>Description</i>	<i>Value</i>
$\zeta$	Damping coefficient	2.6
$T_{settling}(2\%)$	2% Settling Time	100 ms
$K_p$	Proportional Gain	0.0242
$T_i$	Integral Time Constant	0.0131

In Fig. 1.35 it is shown the step response of the voltage loop.

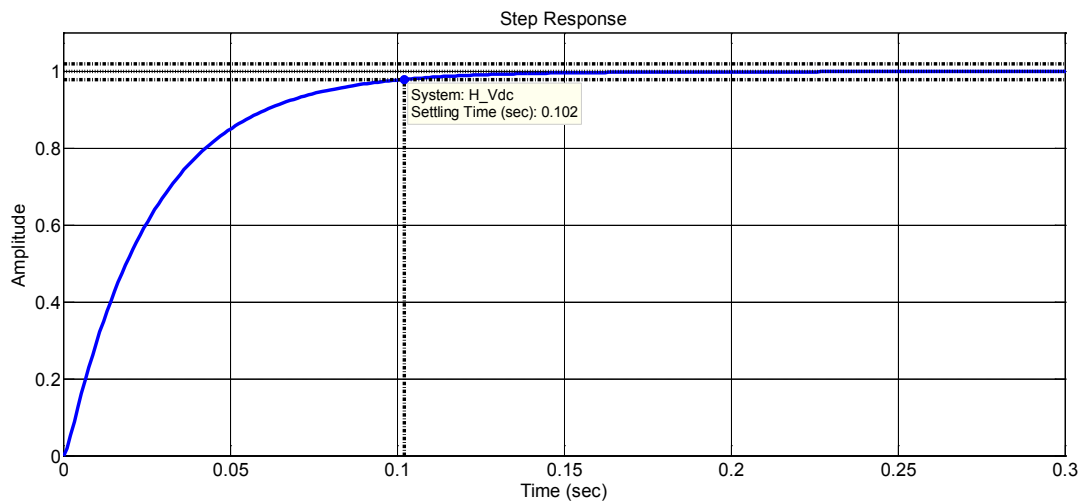


Fig. 1.35: Voltage loop step response of the simulated model with a  $T_{settling}(2\%) = 100$ ms.

In Fig. 1.36 the closed voltage loop Bode diagram is compared with that of the closed current loop. The decoupling condition between the current and voltage dynamics has been verified comparing the bandwidths of the two systems, and ensuring a distance in frequency of a decade between them.

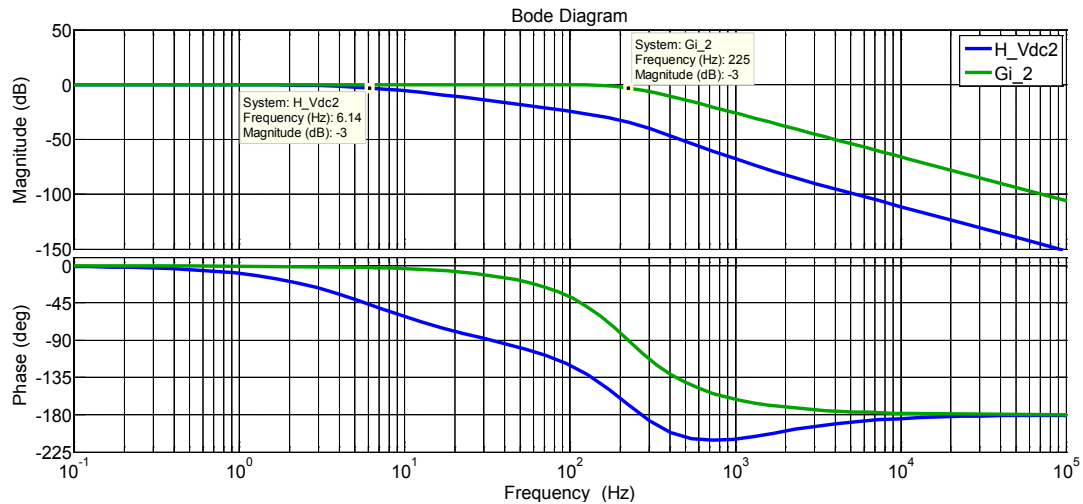


Fig. 1.36: Voltage and current closed loop Bode diagrams of the simulated model.

To validate the accuracy of the proposed model, the step response of the real 5-levels SSBC MMCC has been compared with those of the Average and Small signal model. The test has been performed using the same control and power stage parameters for all the three models. The small signal model has been derived considering  $V_{DC} = 250V$  at steady-state and balanced loads  $R = R_1 = R_2 = 62.5\Omega$ , corresponding to a total power of  $P = 2kW$ .

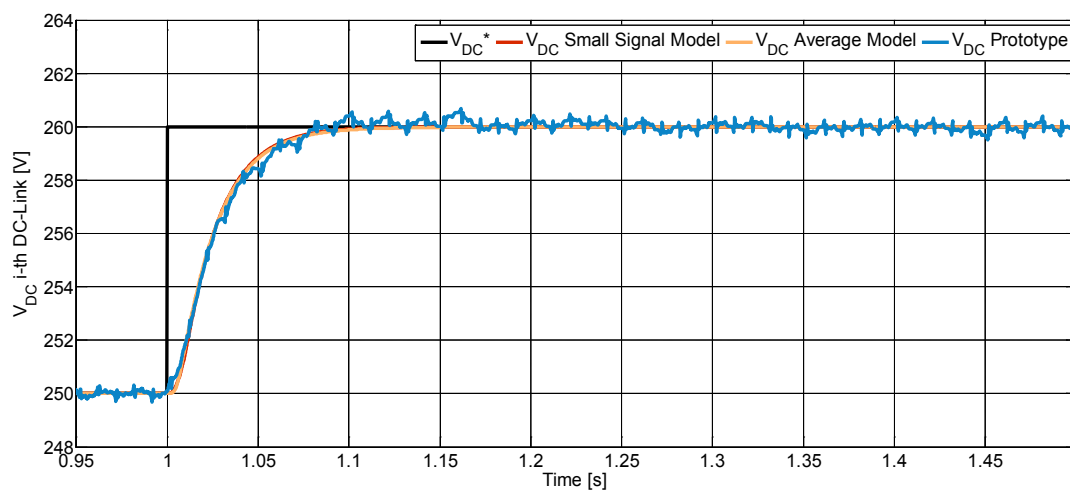


Fig. 1.37: Step response to a small variation of the reference  $\Delta V^* = 10V$ , with a  $T_{\text{settling}} = 100\text{ms}$

The accuracy of the proposed model has been proved in Fig. 1.37 where the step response to a small reference variation, at  $t=1s$   $\Delta V^* = 10V$ , is shown for all the models. As shown in Fig.1.37, the step response of the small signal model matches the measured response of the real system. The measured grid current and voltage waveforms are shown in Fig. 1.38 – 1.39. In particular, in Fig. 1.38 at  $t=1s$  a small voltage reference variation of  $10V$  is applied and it is shown the behavior of the current before, during and after the variation. Fig. 1.39 shows the grid voltage and the grid current in steady-state condition. It is possible to observe that the SSBC MMCC is operating as a rectifier since the grid voltage and the grid current are  $180^\circ$  phase-shifted.

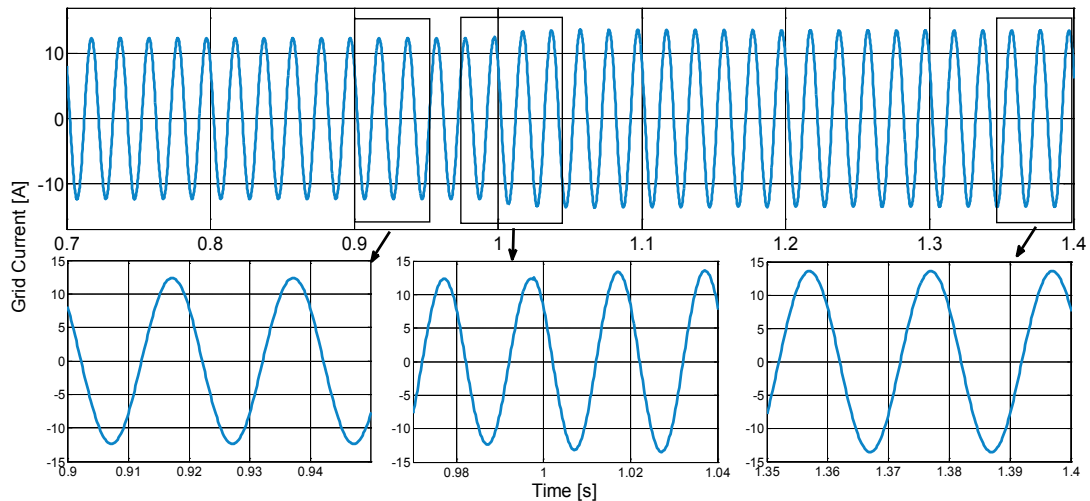


Fig. 1.38: Grid current in case of a small variation of the reference  $\Delta V^* = 10V$ .

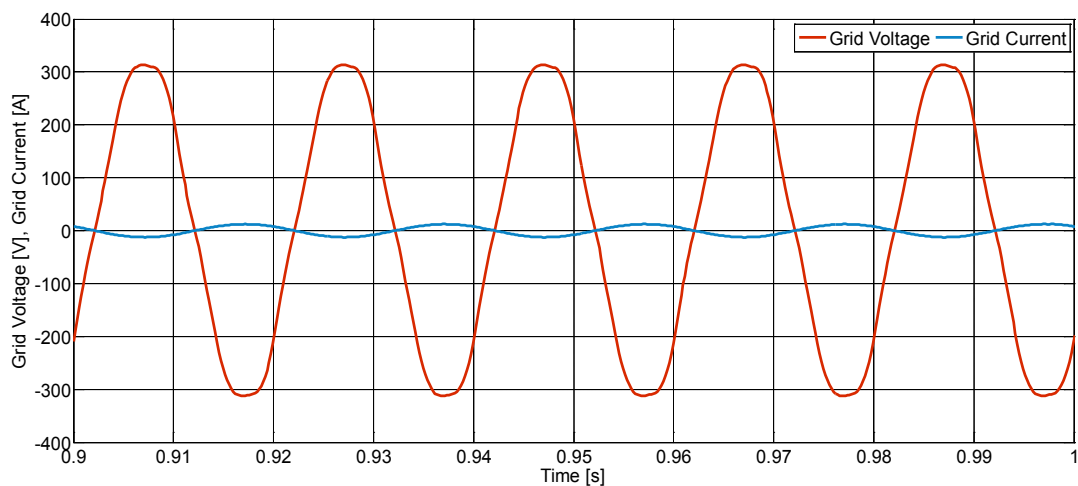


Fig. 1.39: Grid voltage and current in steady-state operation and nominal power of  $P_n = 2kW$ .

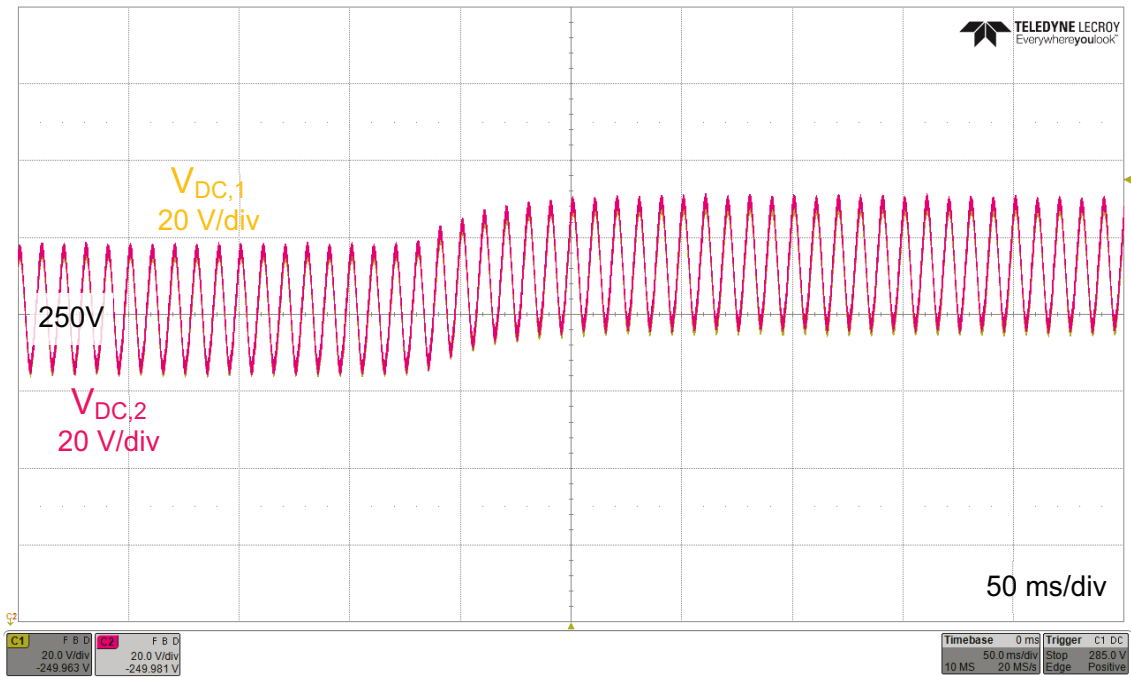


Fig. 1.40: Prototype –  $V_{DC,1}$  and  $V_{DC,2}$  step response to  $\Delta V^* = 10V$ , with a  $T_{\text{setting}} = 100\text{ms}$ .

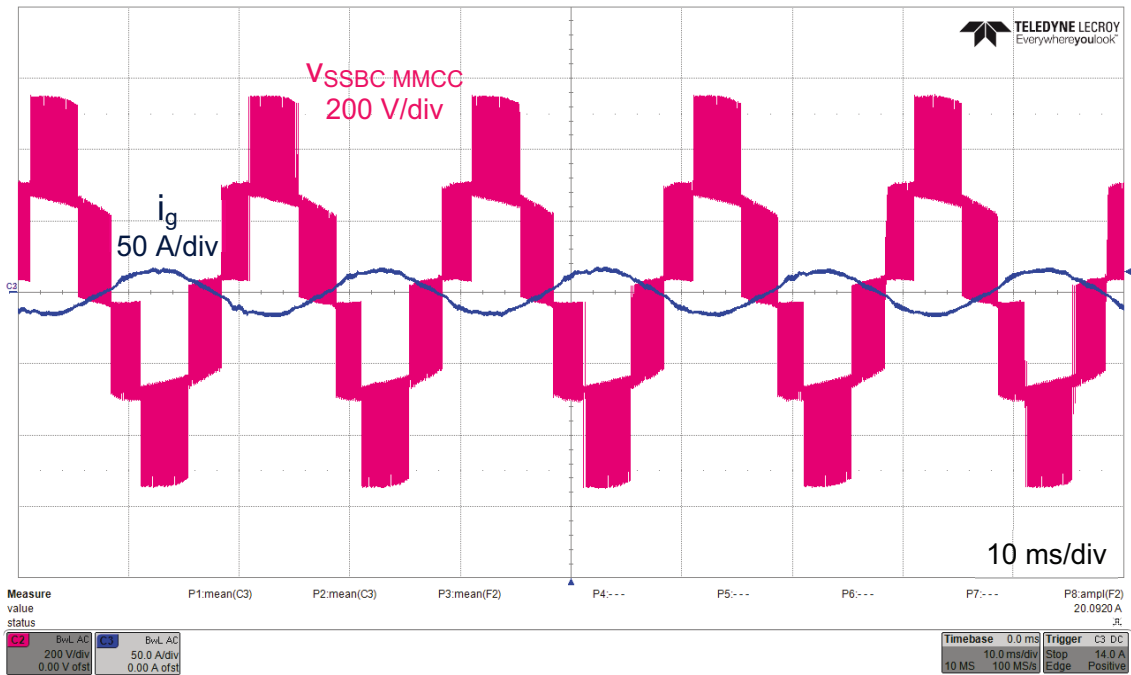


Fig. 1.41: Prototype – Grid Current and 5-levels SSBC MMCC voltage in steady-state operation  $P_n = 2\text{kW}$ .

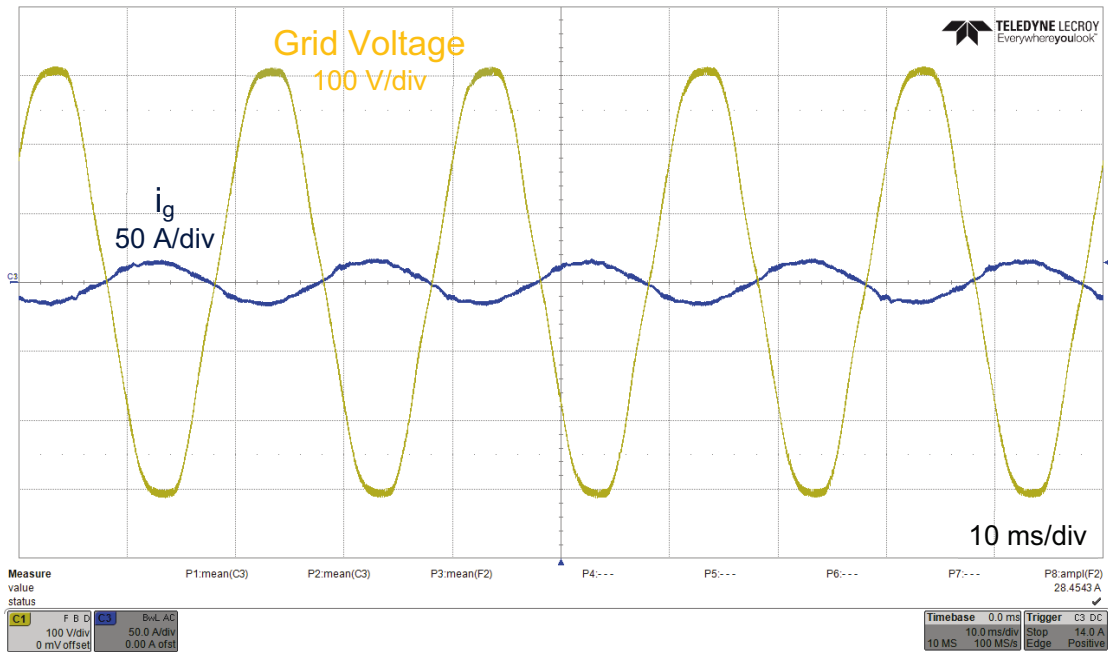


Fig. 1.42: Prototype – Grid Current and grid voltage in steady-state operation  $P_n = 2\text{ kW}$ .

Setting the settling time,  $T_{\text{settling}}(2\%) = 250\text{ ms}$ , the following controllers parameters in Tab. 1.6 have been adopted.

Tab. 1.6: PI Voltage Controller Parameters.

<i>Symbol</i>	<i>Description</i>	<i>Value</i>
$\zeta$	<i>Damping coefficient</i>	4
$T_{\text{settling}}(2\%)$	<i>2% Settling Time</i>	250 ms
$K_p$	<i>Proportional Gain</i>	0.0101
$T_i$	<i>Integral Time Constant</i>	0.0131

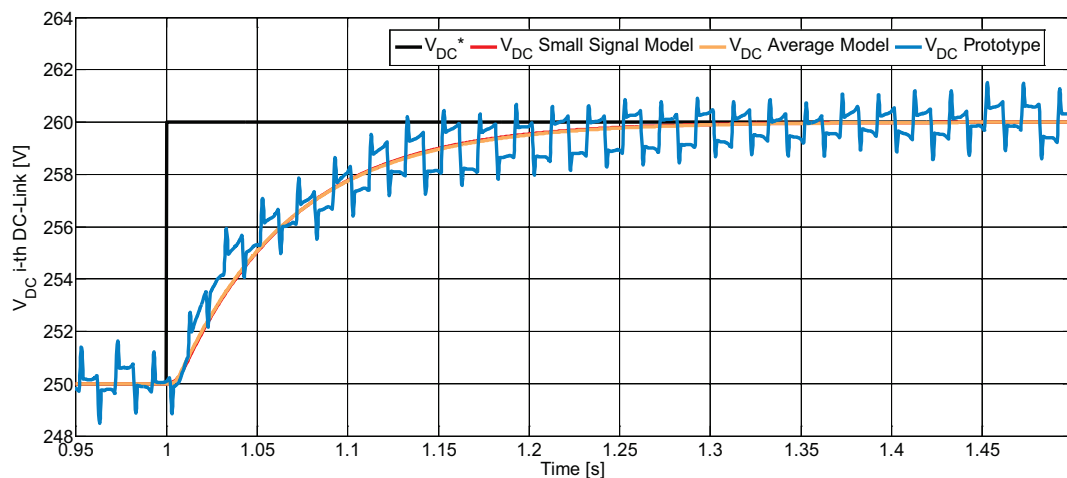


Fig. 1.43: Step response to a small variation of the reference  $\Delta V^* = 10\text{ V}$ , with a  $T_{\text{settling}} = 250\text{ ms}$

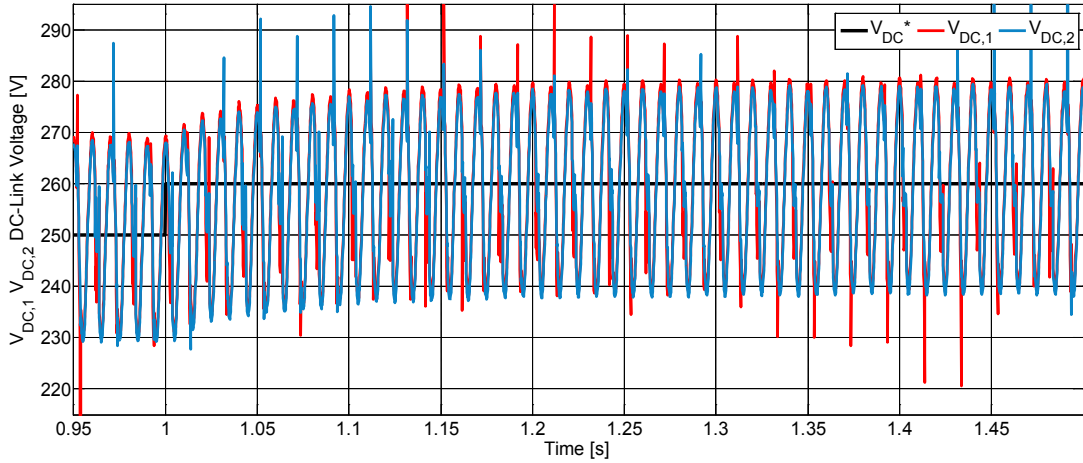


Fig.1.44:  $V_{DC,1}$  and  $V_{DC,2}$  step response to  $\Delta V^* = 10V$ , with a  $T_{\text{setting}} = 250\text{ms}$ .

## 1.8 $V_{DC}$ Voltage Balance Control

In order to ensure proper operation of the SSBC MMCC, the balance of each DC-Link voltage  $V_{DC,i}$  must be ensured. A controller is employed to fulfill this goal as shown in Fig. 1.45, where  $v_{SSBC\_MMCC}^*$  is the average SSBC MMCC voltage and it is required by the overall power stage in order to delete the current error,  $V_{DC,i}$  is the DC voltage measured at the  $i$ -th DC-Link,  $i_g^*$  is the current loop reference,  $m_{BAL,i}$  represents the contribution to the modulating signal of the  $i$ -th H-Bridge in order to balance the  $i$ -th  $V_{DC}$ . The modulating signal for the  $i$ -th H-Bridge is defined as:

$$m_i = m \left[ 1 - \text{sign}(i_g^*) K_{pBAL,i} \left( 1 + \frac{1}{T_{BAL,i} s} \right) \left( \frac{1}{N} \sum_{i=1}^N V_{DC,i} - V_{DC,i} \right) \right] \quad (1.82)$$

where  $K_{pBAL,i}$  is the proportional gain related to the  $i$ -th cell and varying the proportional gain it is possible to regulate the control action;  $T_{BAL,i}$  is the correspondent  $i$ -th integral time constant needed to guarantee a zero error steady-state. In the considered case study the same control parameters are used for all the buses. Differently from the modulation signal  $m$ , the output of the voltage balance controller is not a sinusoidal signal. Hence to adjust the amplitude of the modulating signal, the output of the controller is multiplied by  $m$  and by the sign of the grid current, resulting in  $m_{BAL,i}$ ; finally  $m_i$  is obtained subtracting  $m_{BAL,i}$  to  $m$ . The proposed voltage balance control has been applied to a multi-DC-bus provided by a 5-levels SSBC MMCC in grid connected operation.

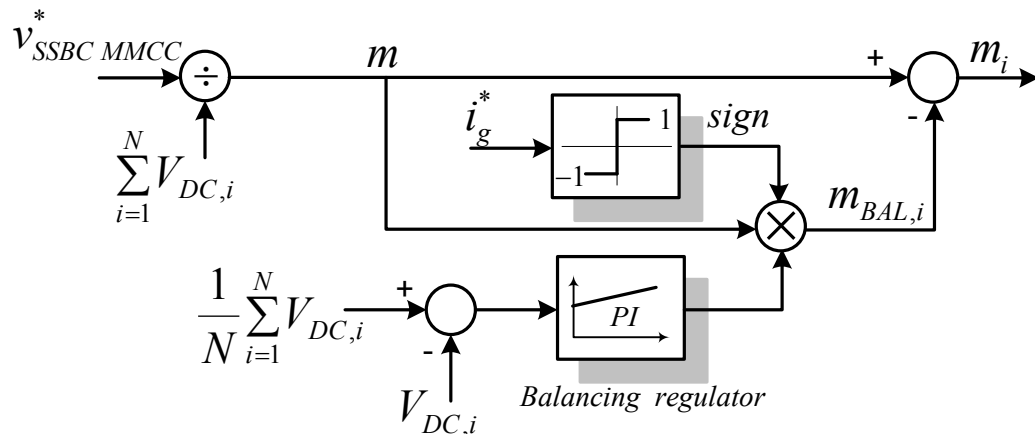


Fig. 1.45: Voltage balance control loop of the i-th DC-Link.

In the following, the simulation results are compared to the experimental results. The experimental tests have been performed on a 5-levels SSBC MMCC which consists of two series connected Danfoss VLT 7.6kVA H-Bridges. The power stage parameters are reported in Tab. 1.7.

Tab.1.7: Power Stage Parameters of the 5-levels SSBC MMCC based on two Danfoss VLT 7.6kVA. converters

<b><i>Symbol</i></b>	<b><i>Description</i></b>	<b><i>Value</i></b>
$E$ (RMS)	RMS grid Voltage	220 V / 50Hz
$L_g$	AC Inductor filter	5 mH
$V_{DC,1} \sim V_{DC,2}$	DC Voltage in each cell	200 V
$C_1 \sim C_2$	DC Capacitor	320 $\mu$ F
$R_1 = R_2$	Passive Loads	114 $\Omega$
$f_{sw}$ SSBC MMCC	SSBC Switching Frequency	10 kHz

In this case the control system has been implemented with a different dSPACE platform respect to the previous cases. The DS1006 dSPACE Board is based on a quad-core AMD Opteron™ x86 processor with 2.8 GHz clock frequency required for large-scale real-time applications. The processor board works in parallel with a DS5203 FPGA Board, it features the programmable Xilinx Virtex®-5 FPGA with ISE support or Vivado® support. The DS5203 FPGA Boards operate at 100MHz and are used for relieving the processor board of tasks such as signal pre-processing.

Starting from a steady-state condition where the load in each DC-Link is equal to  $R_1=R_2=114\Omega$  and the power delivered by each H-Bridge is  $P_1=P_2=350W$ , at time  $t=1s$  a load variation is applied to the first DC-Link and  $R_1$  changes from  $114\Omega$  to  $85\Omega$ . This load variation corresponds to a change of the 30% in the power delivered by the first bus, as a consequence  $P_1$  varies from  $350W$  to  $470W$  and  $I_{DC,1}$  from  $1.75A$  to  $2.35A$ ; while  $P_2=350W$  and  $I_{DC,2}=1.75A$ . The voltage references on each DC-Link remain unchanged and equal to  $200V$ .

Fig. 1.46 shows the DC-Link voltage when occurs the first load variation of 30%; the balance control acts modifying the modulating signals in input to the PWM modulators, and after a small transient of  $500ms$ , the new steady-state condition is reached with all the DC-Link voltages balanced around the value of  $200V$ . Around the average value of  $200V$  it can be observed the typical second harmonic component whose depends on the power delivered by the correspondent H-Bridge. Since  $P_1 > P_2$ , the ripple in  $V_{DC,1}$  is bigger than in  $V_{DC,2}$ .

At  $t=1.8s$  another load variation is applied to the first DC-Link and  $R_1$  varies from  $85\Omega$  to  $50\Omega$ . This load variation corresponds to a 50% displacement in the power delivered by the two buses:  $P_1$  varies from  $470W$  to  $800W$  and consequently  $I_{DC,1}$  from  $2.35A$  to  $4A$ ; while  $P_2=350W$  and  $I_{DC,2}=1.75A$ . The balance control acts modifying the modulating signals in input to the PWM modulators, as shown in Fig. 1.46.

Differently from the previous load step variation, the DC-Link voltages  $V_{DC,1}$  and  $V_{DC,2}$  appear distorted due the modulating signal saturation. It implies that an imbalance up to 50% can be supported by the voltage balance control while over 50% no control action can be achieved. The last operating condition represents the control limit and must be avoided, reconfiguring the layout of the loads in the multi-DC bus.

Fig. 1.47 shows the DC currents  $I_{DC,1}$  and  $I_{DC,2}$  in the same load variations.

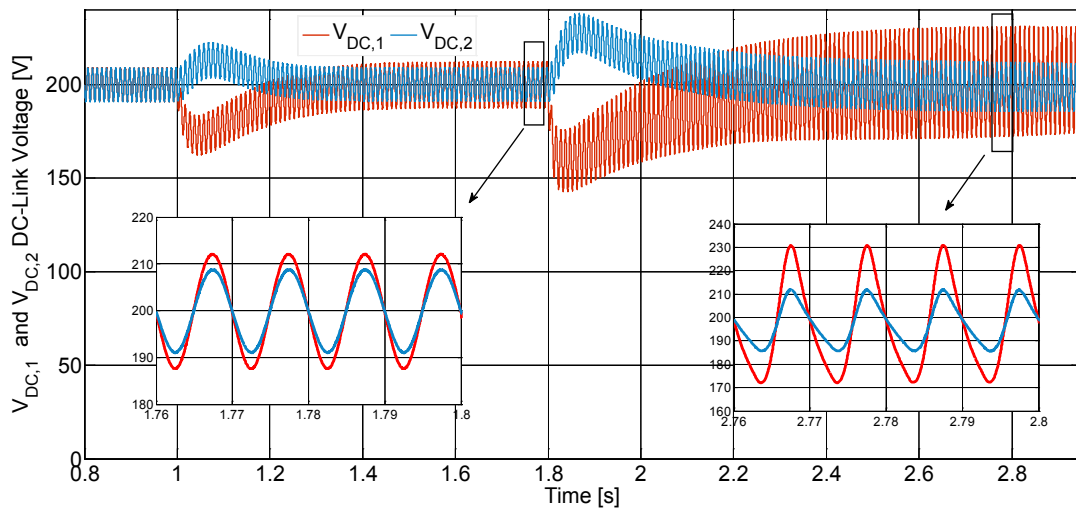


Fig. 1.46: Simulation - DC-link voltages in case of load variations: 30% at  $t=1$ s and 50% at  $t=1.8$ s.

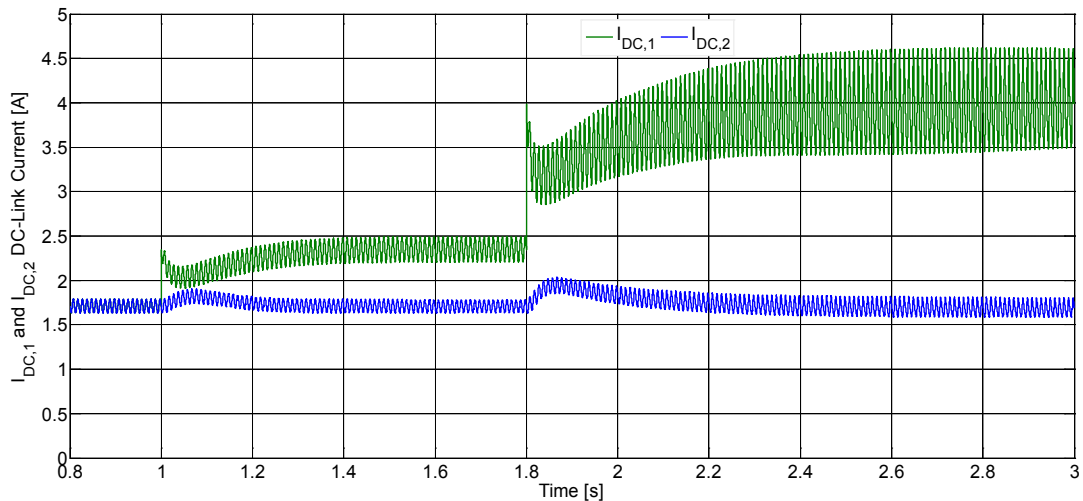


Fig. 1.47: MATLAB - DC-link currents in case of load variations: 30% at  $t=1$ s and 50% at  $t=1.8$ s.

The simulation results have been compared to the experimental results. The tests have been performed with the same power step variations: power imbalance of 30% in the first step and more than 50% in the second step.

Fig. 1.48 shows the prototype DC-Link voltages ( $V_{DC,1}$  and  $V_{DC,2}$ ) and currents ( $I_{DC,1}$  and  $I_{DC,2}$ ) in the two successive power variations. The experimental results confirm the simulations in terms of transient behavior and power imbalance limit.

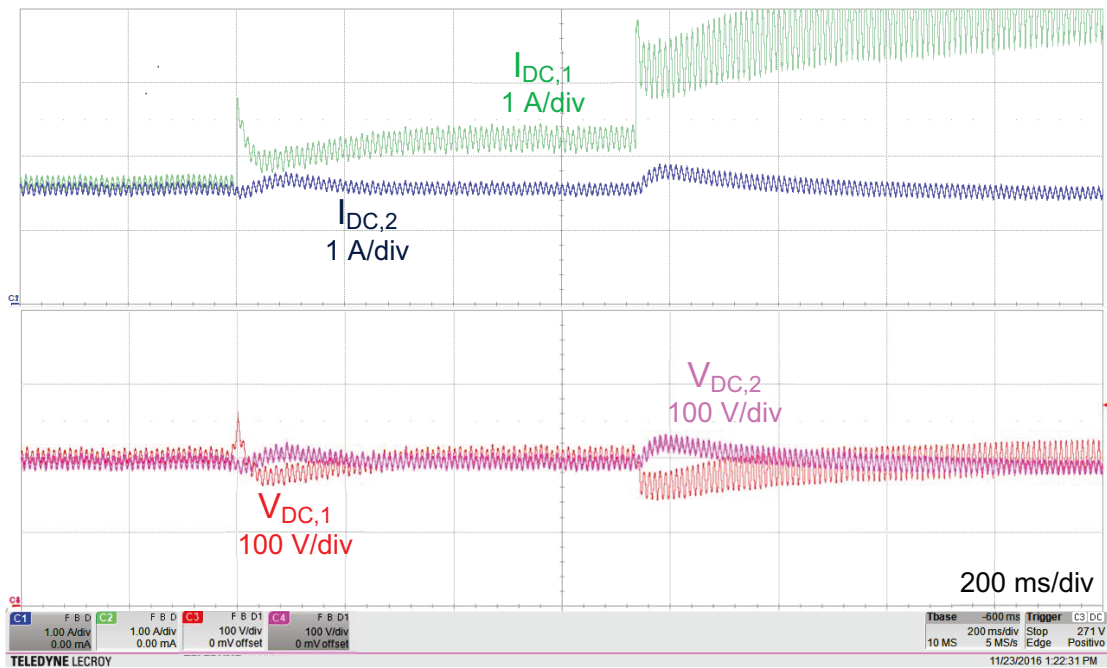


Fig. 1.48: Experimental results - DC-link currents and voltages with two successive load variations: 30% and 50%.

The operating has been verified comparing the modulating signal in input to each H-Bridge PWM modulator in case of different power imbalance conditions. In Fig. 1.49, the modulating signals,  $m_1$  and  $m_2$ , of each H-Bridge are perfectly overlapping because the two DC-Links are delivering the same power:  $P_1 = P_2$ .

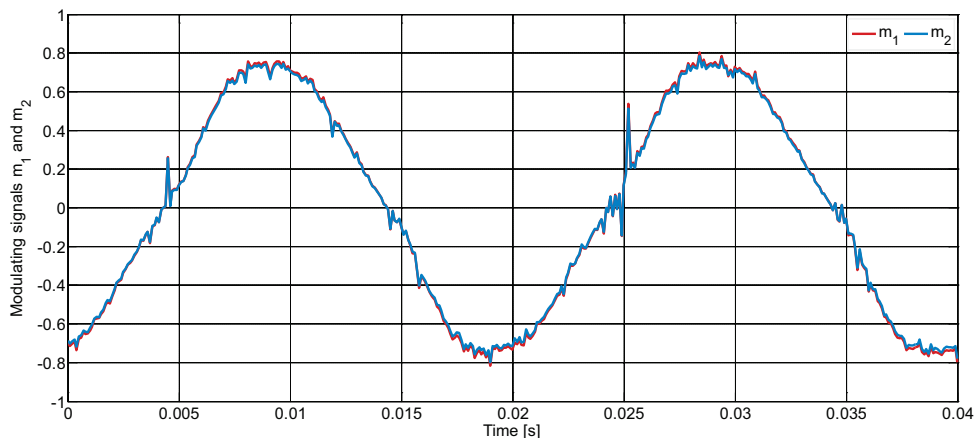


Fig. 1.49: Modulating signals,  $m_1$  and  $m_2$ , when each cell delivers the same power:  $P_1 = P_2$ .

Fig. 1.50 shows the modulating signals when a 30% power imbalance occurs:  $P_1 \neq P_2$ . Finally, Fig. 1.51 shows the modulating signals when a power imbalance over 50%

occurs: in this case the corrective action imposed by the voltage balance controller saturates the modulating signal  $m_1$ . This condition represents the controllability limit and it must be avoided in order to guarantee the stability of the entire system.

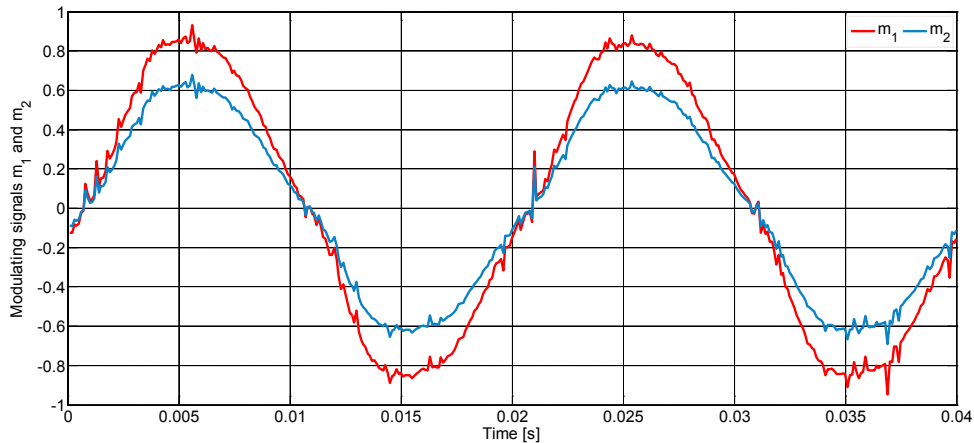


Fig. 1.50: Modulating signals,  $m_1$  and  $m_2$ , when each cell delivers a different power:  $P_1 \neq P_2$  ( $\Delta P=30\%$ ).

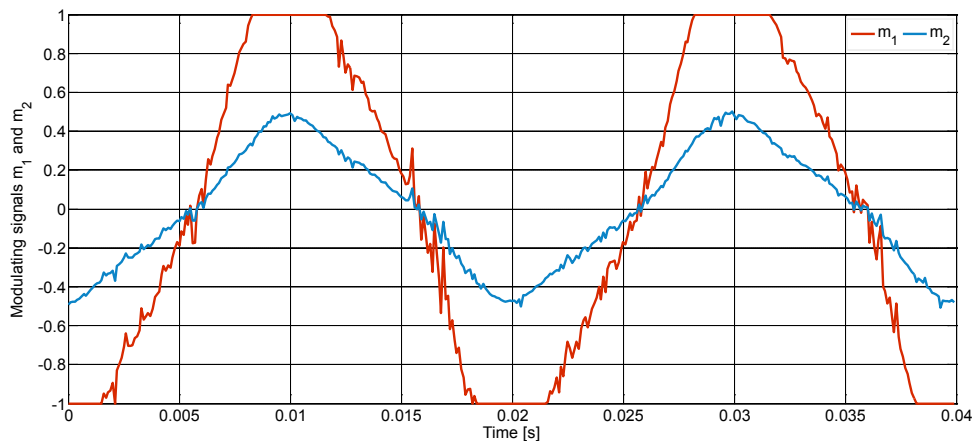


Fig. 1.51: Modulating signals,  $m_1$  and  $m_2$ , when each cell delivers a different power:  $P_1 \neq P_2$  ( $\Delta P=50\%$ ).

## 1.9 SSBC MMCC Feedback Linearization Control

Feedback linearization (FL) is an approach to nonlinear control design which has attracted a great deal of research interest in recent years. The central idea of the approach is to algebraically transform a nonlinear system dynamics into a linear one, so that linear control techniques can be applied. The obtained linear system, can be used for the design of robust or adaptive controllers. Feedback linearization is achieved by

the exact state transformation and feedback, rather than by linear approximations of the dynamics [20].

In its simplest form, the idea of cancelling the nonlinearities and imposing a desired linear dynamics, can be applied to a class of nonlinear systems described by the so-called *companion form*, or *controllability canonical form*. A system is said to be in companion form if its dynamics is represented by:

$$\dot{x}^{(n)} = f(\mathbf{x}) + b(\mathbf{x})u \quad (1.83)$$

where  $u$  is the scalar control input,  $x$  is the scalar output of interest,  $\mathbf{x} = [x, \dot{x}, \dots, x^{(n-1)}]^T$  is the state vector, and  $f(\mathbf{x})$  and  $b(\mathbf{x})$  are nonlinear functions of the state. Although derivatives of  $x$  appear in this equation, no derivative of the input  $u$  is present. Assuming  $b$  to be invertible and non-zero and using the control input, it results:

$$u = b(\mathbf{x})^{-1} [v - f(\mathbf{x})] \quad (1.84)$$

the nonlinearities can be cancelled and a new simple input-output relation (multiple-integrator form) is obtained:

$$\dot{x}^{(n)} = v \quad (1.85)$$

where  $v$  represents the new scalar control input chosen so that the linear equivalent system satisfies the required specifications. If a tracking control problem is considered for the output variable  $y$ :

$$y = h(\mathbf{x}) \quad (1.86)$$

a difficulty with this model is that the output  $y$  is only indirectly related to the input  $u$  through the state variable  $\mathbf{x}$  and the nonlinear state equation (1.83). The difficulty of the tracking control design can be reduced if it can be *found a direct and simple relation between the system output  $y$  and the control input  $u$* ; this idea constitutes the so-called *Input-Output* linearization approach to nonlinear control design [20].

This approach has been used for the control of the output voltage in a SSBC MMCC when the nonlinearity of the plant is taken in account in the model. Neglecting the

power losses, the instantaneous input-output power balance for a  $2N+1$  level SSBC MMCC grid converter is described by:

$$\frac{1}{2}(E_d I_{g,d} + E_q I_{g,q}) = \sum_{i=1}^N \left( V_{DC,i} I_{o,i} + C_i \frac{dV_{DC,i}}{dt} V_{DC,i} \right) \quad (1.87)$$

considering a synchronous (with the grid voltage vector) rotating direct-quadrature ( $d-q$ ) frame, where  $E_{d,q}$  are the  $d-q$  components of the grid voltage,  $I_{g,d}$  and  $I_{g,q}$  are the  $d-q$  components of the grid current and  $I_{o,i}$  is the DC current required by the  $i$ -th output stage. If the output stage in each DC-link is a pure DC resistive load  $R_i$ , the power balance equation (1.87) becomes:

$$\frac{1}{2}(E_d I_{g,d} + E_q I_{g,q}) = V_{DC,i} \sum_{i=1}^N \left( \frac{V_{DC,i}}{R_i} + C_i \frac{dV_{DC,i}}{dt} \right) \quad (1.88)$$

Considering a perfect power distributions in each cell,  $R=R_i$ , and supposing that each DC-link stage is characterized by the same capacitor value,  $C=C_i$ , eq. (1.88) can be rewritten as:

$$\frac{1}{2}(E_d I_{g,d} + E_q I_{g,q}) = \frac{NV_{DC}}{N} \left( \frac{NV_{DC}}{R} + C \frac{d(NV_{DC})}{dt} \right) \quad (1.89)$$

If a VOC is applied in the synchronization then  $E_q=0$  and considering to control the total voltage,  $V_{DC,sum}$ , the following nonlinear model is derived:

$$\frac{1}{2} E_d I_{g,d} = V_{DC,sum} \left( \frac{V_{DC,sum}}{NR} + \frac{C}{N} \frac{dV_{DC,sum}}{dt} \right) \quad (1.90)$$

From eq. (1.90), the companion form of the nonlinear plant in the state-space can be written as:

$$\begin{cases} \dot{V}_{DC,sum} = f(V_{DC,sum}) + b(V_{DC,sum}) I_{g,d} \\ y = V_{DC,sum} \end{cases} \quad (1.91)$$

where the scalar control input is the grid current  $I_{g,d}$ , the state variable is  $V_{DC,sum}$  which is equal to the output variable. Hence the nonlinear function  $b(V_{DC,sum})$  can be described by:

$$\begin{cases} \dot{V}_{DC,sum} = -\frac{1}{RC}V_{DC,sum} + \frac{NE_d}{2C} \frac{1}{V_{DC,sum}} I_{g,d} \\ y = V_{DC,sum} \end{cases} \quad (1.92)$$

If the grid voltage  $E_d$  is considered constant and the total voltage  $V_{DC,sum}$  is measurable, the input-output linearization law is the following:

$$I_{g,d} = \frac{2V_{DC,sum}}{E_d} v \quad (1.93)$$

which results in a linear first order system:

$$\begin{cases} \dot{V}_{DC,sum} = -\frac{1}{RC}V_{DC,sum} + \frac{N}{C}v \\ y = V_{DC,sum} \end{cases} \quad (1.94)$$

Eq.(1.94) can be expressed in the Laplace domain as:

$$V_{DC,sum} = \frac{\frac{N}{Cs}}{1 + \frac{1}{RCs}} v = \frac{N}{C \left( s + \frac{1}{RC} \right)} v \quad (1.95)$$

A PI controller is employed in the outer loop to eliminate the tracking error in presence of parameters variations; this is an ad-hoc approach to the robustness problem [21].

The DC voltage control scheme based on the FL is shown in Fig. 1.52, where the inner current loop, designed to achieve short settling times, is taken into account just by means of a delay transfer function and  $K_p$  and  $T_i$  are respectively the proportional gain and the integral time constant of the voltage regulator. Hence the output of the voltage controller can be defined as:

$$v = K_p \left( 1 + \frac{1}{T_i s} \right) (V_{DC,sum}^* - V_{DC,sum}) \quad (1.96)$$

The open loop transfer function:

$$V_{DC,sum} = \frac{K_p}{s} \left( s + \frac{1}{T_i} \right) \frac{N}{C \left( s + \frac{1}{RC} \right)} (V_{DC,sum}^* - V_{DC,sum}) \quad (1.97)$$

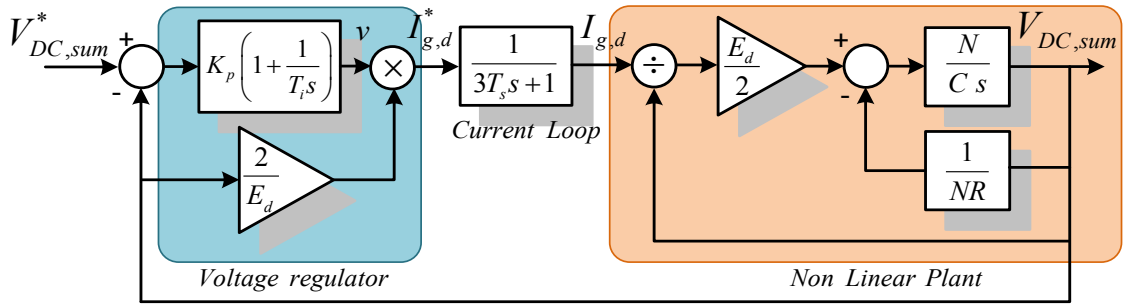


Fig. 1.52: DC voltage control of the grid-connected converter based on the FL.

A simple tuning procedure can be adopted. The parameters of the DC voltage control loop ( $K_p$  and  $T_i$ ) are tuned in order to achieve an asymptotically stable first order system and a dynamics at least ten times slower than the inner current loop. Designing the integral time constant in order to delete the dynamic of the slower pole,

$$T_i = RC \quad (1.98)$$

the output variable is in a linear single-integrator relation with the tracking error:

$$V_{DC,sum} = K_p \frac{N}{C s} (V_{DC,sum}^* - V_{DC,sum}) \quad (1.99)$$

This leads to a first order closed-loop transfer function:

$$V_{DC,sum}^* = \frac{1}{\left( \frac{C}{NK_p} s + 1 \right)} V_{DC,sum} = \frac{1}{\left( \frac{T_{setling}}{3} s + 1 \right)} V_{DC,sum} \quad (1.100)$$

Eq. (1.100) underline the relation between the settling time,  $T_{setling}$ , and the value of  $K_p$  in the pole allocation. The relation is expressed as follows:

$$K_p = \frac{3C}{T_{settling} N} \quad (1.101)$$

In order to validate the SSBC MMCC feedback linearization control, the simulation results obtained through the PLECS switching model are compared with the results obtained in case of the non linear plant (with reference to the Fig. 1.52). The power stage parameters used in both the compared models are summarized in Tab. 1.4. Assuming a settling time  $T_{settling}(5\%) = 100ms$ , the tuning parameters of the DC voltage control loop are summarized in Tab. 1.8.

Tab. 1.8: FL Voltage Controller Parameters

<i>Symbol</i>	<i>Description</i>	<i>Value</i>
$T_{settling}(5\%)$	<i>5% Settling Time</i>	<i>100 ms</i>
$K_p$	<i>Proportional Gain</i>	<i>0.0063</i>
$T_i$	<i>Integral Time Constant</i>	<i>0.0263</i>

The simulation has been structured in order to validate the tracking capability of the control and the linearization of the nonlinear plant. The 5-level SSBC MMCC with a rated power of  $2kW$  is perturbed at  $t_1$  and  $t_2$  starting from a steady-state condition of  $V_{DC,sum}^* = 500V$ .

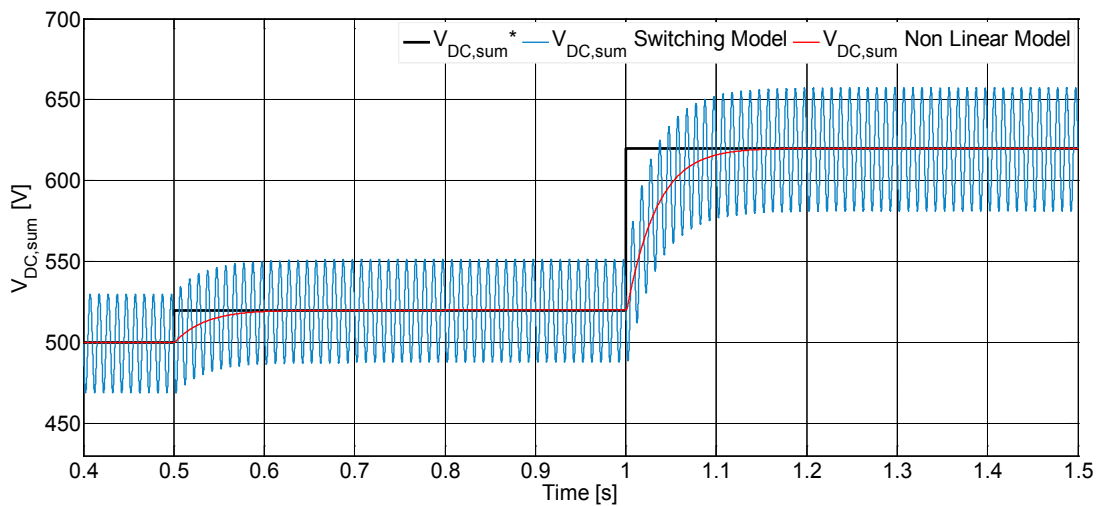


Fig. 1.53: DC voltage control of the grid-connected SSBC MMCC based on the FL.

At  $t_1=0.5s$ ,  $V_{DC,sum}^*$  changes from  $500V$  to  $520V$  and at  $t_2=1s$   $V_{DC,sum}^*$  changes from  $520V$  to  $620V$ . The results, shown in Fig. 1.53, prove that, despite the second harmonic

contribution, the nonlinear model has the same dynamics of the switching model and the linearization is verified starting from different initial conditions.

The FL control has been compared to the PI control in terms of tracking and disturbance rejection capability, when the non linear plant of Fig. 1.52 is taken into account and different reference variations and load variations are applied to the system. The comparative simulation in Fig. 1.54 underline that the two control technique have a similar responses to step variations, but the PI controller is faster than FL in disturbance rejection capability, when a load variation occurs. Thus it means that, when the dynamic of the control is chosen properly, in terms of overshoot and time settling, the linear PI control and the FL control can be used indistinctly. This is underlined in [22] where the tuning procedure with the method of ‘symmetrical optimum’ in the DC voltage control loop fails in case of high step variations in the voltage reference.

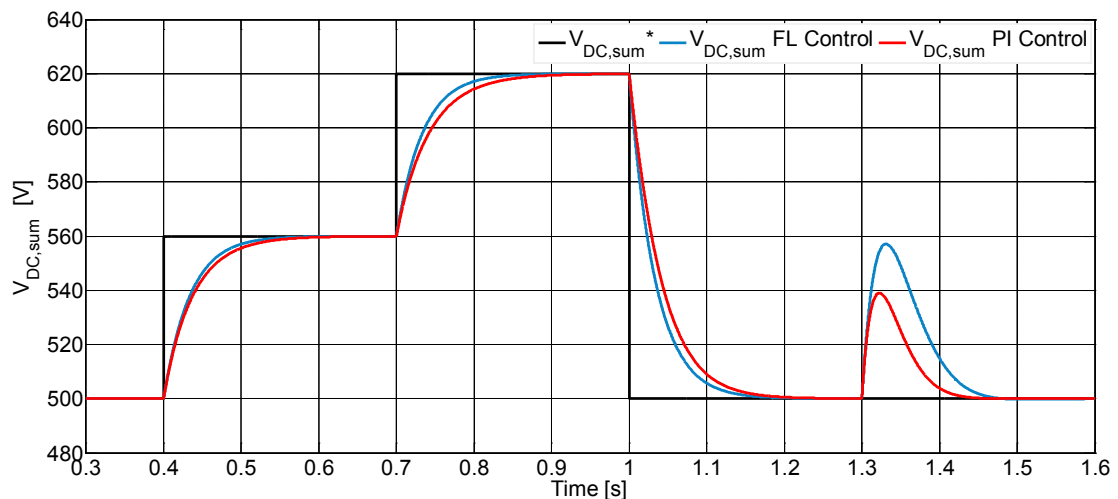


Fig. 1.54: Comparison of the DC voltage control of the SSBC MMCC based on the FL and PI controller.

The FL and the PI control have been compared also in term of power quality of the injected grid current, when the 5-level SSBC MMCC delivers a rated power of  $2kW$ . The grid current THD(%) has been calculated in both the cases using the PLECS switching model, resulting in a  $THD_{PI}(\%) = 4.55\%$  and in a  $THD_{FL}(\%) = 3.58\%$ . This result can be easily justified comparing the FFT of the grid current  $i_g$  in both the cases as shown in Fig. 1.55 and Fig. 1.56. Comparing them, it can be shown that the third harmonic component at 150Hz in the FL control is three times smaller than in the PI

control. This is the result of a different proportional gain value  $K_p$  and hence a different attenuation of the second harmonic component at 100Hz presents in the DC-link voltage.

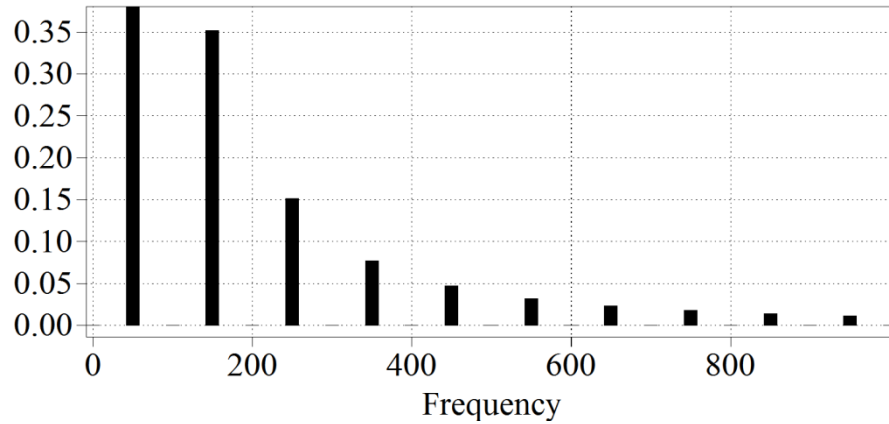


Fig. 1.55: FFT of the grid current  $i_g$  when the DC voltage control of the SSBC MMCC is based on the PI.

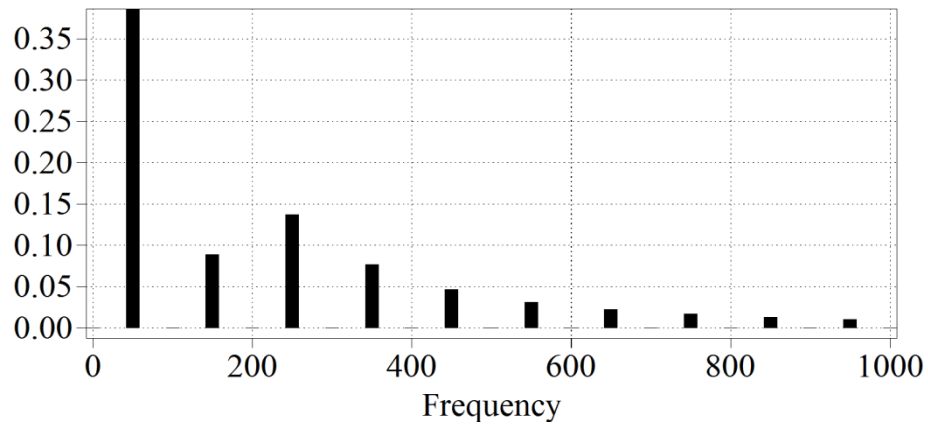


Fig. 1.56: FFT of the grid current  $i_g$  when the DC voltage control of the SSBC MMCC is based on the FL.

## 1.10 SSBC MMCC PWM Modulator

The PWM modulation of the SSBC MMCC is based on the phase-shift between the carriers of two adjacent cells:

$$\Phi_{CR} = \frac{360^\circ}{2N} \quad (1.102)$$

where  $N$  represents the number of cells. This type of modulation is applied for multilevel converters and it allows increasing the output voltage range and reducing the

harmonics in the resulting waveform. The carrier relative to each H-Bridge is out of phase with respect to the carrier of the adjacent cells by an angle equal to  $\Phi_{CR}$ . In case of 5-level SSBC MMCC the carrier relative to each H-Bridges is  $90^\circ$  phase-shifted.

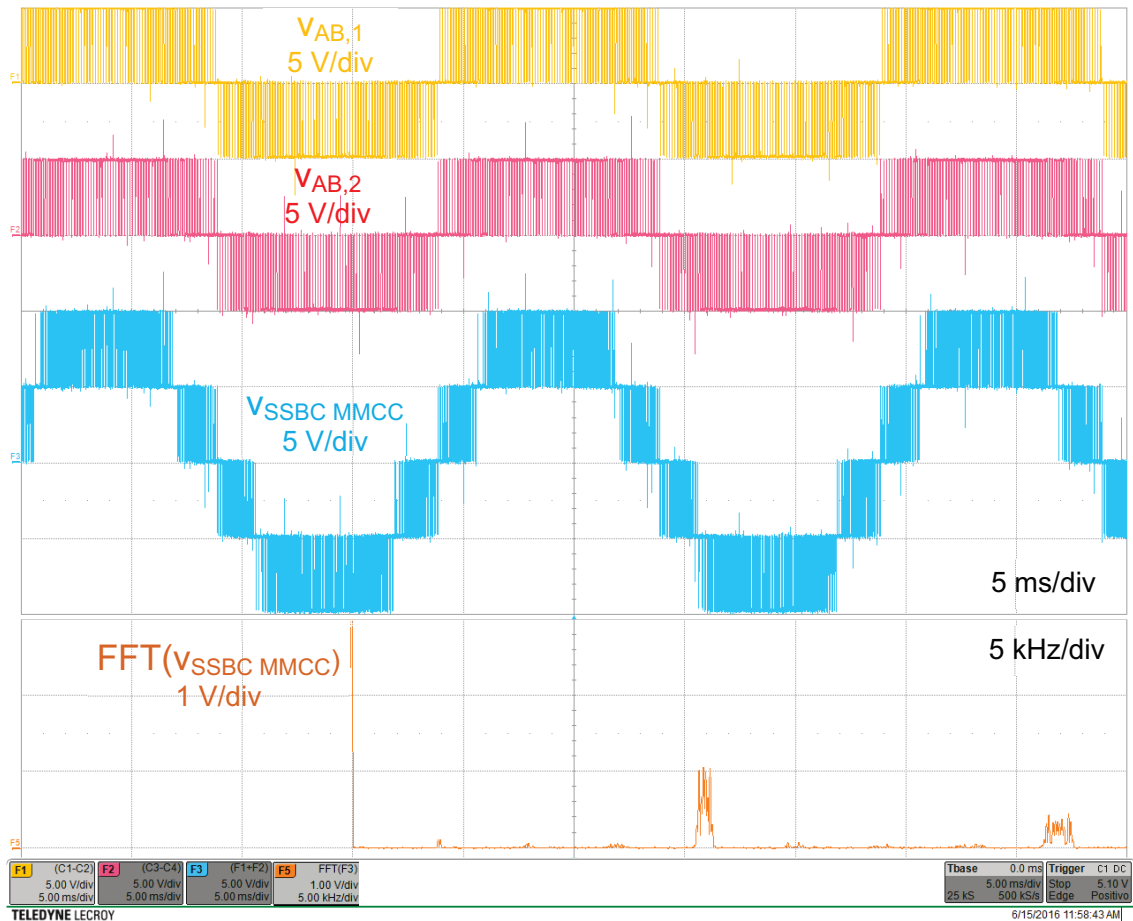


Fig. 1.57: 5-level PWM generated by a SSBC MMCC inverter ( $M = 0.8$ ,  $f = 50\text{Hz}$ ,  $f_{sw} = 4\text{kHz}$ ).

If unipolar modulation is adopted for each H-Bridge, the system operates with a virtual switching frequency equal to twice the real switching frequency of each cell multiplied by the number of cells for each phase. With the phase shifted modulation, in the produced PWM voltage, it is possible to achieve harmonic cancellation up to the  $2N$ -th carrier multiple [23]. In Fig. 1.57 the three level (typical of unipolar modulation) output voltages of each H-bridge ( $v_{AB,1}$  and  $v_{AB,2}$ ) the 5-level SSBC MMCC output voltage are represented. This PWM signals have been generated with a low DC voltage source of 5V, a modulating signal with an amplitude  $M = 0.8$  and a frequency  $f = 50\text{Hz}$ , while the switching frequency is  $f_{sw} = 4\text{kHz}$ . In Fig. 1.57 there is also represented the harmonic

spectrum of the 5-levels SSBC MMCC output voltage. With  $N=2$  the harmonic cancellation up to the 4th carrier harmonic is achieved, indeed the first significant harmonic carrier is located at 16 kHz.

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## Chapter II

# DAB Converters for DC Smart Grids: Modeling and Control

The DAB converter topology has been introduced in [1]-[2] and it offers many advantages in DC/DC conversion which can be summarized in: bidirectional power flow, galvanic isolation, step up/down capabilities and Zero Voltage Switching (ZVS) depending on the operating condition [1], [2], [3], [4], [5].

The bidirectional capabilities make it an attractive choice in many applications; e.g., energy storage systems, where it is needed to control the power flow between the energy storage and the loads [4]. Fig. 2.1 represents the DAB circuit configuration consisting of two active H-Bridges connected by a High Frequency Transformer (HFT) on their AC sides, enabling power flow in both directions in case of active loads.

Choosing the proper turns ratio for the HFT, DAB converters allow the connection of loads and storages characterized by different voltage levels. Besides, in case of applications where galvanic isolation is required, the presence of a HFT instead of a low frequency transformer allows to reduce the size of the power conversion system resulting in high power density.

Looking at the DC Smart Grids, the DAB converters provide flexibility to the DC Multibus thanks to the possibility to extend the voltage range operation and to ensure galvanic isolation avoiding faults propagation.

Considering other examples of DC Smart Grids such as in a MEA, volume and weight optimization is a critical issue. Hence the increase of the transformer fundamental frequency allows volume and weight reduction without increasing the winding current density  $J_{rms}$  and/or the maximum core flux density  $B_{max}$ . It is evident when calculating the product of the core cross section area  $A_{core}$  and the winding window area  $A_{wdg}$ , which

defines the dependency of the physical size and/or volume of a transformer on the power to be transferred [6]. It results:

$$A_{core} A_{Wdg} = \frac{\sqrt{2}}{\pi} \frac{P}{k_W J_{rms} B_{max} f} \rightarrow V \propto (A_{core} A_{Wdg})^{\frac{3}{4}} \propto \frac{1}{f^{\frac{3}{4}}} \quad (2.0)$$

where  $f$  denotes the transformer operating frequency, and  $k_W$  is the winding window filling factor. This is especially relevant in applications where space and weight are critical, as in the case of traction applications, electric vehicles and in aerospace application [7]. Also, the step up/down capability allows for large differences between the input and output voltages, since the voltage conversion ratio depends not only on the control of the power switches, but also on the transformer turns ratio, making this topology suitable for applications requiring large boost/buck capabilities [8].

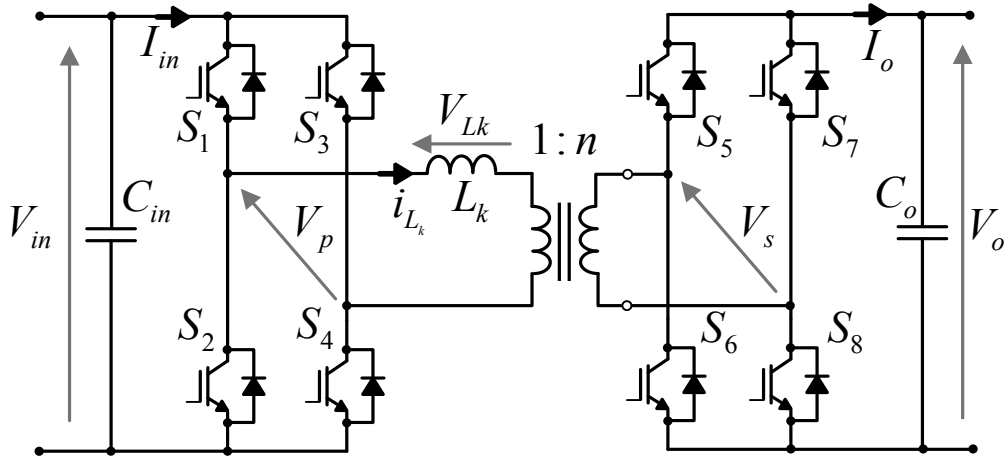


Fig. 2.1: DAB converter.

## 2.1 DAB Converter Switching Function

Several switching schemes have been developed to improve the DAB operation [9], [10]; however, in this study has been implemented the switching scheme based on the assumption that the only control input to the system is the phase shift (PS) between the two converters. Each H-Bridge is driven with constant duty cycle (50%) to generate a high frequency square-wave voltage to its transformer terminals. Thanks to the presence of a leakage inductance  $L_k$  in the HFT, the two square waves can be properly shifted to

control the power flow from one DC side to the other and vice versa, so bidirectional power flow can be achieved. The direction of the power flow is imposed by the bridge which generates the leading square wave.

In case of a power transfer from the primary side to the secondary side the main waveforms of the DAB converter are shown in Fig. 2.2. A constant reference signal with amplitude of 0.5 p.u. is compared to a unitary high frequency saw-tooth carrier, generating a 50% duty cycle signal to the gate of each switch. In this switching scheme, the power switches are treated as diagonal pairs (pairs  $S_1$ - $S_4$ , and  $S_2$ - $S_3$ ) with constant 50% duty cycle for all pairs; besides the signal for pair  $S_1$ - $S_4$  is complementary to the signal for pair  $S_2$ - $S_3$  as shown in Tab. 2.1. The same switching scheme is applied to the second bridge for the diagonal pairs  $S_5$ - $S_8$  and  $S_6$ - $S_7$ . As shown in Fig. 2.2, with this control signals, a square wave voltage  $V_p$ , with amplitude  $\pm V_{in}$  is generated in the primary side of the transformer. In a similar way, a square wave voltage  $V_s$  with values  $\pm V_o$  is generated in the secondary side of the transformer. All the control signals of the secondary bridge are similar to those of the primary bridge, but with a certain phase shift, indicated in Fig. 2.2 with  $\varphi$ .

The shift  $\varphi$  is the ratio of time delay between the two bridges to one-half of switching period. The voltage on the leakage inductance,  $V_{Lk}$ , is the difference between the phase shifted voltages  $V_p$  and  $V_s'$  (where the apex denotes the quantities referred to the primary side). Therefore a current,  $i_{Lk}$ , flows through  $L_k$  and its behavior depends on the phase shift between  $V_p$  and  $V_s'$  and on the value of  $L_k$ . A typical behavior of the leakage current  $i_{Lk}$  is represented in Fig. 2.2 in case of a positive power flow (from primary to secondary side).

Tab. 2.1: DAB switching table.

$S_1 - S_4$	$S_2 - S_3$	$V_p$	$S_5 - S_8$	$S_6 - S_7$	$V_s$
1	0	$V_{in}$	1	0	$V_o$
0	1	$-V_{in}$	0	1	$-V_o$

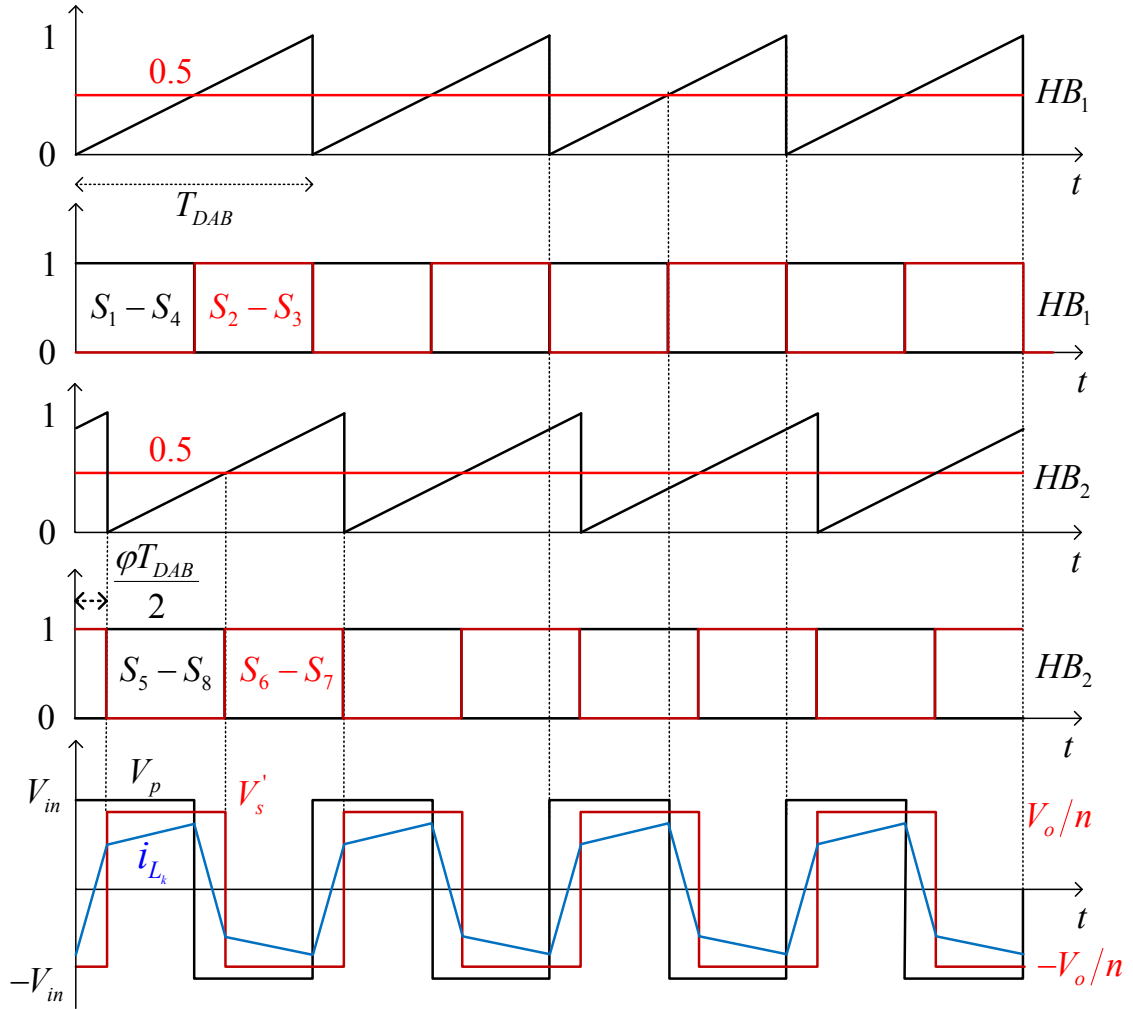


Fig. 2.2: DAB – Typical switching waveforms for Primary to Secondary power transfer.

## 2.2 DAB Converter Average Model

The DAB converter average model can be analytically derived studying the behavior of the leakage current that flows through  $L_k$ . The input and output average currents can be evaluated, as in [11]. Due to the symmetry of the circuit, using graphical techniques on the inductor waveform over half a switching period and considering the representation of the quantities of the output current in Fig. 2.3, equations (2.1) and (2.2) are obtained, for the two different states of the converter in a semi-period.

$$V_{Lk} = V_{in} + V_o' = L_k \frac{2(I_1 + I_2)}{\varphi T_{DAB}} \quad \text{for } 0 < t < \frac{\varphi T_{DAB}}{2} \quad (2.1)$$

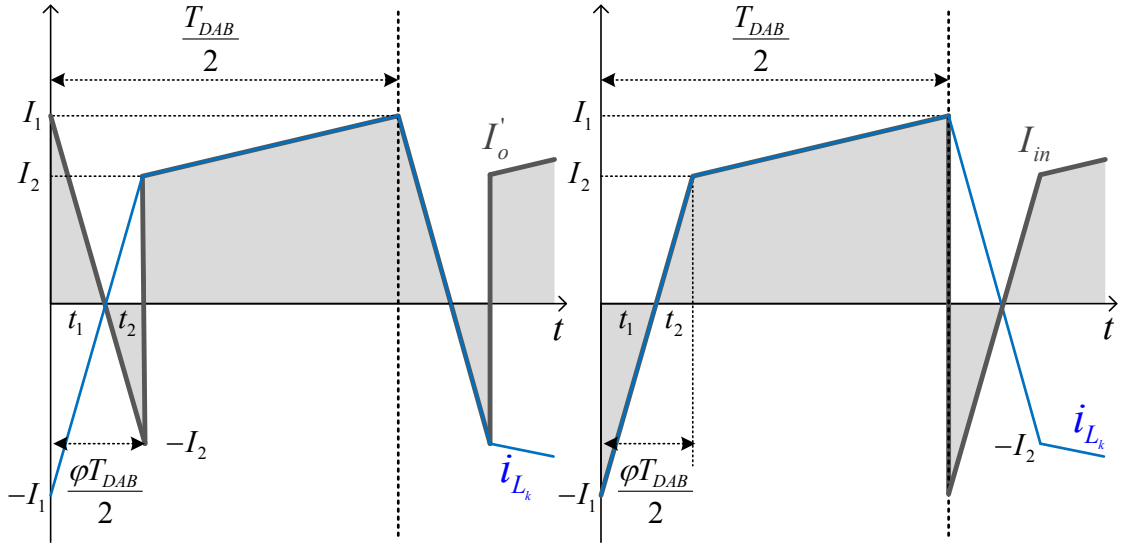


Fig. 2.3: Waveform of the output current  $I_o'$  (left) and input current  $I_{in}$  (right).

$$V_{Lk} = V_{in} - V_o' = L_k \frac{2(I_1 - I_2)}{(T_{DAB} - \varphi T_{DAB})} \quad \text{for } \frac{\varphi T_{DAB}}{2} < t < \frac{T_{DAB}}{2} \quad (2.2)$$

with:

$$V_o' = \frac{V_o}{n}; \quad \frac{I_1}{t_1} = \frac{I_2}{t_2}; \quad t_1 + t_2 = \frac{\varphi T_{DAB}}{2}; \quad (2.3)$$

Solving this set of equations, the following are obtained:

$$I_1 = \frac{T_{DAB}}{4L_k} (2V_o'\varphi + V_{in} - V_o') \quad (2.4)$$

$$I_2 = \frac{T_{DAB}}{4L_k} (2V_{in}\varphi + V_o' - V_{in}) \quad (2.5)$$

$$t_1 = \frac{T_{DAB}}{2} \left( \frac{2V_o'\varphi + V_{in} - V_o'}{2(V_o' + V_{in})} \right) \quad (2.6)$$

$$t_2 = \frac{T_{DAB}}{2} \left( \frac{2V_{in}\varphi + V_o' - V_{in}}{2(V_o' + V_{in})} \right) \quad (2.7)$$

The average current injected into the output cell  $I'_{o,avg}$  and referred to the primary side can be obtained calculating the grey area in a semi-period, as shown in Fig. 2.3:

$$I'_{o,avg} = \frac{2}{T_{DAB}} \left( \frac{1}{2} I_1 t_1 - \frac{1}{2} I_2 t_2 + \frac{1}{2} (1 - \varphi) \frac{I_1 T_{DAB}}{2} \right) \quad (2.8)$$

Substituting equations (2.4) – (2.7) in (2.8), the output average current over half a cycle, referred to the primary side, is given by the equation:

$$I'_{o,avg} = \frac{V_{in} T_{DAB} \varphi (1 - \varphi)}{2L_k} \quad (2.9)$$

Using the same analysis, the input average current  $I_{in,avg}$  can be graphically obtained:

$$I_{in,avg} = \frac{2}{T_{DAB}} \left( \frac{1}{2} I_2 t_2 - \frac{1}{2} I_1 t_1 + \frac{1}{2} (1 - \varphi) \frac{T_{DAB} (I_1 + I_2)}{2} \right) \quad (2.10)$$

and it results in the following:

$$I_{in,avg} = \frac{V_o T_{DAB} \varphi (1 - \varphi)}{2L_k n} \quad (2.11)$$

where  $T_{DAB}$  is the switching period,  $\varphi$  (control variable) is the phase-shift between the primary and secondary voltages of HFT,  $n$  is the turns ratio and  $L_k$  is the transformer leakage inductance, or more generally the coupling inductance between both bridges.  $V_{in}$  and  $V_o$  are respectively the input and output voltage. The output current referred to the secondary side is:

$$I_{o,avg} = \frac{V_{in} T_{DAB} \varphi (1 - \varphi)}{2L_k n} \quad (2.12)$$

From eq. (2.12) it is possible to derive the simplified average model of DAB, with an ideal transformer, as depicted in Fig. 2.4. Frequencies and time-domain studies were performed by authors of [12] to validate the model for frequency values an order of magnitude lower than the switching frequency. The effects of blanking time were not accounted for.

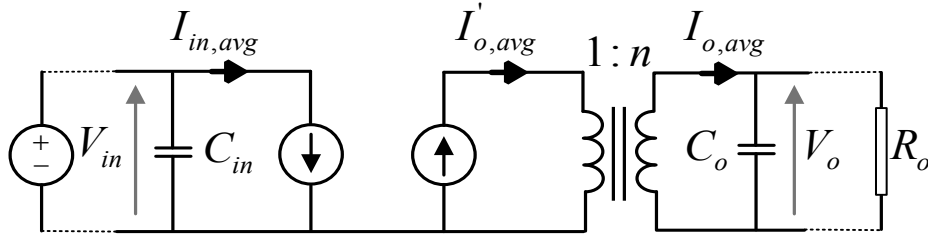


Fig. 2.4: Simplified average model of a DAB.

The real power flows from the bridge with leading phase angle to the bridge with lagging phase angle, the amount of transferred power is controlled by the phase angle difference and it depends on the DC voltages as in [12].

$$P_{DAB} = \frac{V_{in} V_o T_{DAB} \varphi(1-\varphi)}{2L_k n} \quad (2.13)$$

The before derived average model presents a nonlinearity in the actuating term  $\varphi(1-\varphi)$  which represents the expression of a parabolic function; furthermore this term is multiplied in eq. (2.11) for the controlled output voltage  $V_o$  and in eq. (2.12) the same term is multiplied for the input voltage  $V_{in}$ . In order to control the output voltage with a linear regulator, it becomes necessary to derive a linearized model of the system around a stable steady-state point. The linearization procedure has been derived in the following section.

### 2.3 DAB Converter Small Signal Model

The small signal model of the DAB converter has been derived using the linearization technique. The average input and output current equations (2.11) – (2.12) have been perturbed around their steady-state points and it results in:

$$(\tilde{I}_{in} + \bar{I}_{in}) = \frac{T_{DAB}}{2L_k n} (\tilde{\varphi} + \bar{\Phi}) (1 - (\tilde{\varphi} + \bar{\Phi})) (\tilde{V}_o + \bar{V}_o) \quad (2.14)$$

$$(\tilde{I}_o + \bar{I}_o) = \frac{T_{DAB}}{2L_k n} (\tilde{\varphi} + \bar{\Phi}) (1 - (\tilde{\varphi} + \bar{\Phi})) (\tilde{V}_{in} + \bar{V}_{in}) \quad (2.15)$$

where  $(\tilde{X} + \bar{X})$  denotes the sum of the small perturbation of signal  $X$  added to its steady-state value. Solving the eq. (2.15), it results:

$$(\tilde{I}_o + \bar{I}_o) = \frac{T_{DAB}}{2L_k n} (\tilde{\varphi} + \bar{\Phi} - \tilde{\varphi}^2 - 2\tilde{\varphi}\bar{\Phi} - \bar{\Phi}^2) (\tilde{V}_{in} + \bar{V}_{in}) \quad (2.16)$$

Neglecting the square of the perturbation, it can be simplified and solved in the following equations:

$$(\tilde{I}_o + \bar{I}_o) = \frac{T_{DAB}}{2L_k n} (\tilde{\varphi}(1 - 2\bar{\Phi}) + \bar{\Phi}(1 - \bar{\Phi})) (\tilde{V}_{in} + \bar{V}_{in}) \quad (2.17)$$

$$\tilde{I}_o = \frac{T_{DAB}}{2L_k n} (\tilde{\varphi}(1 - 2\bar{\Phi})\bar{V}_{in} + \tilde{V}_{in}(1 - \bar{\Phi})\bar{\Phi} + \tilde{\varphi}\tilde{V}_{in}(1 - 2\bar{\Phi})) \quad (2.18)$$

Assuming to neglect the product of two perturbations, it results:

$$\tilde{I}_o = \frac{T_{DAB}}{2L_k n} [\tilde{\varphi}(1 - 2\bar{\Phi})\bar{V}_{in} + \tilde{V}_{in}(1 - \bar{\Phi})\bar{\Phi}] \quad (2.19)$$

In the same way the input current  $\tilde{I}_{in}$  results in:

$$\tilde{I}_{in} = \frac{T_{DAB}}{2L_k n} [\tilde{\varphi}(1 - 2\bar{\Phi})\bar{V}_o + \tilde{V}_o(1 - \bar{\Phi})\bar{\Phi}] \quad (2.20)$$

Assuming to supply a resistive load  $R_o$ , as in Fig. 2.4, the transfer function between the output current  $\tilde{I}_o$  and the output voltage  $\tilde{V}_o$  is:

$$\tilde{V}_o = \left( \frac{R_o}{R_o C_o s + 1} \right) \tilde{I}_o \quad (2.21)$$

Substituting (2.19) in (2.21), it is obtained:

$$\tilde{V}_o = \left( \frac{R_o}{R_o C_o s + 1} \right) \frac{T_{DAB}}{2L_k n} [\tilde{\varphi}(1 - 2\bar{\Phi})\bar{V}_{in} + \tilde{V}_{in}(1 - \bar{\Phi})\bar{\Phi}] \quad (2.22)$$

Denoting two constant gains as

$$G_\varphi = \frac{T_{DAB}}{2L_k n} (1 - 2\bar{\Phi}) \bar{V}_{in} \quad G_V = \frac{T_{DAB}}{2L_k n} (1 - \bar{\Phi}) \bar{\Phi} \quad (2.23)$$

the final expression of the output voltage loop is:

$$\tilde{V}_o = \left( \frac{R_o}{R_o C_o s + 1} \right) [G_\varphi \tilde{\varphi} + G_V \tilde{V}_{in}] \quad (2.24)$$

In such control system,  $\tilde{V}_o$  is the controlled variable,  $\tilde{\varphi}$  is the control input,  $\tilde{V}_{in}$  is considered as an external disturbance, while  $R_o C_o$  is the time constant of the plant. Fig. 2.5 shows the block diagram representation of the DAB small signal model.

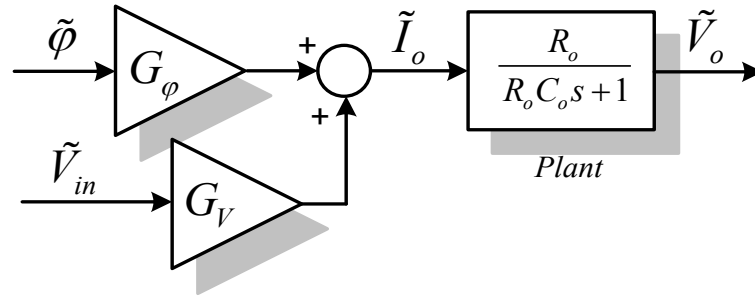


Fig. 2.5: DAB output voltage small signal model.

## 2.4 DAB Output Voltage Control Loop

The proposed output voltage control loop is based on the small signal model in (2.24), where a constant DC voltage supply is assumed for the input voltage  $V_{in}$ . With this hypothesis, the small variation  $\tilde{V}_{in}$  can be neglected and eq. (2.24) becomes:

$$\tilde{V}_o = G_\varphi \left( \frac{R_o}{R_o C_o s + 1} \right) \tilde{\varphi} \quad (2.25)$$

The control of  $\tilde{V}_o$  is carried out by means of a PI regulator and the complete voltage control loop is represented in Fig. 2.6. The PI control law is the following:

$$\tilde{\varphi} = K_{p_o} \left( 1 + \frac{1}{T_{i_o} s} \right) (\tilde{V}_o^* - \tilde{V}_o) \quad (2.26)$$

where  $K_{p_o}$  is the proportional gain and  $T_{i_o}$  is the integral time constant.

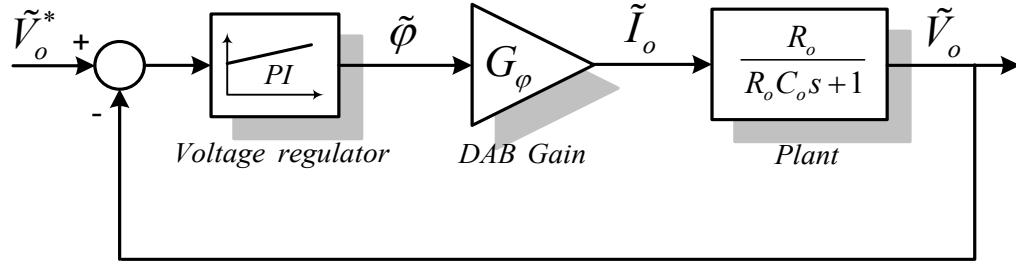


Fig. 2.6: Voltage Control loop of the DAB converter based on a PI controller.

Substituting (2.26) in (2.25) the open loop transfer function is the following:

$$G_{V_o}(s) = \frac{G_\varphi K_{p_o}}{T_{i_o}} \left( \frac{T_{i_o} s + 1}{s} \right) \left( \frac{R_o}{R_o C_o s + 1} \right) \quad (2.27)$$

#### 2.4.1 Voltage Controller Design and Validation

Choosing  $T_{i_o}$  equal to the plant time constant  $R_o C_o$ , and supposing a perfect pole-zero cancellation, the voltage open-loop transfer function in the S-Laplace domain is:

$$G_{V_o}(s) = G_\varphi K_{p_o} \left( \frac{1}{C_o s} \right) \quad (2.28)$$

The closed loop transfer function with a unitary feedback branch is:

$$H_{V_o}(s) = \frac{1}{\left( 1 + \frac{s}{K_{DAB} K_{p_o}} \right)} \quad \text{with } K_{DAB} = \frac{G_\varphi}{C_o} \quad (2.29)$$

It results in a first order system, with a tracking and rejection capability depending on the value of the proportional gain  $K_{p_o}$ . In a first order system as in (2.29),  $K_{p_o}$  and the settling time  $T_{settling}$  are linked by the following equation

$$K_{p_o} = \frac{3}{T_{settling} K_{DAB}} \quad (2.30)$$

where  $T_{settling}$  is assumed as the time to reach the 5% of the final value in case of a step response. Increasing  $K_{p_o}$  it results in a faster step response with a small  $T_{settling}$  and vice versa. Simulation and experimental results are reported in the following, considering the power stage parameters as in Tab. 2.2. The leakage inductance can be calculated as:

$$L_k = \frac{V_o V_{in} T_{DAB} \varphi_{\max} (1 - \varphi_{\max})}{2n P_{\max}} \approx 63 \mu H \quad (2.31)$$

The following second order equation has to be solved in order to determine the phase shift  $\Phi$ . Two solutions are possible, the right solution satisfies the relation  $\Phi < \varphi_{\max}$ :

$$\bar{\Phi}^2 - \bar{\Phi} + \frac{2L_k P_n f_{sw\_DAB}}{\bar{V}_o \bar{V}_{in}} = 0 \quad \text{with } \bar{\Phi} \leq \varphi_{MAX} \quad (2.32)$$

Tab. 2.2: DAB Power Stage Parameters

<b><i>Symbol</i></b>	<b><i>Description</i></b>	<b><i>Value</i></b>
$V_{in}$	<i>Input DC Voltage</i>	250 V
$V_o$	<i>Output DC Voltage</i>	250 V
$L_k$	<i>Leakage Inductance</i>	63 $\mu H$
$n$	<i>Transformer turns ratio</i>	1
$C_{in} \sim C_o$	<i>DC Capacitor</i>	420 $\mu F$
$R_o$	<i>Passive Load</i>	62.5 $\Omega$
$f_{sw\_DAB}$	<i>DAB Switching Frequency</i>	12 kHz
$P_n$	<i>Nominal Power</i>	1 kW
$P_{MAX}$	<i>Maximum Power</i>	2 kW
$\varphi_{max}$	<i>Maximum Phase Shift</i>	0.051
$\Phi$	<i>Nominal Phase Shift</i>	0.0248

The simulation results are confirmed by the experimental results. The experimental setup is based on DAB converter assembled with IGBT Danfoss module DP25H1200T101616 and controlled with a dSPACE SCALEXIO system. In Fig. 2.7 the DAB converter is represented and it is visible the HFT (Tauscher Transformatoren GmbH, 600V, 20A, 12 kVA, 12 kHz, 1:1 ratio).

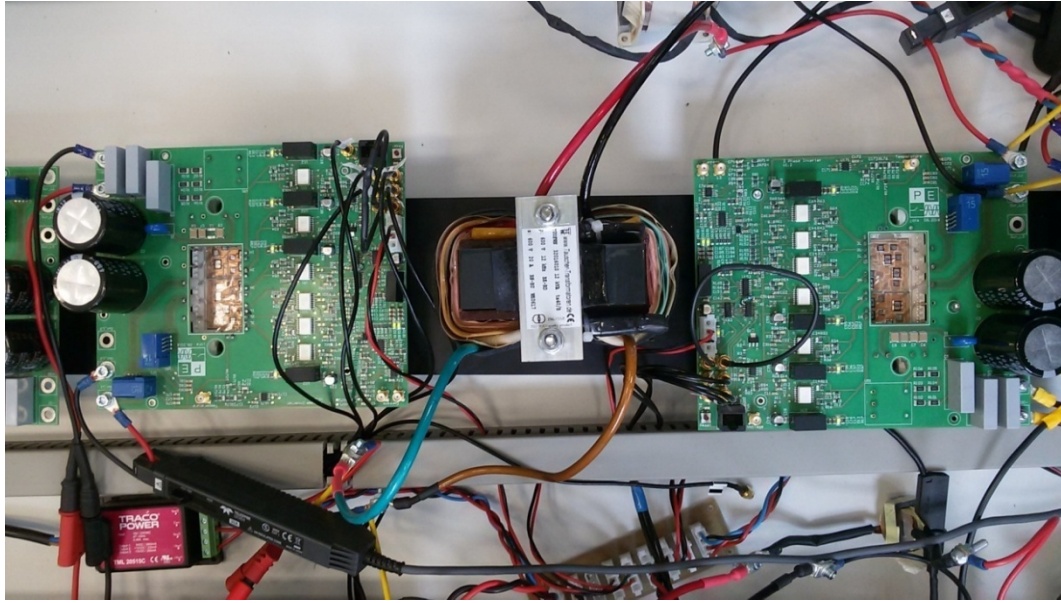


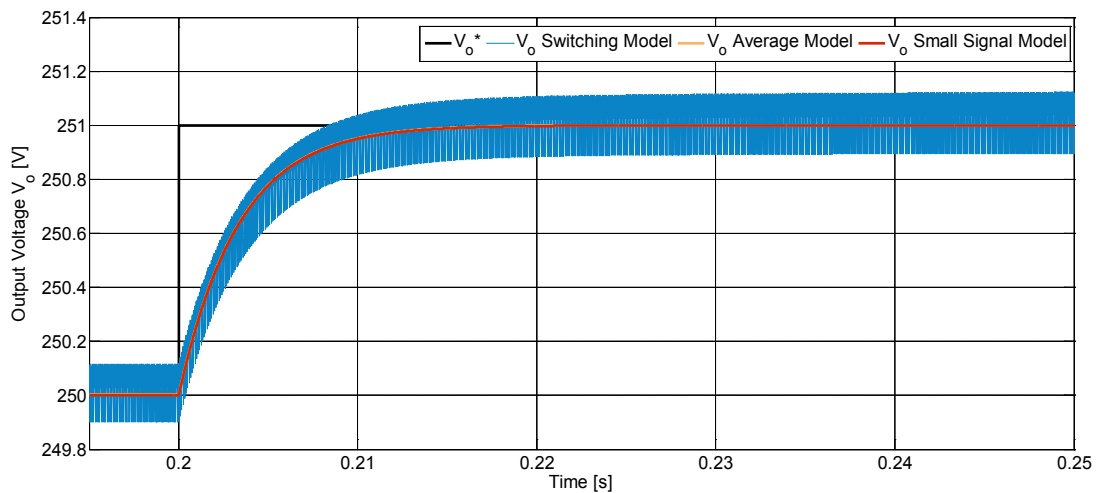
Fig. 2.7: DAB prototype with 12 kHz HFT.

The controller parameters are reported in the following:

$$T_{i_o} = R_o C_o = 0.0263$$

$$T_{settling} (5\%) = 0.01 \quad \rightarrow \quad K_{p_o} = \frac{3}{T_a K_{DAB}} \approx 10^{-3} \quad (2.33)$$

The step response to a  $\Delta V_o^* = 1V$  variation of the reference  $V_o^*$  is reported in Fig. 2.8 for both the average and the small signal model. The results are compared with the results provided the switching model implemented through the PLECS toolbox, validating the derived mathematical models.

Fig. 2.8: DAB Switching, Average and Small Signal model: Step response to a  $\Delta V_o^* = 1V$  variation.

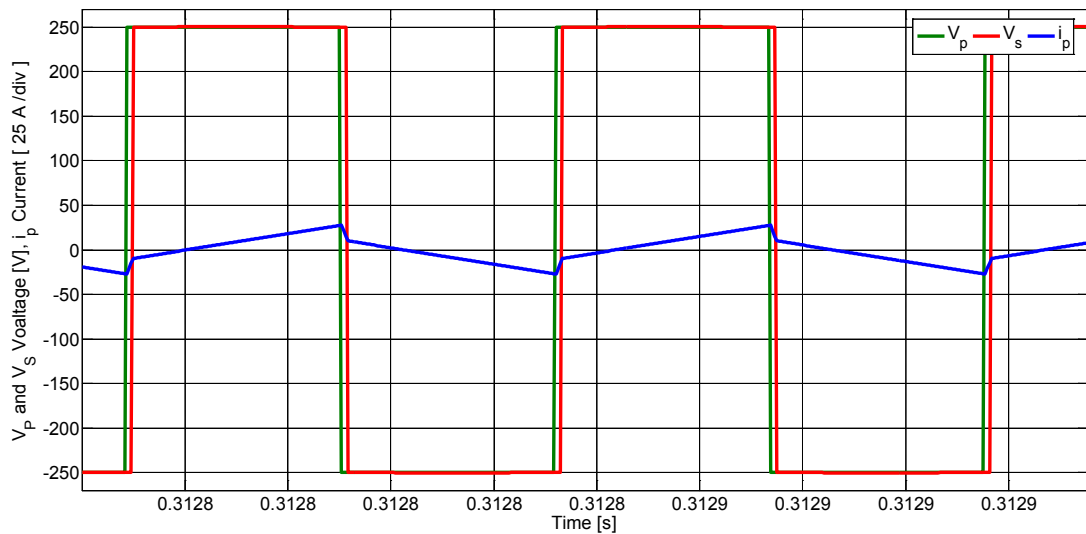


Fig. 2.9: DAB Simulation results: HFT Primary and Secondary voltage, Primary leakage current.

The small signal model and its control method are validated comparing the experimental results with the same obtained in case of the average and small signal model. In Fig. 2.9 and Fig. 2.10 the typical HFT waveforms (Primary voltage, Secondary voltage, Leakage current) are represented in case of simulation and experimental results respectively. In Fig. 2.11-2.13 the experimental output voltage is reported in case  $\Delta V_o^* = 1V$  is applied considering different settling times: 10ms, 100ms and 1000ms. In all the cases, correspondence among the analytical models and the experimental results is verified.

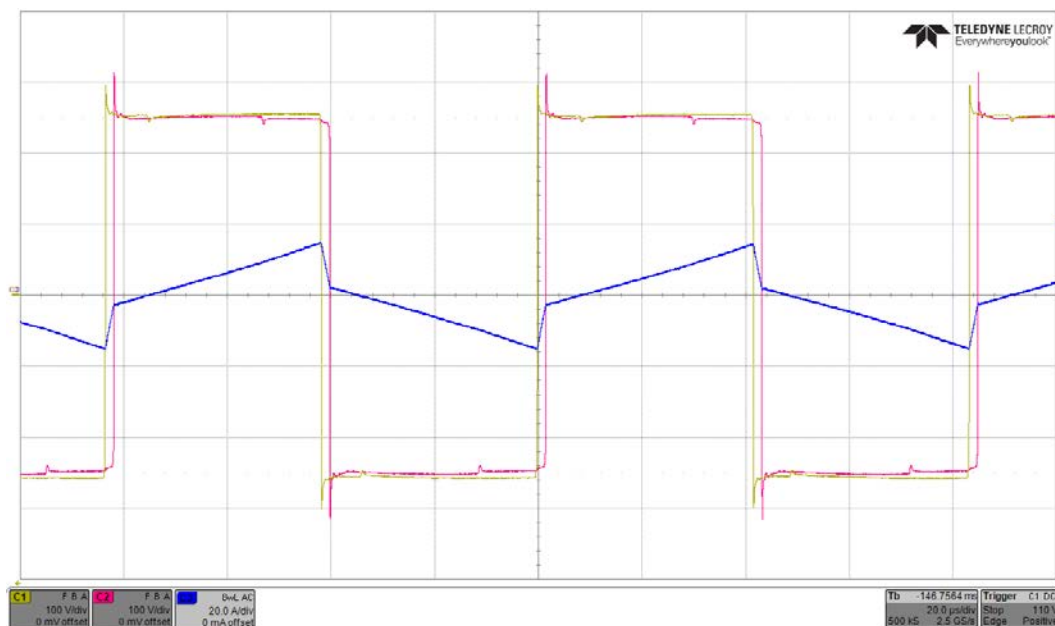


Fig. 2.10: DAB experimental results: HFT Primary and Secondary voltage, Primary leakage current.

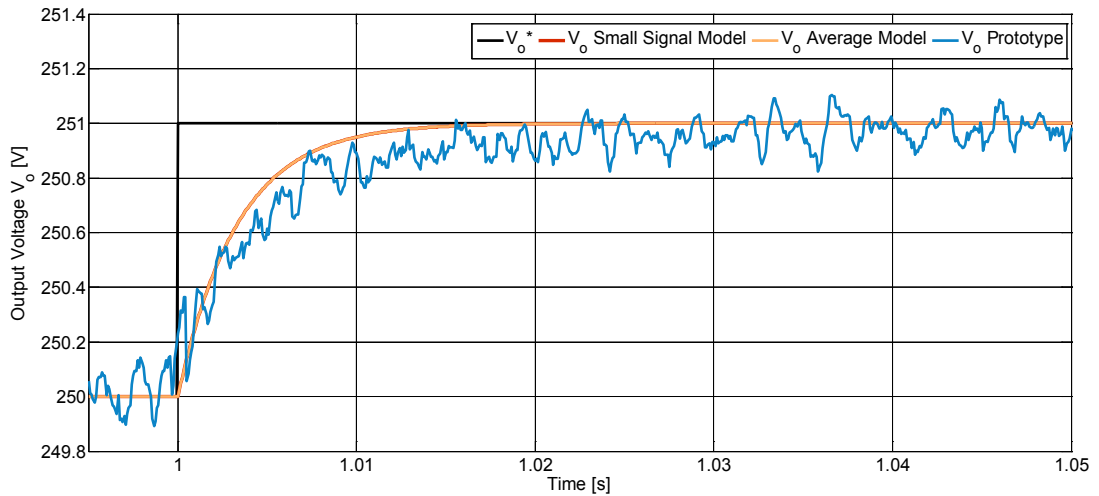


Fig. 2.11: Experimental results: Step response to a  $\Delta V_o^* = 1V$  reference variation, in case of  $T_{\text{settling}} = 10\text{ms}$ .

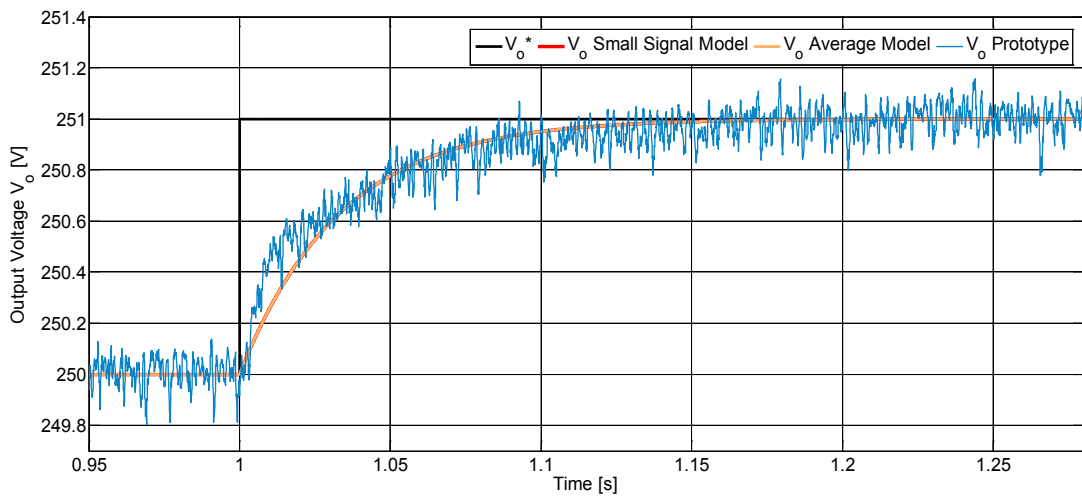


Fig. 2.12: Experimental results: Step response to a  $\Delta V_o^* = 1V$  reference variation, in case of  $T_{\text{settling}} = 100\text{ms}$

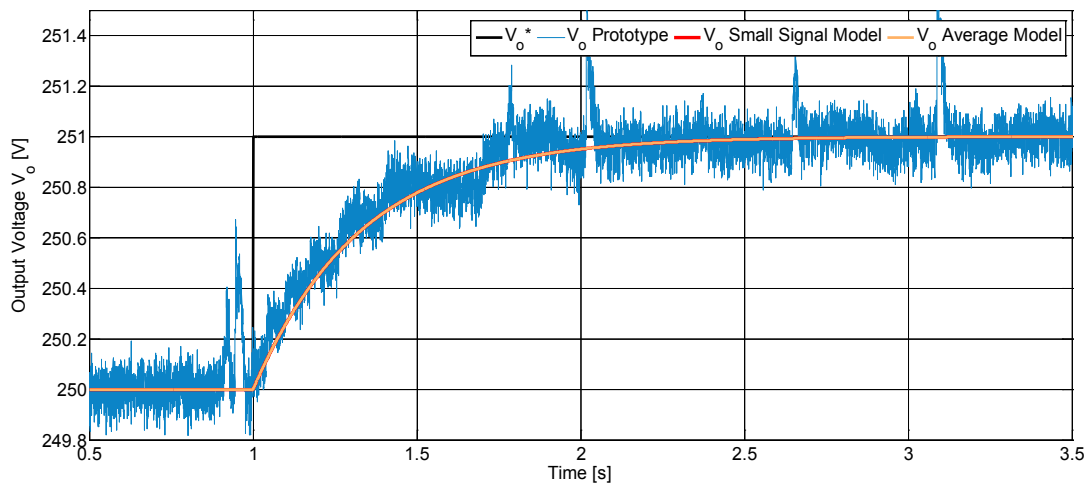


Fig. 2.13: : Experimental results: Step response to a  $\Delta V_o^* = 1V$  reference variation,  $T_{\text{settling}} = 1000\text{ms}$ .

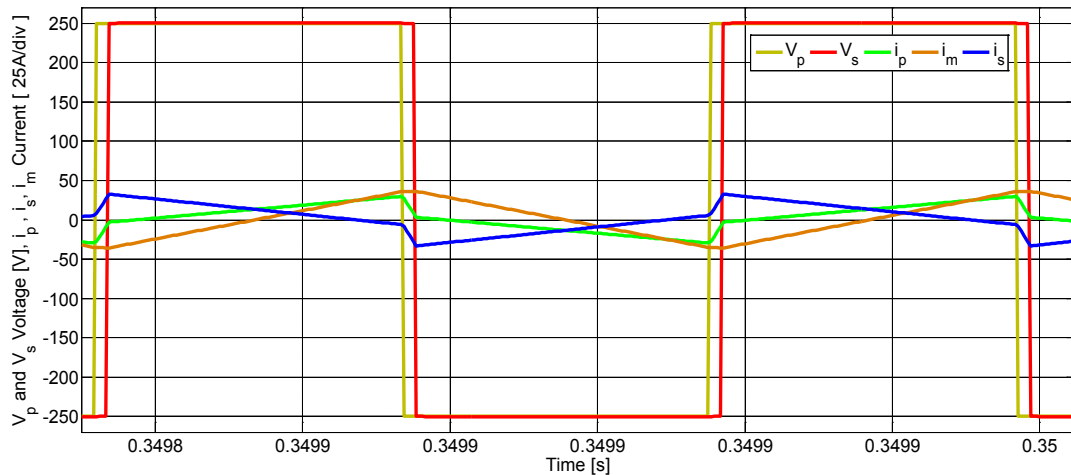


Fig. 2.14: HFT - Primary and Secondary voltage, Primary and Secondary current, Magnetizing current in PLECS simulation

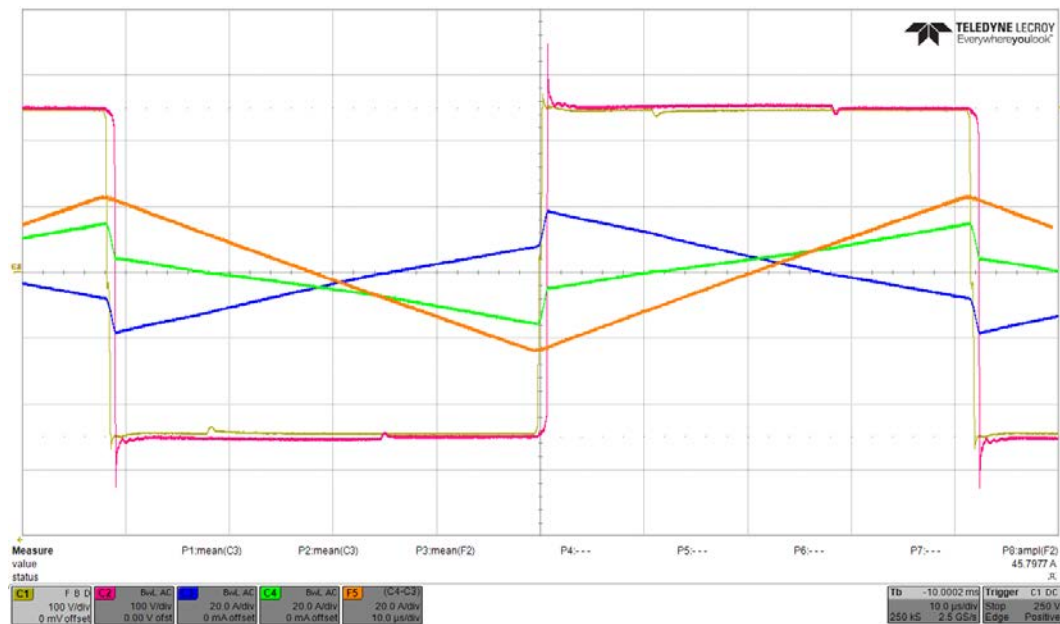


Fig. 2.15: HFT - Primary and Secondary voltage, Primary and Secondary current, Magnetizing Current in Prototype DAB.

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# Chapter III

## SSBC and DAB Converters for MEA Applications

In the new aircrafts the requirement for electrical power onboard is forecasted to rise dramatically because of the following reasons:

- 1) additional electrical loads due to an increased use of electrical actuators and landing gear;
- 2) increased cabin loads for better in-flight entertainment;
- 3) information services and passenger comfort electrically operated (Environmental Conditioning Systems (ECS));
- 4) anti-icing of the wings;
- 5) flight controls and other electrical loads [1].

To meet these requirements, a major reorganization of the aircraft electrical generation and power distribution systems is being undertaken coupling with the MEA concept. In a MEA, the jet engine is optimized to produce the thrust and the electric power. An electric machine is used for starting the engine and for generating electric power. Most of the loads are electrical, including the de-icing and ECSs. The fuel, hydraulic and oil pumps are all driven by electric motors. The more advanced MEA are currently the A380 and B787 where the generator output frequency is allowed to vary from 360 to 800 Hz (variable frequency operation), instead of 400 Hz (constant frequency operation), thus the engine speed is allowed to vary over a speed range of about 2:1.

The wide variation of the frequency can have effect on frequency-sensitive aircraft loads (such as AC electric motors) and on power converters employed in the MEA, involving the need of a complete replacement of the power electronics equipment.

In the MEA, DC power distribution enables a more efficient use of the generated power and aids in paralleling and load sharing. In this scenario a MEA with a DC power distribution system can be treated as DC Smart Grid.

The variable frequency (VF) voltage provided by the electrical machines is converted to 270 V<sub>DC</sub> and then converted to VF AC to control the ECS compressor motors and fans, electrically driven hydraulic pumps, nitrogen generating systems (NGSs) and so on. If the main AC/DC converter is an active rectifier, it can also be used for starting the engines electrically.

Recent developments in power electronics have advanced active rectifier technologies which could replace the traditional TRU [2]. Furthermore, the active rectifier could facilitate the substitution of the synchronous machines by induction machines since the active rectifier can regulate the voltage at the AC bus of the aircraft. This implies lower weight and smaller volume of the machine, pursuing the main goal in the field of MEA. A simplified representation of the desired MEA power conversion system and loads is shown in Fig. 3.1.

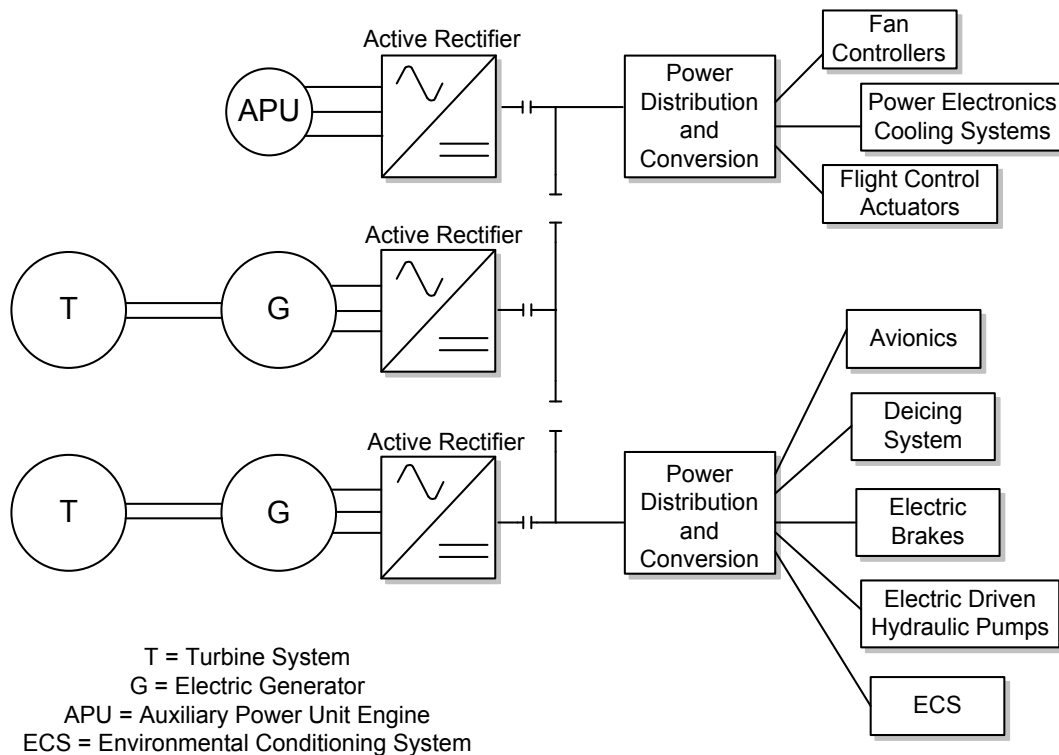


Fig. 3.1: Typical MEA power conversion system and loads.

One of the main constraints for the power converters applied to aircrafts is the low ratio between the switching frequency and the fundamental frequency (400 Hz), coupled to the need of filter size minimization [3]. An advanced active rectifier unit, facilitating the DC power distribution system in a MEA, can be based on a SSBC MMCC [4] coupled to several DAB converters as discussed in the previous Chapters.

The SSBC MMCC topology results particularly suitable for the present application since it provides a virtual switching frequency equal to twice the real switching frequency multiplied by the number of H-Bridge cells for each phase; furthermore it ensures high power quality performances with reduced switching frequency. The system redundancy is guaranteed since a single load can be supplied by a sole DC bus, by more buses simultaneously or sequentially [5]. The DAB converter [6] ensures the desired output voltage (270V) avoiding the occurrence of undesired circulating currents in case of loads sharing among DC buses.

### **3.1 Power quality issues for MEA**

Recognizing the negative impacts of harmonic currents on airborne electrical power generation and distribution systems, the international standard ISO-1540 [7] was the first to introduce limits for input harmonic current distortion of airborne user equipment. Following this trend, the RTCA standard DO-160G [8] added a new section (Section 16) defining limits for current harmonic emissions from loads. Similar requirements have also been discussed among the military system integrators and traduced in the standard MIL-STD-704F [9]. Among the three standards, just the ISO-1540 refers explicitly to the Total Harmonic Distortion (THD) index and, it may be considered that, a special allowance was applied in the past permitting higher harmonic distortion produced by 12-pulse TRU (the current THD limit was 12% for the 12-pulse rectifiers and 8% for all other loads). Actually some aircraft manufacturing enterprises, such as Boeing and Airbus, put forward demands for a harmonic distortion rate around 3%, but controlling effectively the input current harmonics remains a challenge since it is difficult to meet the requirements simultaneously without affecting the other performances, such as the converter voltage transfer ratio, the input power factor and robustness against unbalanced and/or distorted input voltage.

An important drawback related to TRU is the limited power quality performances. However TRU and ATRU were spread out in the past since significant changes in voltage level could be achieved only through transformers. Today power electronics can be used to make these changes in voltage level irrespective of frequency; the use of modular multilevel topologies allows a great improvement of the power quality performances as in the proposed application.

### 3.2 Proposed Active Rectifier

An advanced AC/DC power rectifier for a MEA can be based on a SSBC MMCC.

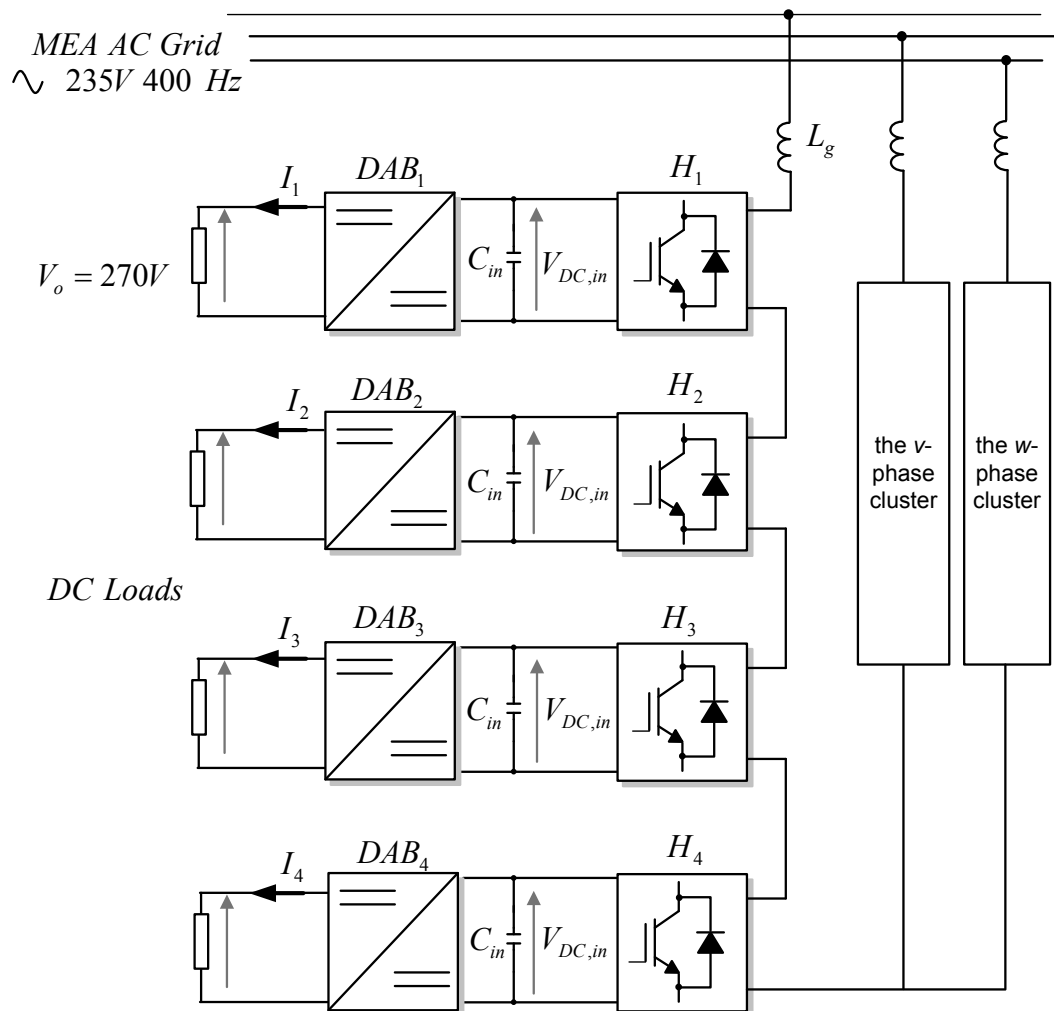


Fig. 3.2: MEA active rectifier unit based on a SSBC MMCC and DAB converters working at the reference voltage  $V_o = 270$  V.

As shown in Fig. 3.2, the SSBC MMCC creates a DC Multibus where each cell is a single-phase H-Bridge power conversion module. Each phase of the SSBC MMCC is treated separately. The performances of a MMCC depends on the number of voltage levels denoted as  $L$ , where  $L$  is defined on the basis of the power conversion cells number  $N$  used for each phase:  $L = 2N + 1$ .

Among the MMCC, the SSBC MMCC represents a topology particularly proper for battery energy storage systems based on one-converter-to-one-battery module [10]-[12]. The SSBC MMCC is coupled to  $N$  DAB converters in order to obtain in output the desired DC voltage level: 270 V. The outputs of the DAB converters can supply loads separately or can share a common load of higher power creating a flexible DC distribution system into the MEA.

### 3.2.1 The SSBC MMCC and Its Control System

In the proposed case-study one leg of the SSBC MMCC is composed by four single-phase H-bridge cells connected in cascade and controlled as shown in Fig. 3.3. If  $N = 4$  the resulting number of level is  $L = 9$ . For each power cell the same DC-Link voltage values is assumed and a unipolar phase-shifted Pulse Width Modulation (PWM) is adopted.

The modulating signal is provided by the control system while the phase shift angle between the carriers of two adjacent cells is:

$$\phi_{cr} = \frac{360^\circ}{(L-1)} \quad (3.1)$$

Hence, in the considered case-study, it results:  $\phi_{cr} = 45^\circ$ . Denoting as  $V_{MEA}$  the RMS value of the MEA AC grid and assuming  $V_{MEA} = 235$  V, it results that

$$V_{AC,H} = \frac{V_{MEA}}{N} \quad (3.2)$$

$V_{AC,H}$  is the RMS value of the first-order component of the AC voltage applied to each H-bridge cell, hence

$$V_{DC,in}^* = \frac{\sqrt{2}V_{AC,H}}{M} \quad (3.3)$$

Eq. (3.3) represents the DC voltage reference value for each cell, where  $M$  is the modulation index. Choosing  $M = 0.83$ , it results  $V_{DC,in}^* = 100 \text{ V}$  that is the minimum DC-link value to ensure the controllability of the converter in parallel operation with the grid.

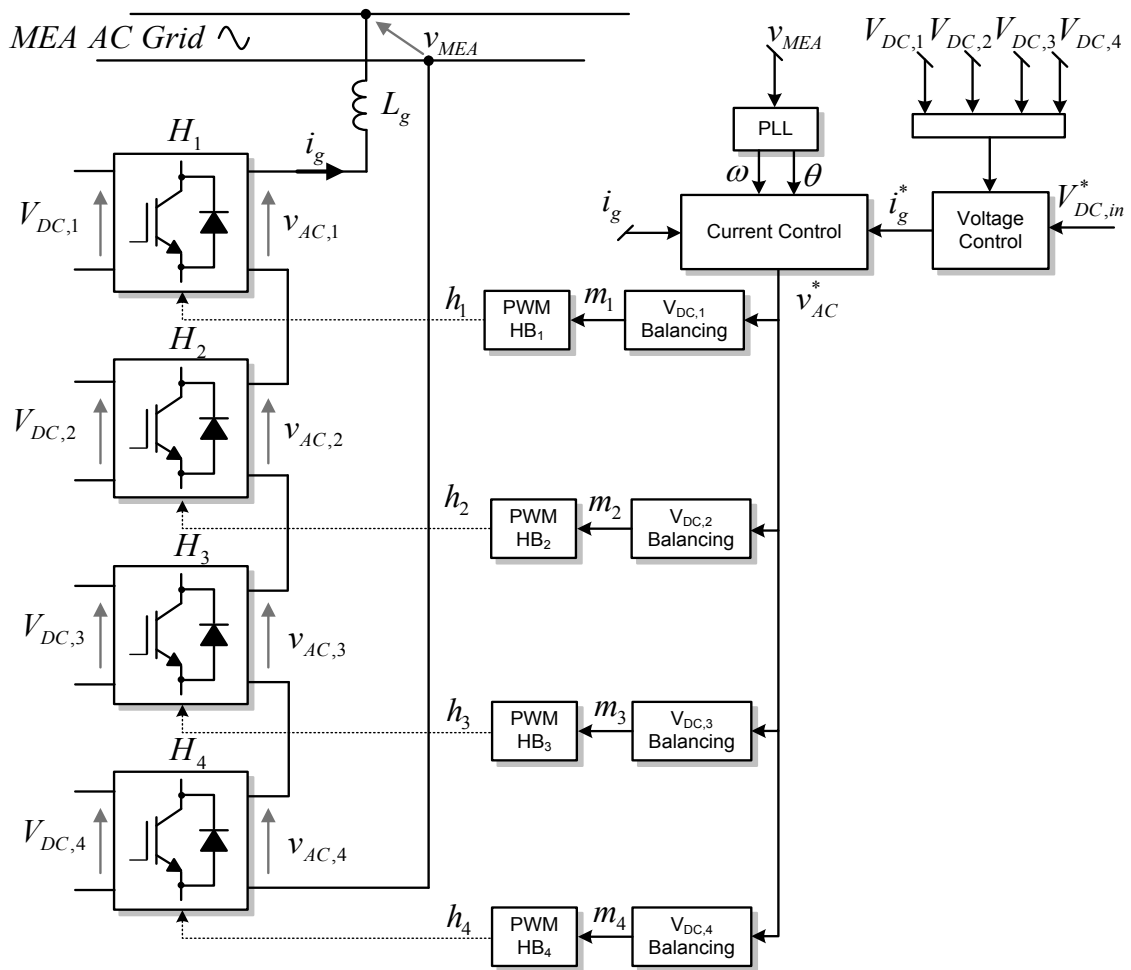


Fig. 3.3  $u$ -phase of the 9-levels SSBC MMCC and its control system.

On the AC side an inductive filter is used to reduce the current harmonic distortion.  $L_g$  is designed limiting to 3% the maximum voltage drop and verifying that the power quality performance on the AC side is in compliance with the aircraft standards. A proper design of the capacitances  $C_{in}$  of each DC-link is fundamental to get the desired DC voltage. Since  $C_{in}$  may be chosen on the basis of the admissible voltage ripple, it can be calculated as:

$$C_{in} = \frac{P_{max}}{(V_{DC,in}^* \Delta U \pm \frac{1}{2} \Delta U^2) f_{sw}} \quad (3.4)$$

where  $P_{max}$  is the maximum value of the instantaneous power,  $V_{DC,in}^*$  is the reference voltage on each DC-link of the SSBC MMCC,  $\Delta U$  is the admissible voltage ripple and  $f_{sw}$  is the switching frequency.

The control system has to guarantee synchronization with the MEA AC grid, hence a PLL circuit is adopted to catch the reference sinusoidal waveform of unitary amplitude, used for the generation of the current reference, as shown in Fig. 3.3. A single voltage controller is used for all the cells, it controls directly the sum of the DC voltage of every cell (or the average value) and indirectly the power exchanged with the main AC providing in output the reference current for P+Resonant current loop. The current control provides in output the sinusoidal duty cycle necessary to obtain the suitable AC converter voltage. A balancing controller adjusts the duty cycle value in each power bridge in order to balance the DC-Link voltages. This cascaded control is equal to that before analyzed in Chapter I.

### 3.2.2 The DAB Converter and Its Control System

In the proposed case-study, four DAB converters are connected to the four DC-links of each phase of the SSBC MMCC (Fig. 3.2). The input voltage  $V_{in}$  denotes the voltage provided by the SSBC MMCC for each cell, the output voltage  $V_o$  denotes the rated voltage at the output of each DAB converter. Different kinds of modulation strategy can be applied for the present topology, however in the present application a bipolar modulation with a 50% duty cycle is adopted in each DAB converter. Resuming the equation of the DAB output current and averaged in a switching period, it results:

$$I_{o,avg} = \frac{V_{in}}{2nL_k f_{sw}} \varphi(1 - \varphi) \quad (3.5)$$

From the equation of the average power processed in the DAB in a switching period, the value of the leakage inductance has been derived as follows:

$$L_k = \frac{V_{in} V_o \Phi_n (1 - \Phi_n)}{2n f_{sw} P_n} \quad (3.6)$$

where  $\Phi_n$  represents the phase shift obtained in correspondence of nominal power  $P_n$ .

The dynamic of the converter can be described using the average model in Fig. 3.4, as:

$$\frac{dV_o}{dt} = -\frac{1}{R_o C_o} V_o + \frac{1}{C_o} \left( \frac{V_{in}}{2nL_k f_{sw}} \varphi (1 - \varphi) \right) \quad (3.7)$$

where  $C_o$  is the output capacitance and  $R_o$  is the load resistance.

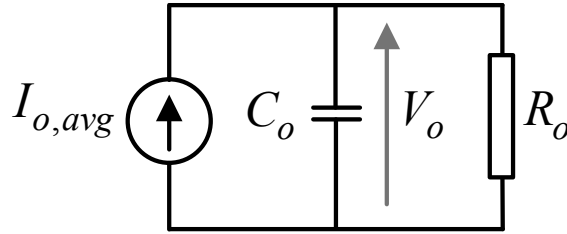


Fig. 3.4: Simplified DAB average model.

Differently from the Chapter 2, linearizing the converter model in order to use linear control techniques, the controller can be designed as follows:

$$V_{aux} = -K_1 V_o + K_2 \int (V_o^* - V_o) dt \quad (3.8)$$

where  $V_{aux}$  is the auxiliary input of the system defined as:

$$V_{aux} = V_{in} \varphi (1 - \varphi) \quad (3.9)$$

Hence, it is obtained:

$$\frac{dV_o}{dt} = -\frac{1}{R_o C_o} V_o + \frac{1}{C_o} \left( \frac{V_{aux}}{2nL_k f_{sw}} \right) \quad (3.10)$$

and replacing the control law in the model, it results:

$$\frac{dV_o}{dt} = -\frac{1}{R_o C_o} V_o + \frac{1}{C_o} \left( \frac{-K_1 V_o + K_2 \int (V_o^* - V_o) dt}{2nL_k f_{sw}} \right) \quad (3.11)$$

In the s-Laplace domain the open loop transfer function can be expressed as follows:

$$G_{V_o}(s) = \frac{K_2 / 2nC_o L_k f_{sw}}{s \left( s + \frac{K_1}{2nC_o L_k f_{sw}} + \frac{1}{R_o C_o} \right)} \quad (3.12)$$

while the closed loop with unitary feedback can be expressed as:

$$H_{V_o}(s) = \frac{K_2 / 2nC_o L_k f_{sw}}{\left( s^2 + \left( \frac{K_1}{2nC_o L_k f_{sw}} + \frac{1}{R_o C_o} \right) s + K_2 / 2nC_o L_k f_{sw} \right)} \quad (3.13)$$

Equation (3.13) can be expressed as a canonical second-order system as function of the damping and nominal frequency by choosing  $K_1$  and  $K_2$  as:

$$K_1 = \left( 2\xi\omega_n - \frac{1}{R_o C_o} \right) 2nC_o L_k f_{sw} \quad (3.14)$$

$$K_2 = \left( 2nC_o L_k f_{sw} \omega_n^2 \right) \quad (3.15)$$

If the system parameters are well known,  $K_1$  and  $K_2$  are tuned in order to satisfy the desired damping  $\xi$  and natural frequency  $\omega_n$  specifications related to the closed-loop transfer function:

$$H_{V_o}(s) = \frac{\omega_n^2}{\left( s^2 + 2\xi\omega_n s + \omega_n^2 \right)} \quad (3.16)$$

The value of  $\xi$  and  $\omega_n$  can be derived from the specifications of the percent overshoot (*p.o.*) and the base frequency  $\omega_b$ :

$$\xi = \sqrt{\frac{[\ln(p.o./100)]^2}{\pi^2 + [\ln(p.o./100)]^2}} \quad (3.17)$$

$$\omega_n = \frac{\omega_b}{-1.19\xi + 1.85} \quad (3.18)$$

The control parameters of the DAB converters ( $K_1$  and  $K_2$ ) have been tuned in order to ensure an overshoot around 2% and a system bandwidth  $\omega_b = 2\pi 32$  rad/s.

The block diagram for the control algorithm is presented in Fig. 3.5.

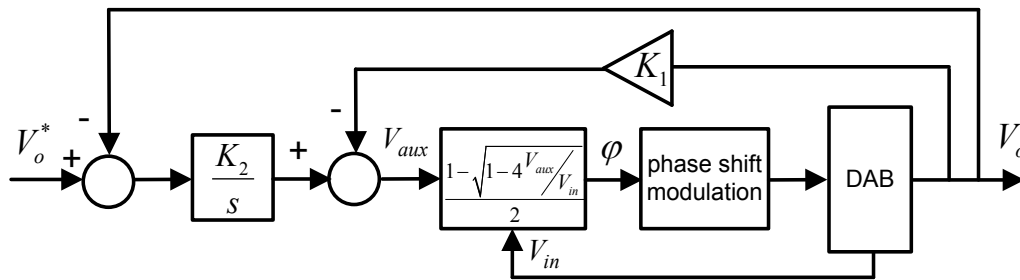


Fig. 3.5: Control of the DAB converter for MEA.

The step response and the Bode diagrams of the closed system loop are reported in Fig.3.6 – Fig. 3.7.

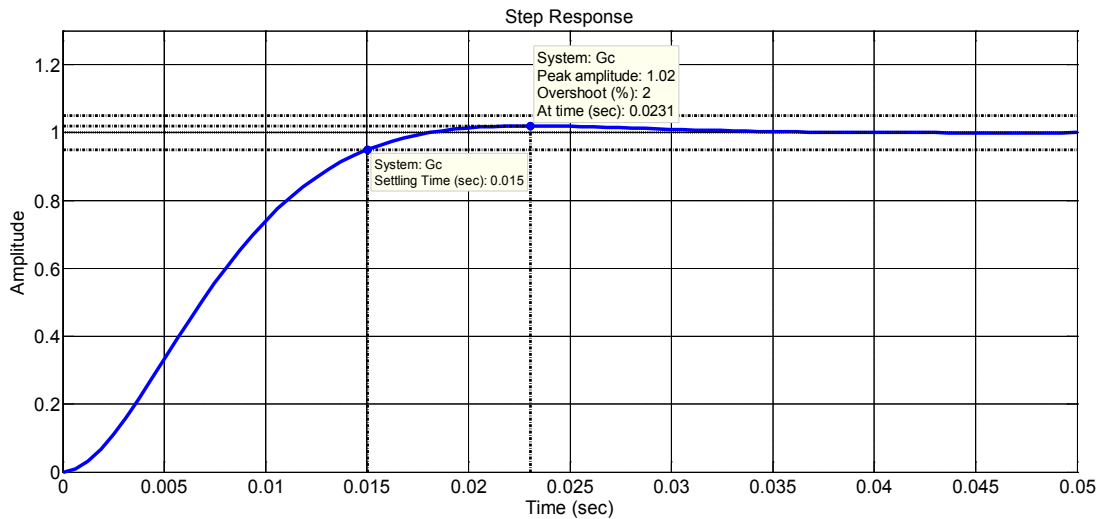


Fig. 3.6: DAB Step response with a 2% overshoot and 15ms settling time.

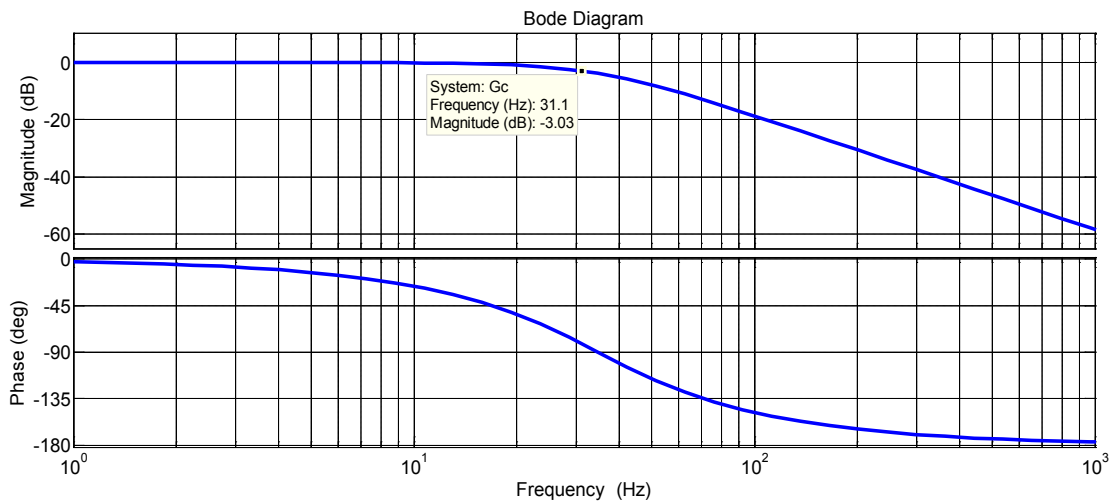


Fig. 3.7: DAB closed loop Bode diagram.

The step response confirms the overshoot of the 2% and a settling time (5%) of 15ms and the Bode diagram confirms the bandwidth of 31.1Hz.

To validate the DAB output voltage model, the simulation results obtained through the switching model have been compared to those related to the average model. The simulation has been structured in order to validate the model in two cases: 1) variations of  $V_o^*$  reference and 2) variation of the load  $R_o$  (the effect of the dead time were not accounted for). In Fig. 3.8 is depicted the time domain simulation used in validation.

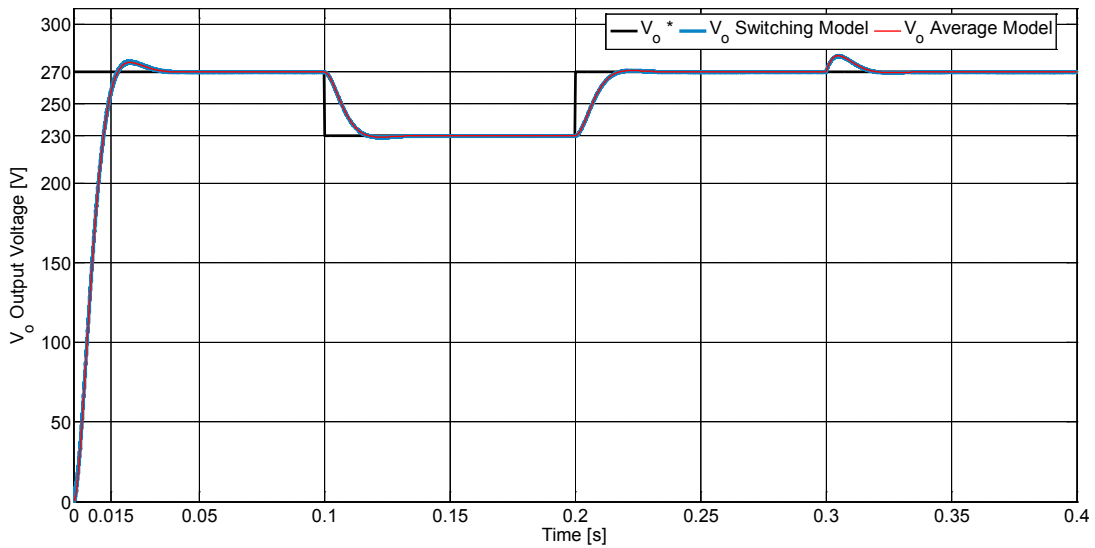


Fig. 3.8: Time domain simulation for DAB model validation.

At  $t=0s$ , the initial output capacitor voltage is equal to zero, the input voltage is  $V_{in}=100V$ , the resistive load is  $R_o=12\Omega$ , while  $V_o^*=270V$ . The control starts and  $V_o$  reaches the 95% of the reference value at  $t=0.015s$  with a 2% overshoot ( $\approx 6V$ ) as required by specification. At  $t=0.1s$  the output reference is stepped down to  $V_o^*=230V$ , while at  $t=0.2s$  it is stepped up to  $V_o^*=270V$ . Finally at  $t=0.3s$  the load is stepped up to  $R_o=13.5\Omega$ , causing a 10% power variation from  $P_n=6kW$  to  $5.4kW$ . In all the cases, the results prove that the average model has the same dynamics of the switching model in terms of tracking disturbance rejection capability.

In Fig. 3.9 are shown the waveforms of the voltage and current at the primary side of the HFT with focus to the phase shift which is set to 0.2 in nominal power load condition.

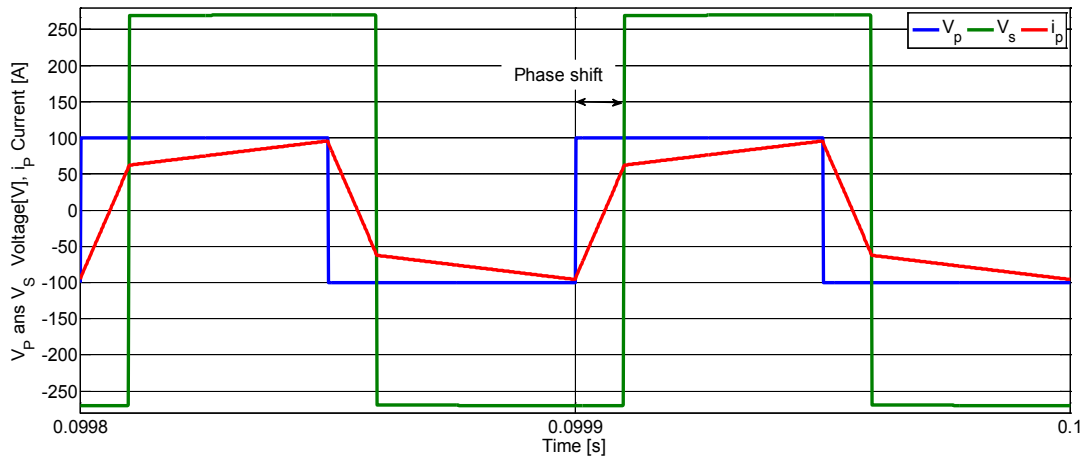


Fig. 3.9: HFT waveforms of a 100V-270V DAB in PLECS simulation.

### 3.3 Behavior of the System in Different Scenarios

The operation of the proposed rectifier unit based on one 9-levels SSBC MMCC and four DAB converters has been investigated in different scenarios:

- A. Steady-state operation at the rated frequency  $f=400$  Hz in case of a single load (shared among all the buses);
- B. Load variations;
- C. Frequency variations in the range 360-800 Hz.

In Tab. 3.1 there are reported the power stage parameters used for the simulation of the SSBC MMCC.

Tab. 3.1: SSBC MMCC Power Stage Parameters.

<b><i>Symbol</i></b>	<b><i>Description</i></b>	<b><i>Value</i></b>
$V_{MEA} (RMS)$	<i>RMS MEA Voltage</i>	<i>235 V / 400Hz</i>
$L_g$	<i>AC Inductor filter</i>	<i>27 <math>\mu</math>H</i>
$V_{DC,in}$	<i>DC Voltage in each cell</i>	<i>100 V</i>
$C_{in}$	<i>DC Capacitor</i>	<i>450 <math>\mu</math>F</i>
$P_n$	<i>Nominal Power</i>	<i>24 kW</i>
$f_{sw}$ SSBC MMCC	<i>SSBC Switching Frequency</i>	<i>10 kHz</i>

In Tab. 3.2 there are summarized the power stage parameters used for the simulation of the DAB stage. The rated power of each cell of the SSBC MMCC is 6kW. The converters have been tested through PLECS toolbox, used for simulation of electrical circuits within the Simulink environment. The models have been developed on the basis of of the SEMiX202GB066HDs trench IGBT modules datasheet.

Tab. 3.2: DAB Power Stage Parameters.

<i>Symbol</i>	<i>Description</i>	<i>Value</i>
$V_{in}$	<i>Input DC Voltage</i>	<i>100 V</i>
$V_o$	<i>Output DC Voltage</i>	<i>250 V</i>
$L_k$	<i>Leakage Inductance</i>	<i>12 <math>\mu</math>H</i>
$n$	<i>Transformer turns ratio</i>	<i>3</i>
$C_o$	<i>Output DC Capacitor</i>	<i>450 <math>\mu</math>F</i>
$R_o$	<i>Passive Load</i>	<i>12.5 <math>\Omega</math></i>
$f_{sw} DAB$	<i>DAB Switching Frequency</i>	<i>10 kHz</i>
$P_n$	<i>Nominal Power</i>	<i>6 kW</i>
$\Phi_n$	<i>Nominal Phase Shift</i>	<i>0.2</i>

### 3.3.1 Steady-state operation

Load sharing allows continuous operation mode even in case of faults on one of the DC buses. Indeed, in case of failure, it is possible to supply part of the load by means of the remaining buses. The first test has been performed in case of a 24 kW single load shared among all the DC buses, as depicted in Fig. 3.10.

The fundamental frequency of the system is  $f=400$  Hz (rated frequency). The equivalent virtual switching frequency is  $2Hf_{sw\_SSBC} = 80$  kHz; does it means that a reduce  $L_g$  filter can be used to satisfy the power quality constraint. The voltage reference for each DC-link of the SSBC MMCC is  $V_{DC,in}^*=100$  V. The voltage reference for the DAB converters is:  $V_o^*=270$ V.

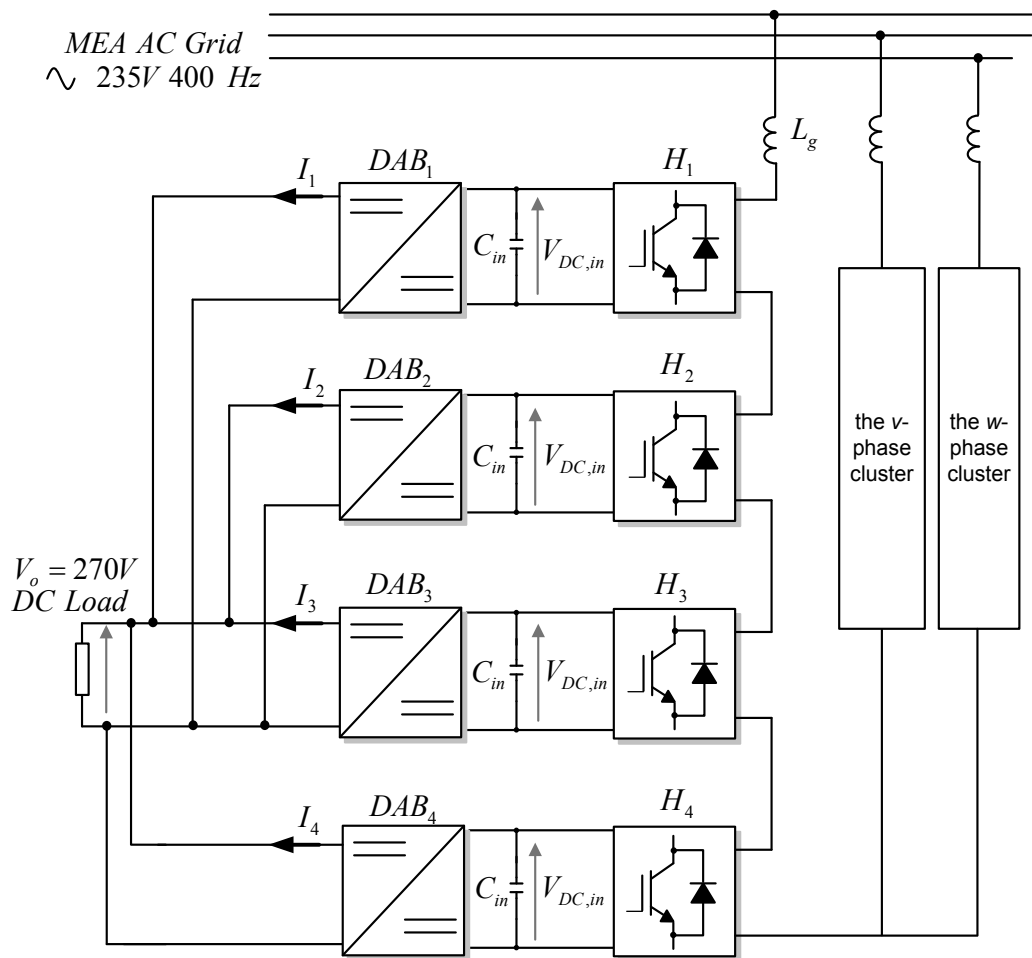


Fig. 3.10: SSBC MMCC and DAB converters with a 24 kW single load shared among all the DC buses.

In Fig. 3.11 the 9-levels voltage of the MMCC SSBC is shown and compared to the MEA AC grid voltage; in the same figure there is depicted the AC current whose THD(%) is equal to 3.5% in compliance with the aircraft standards.

In Fig. 3.12 there are represented respectively the DAB converters output voltages and currents. It is verified that the buses share perfectly the load providing a quarter of the required power.

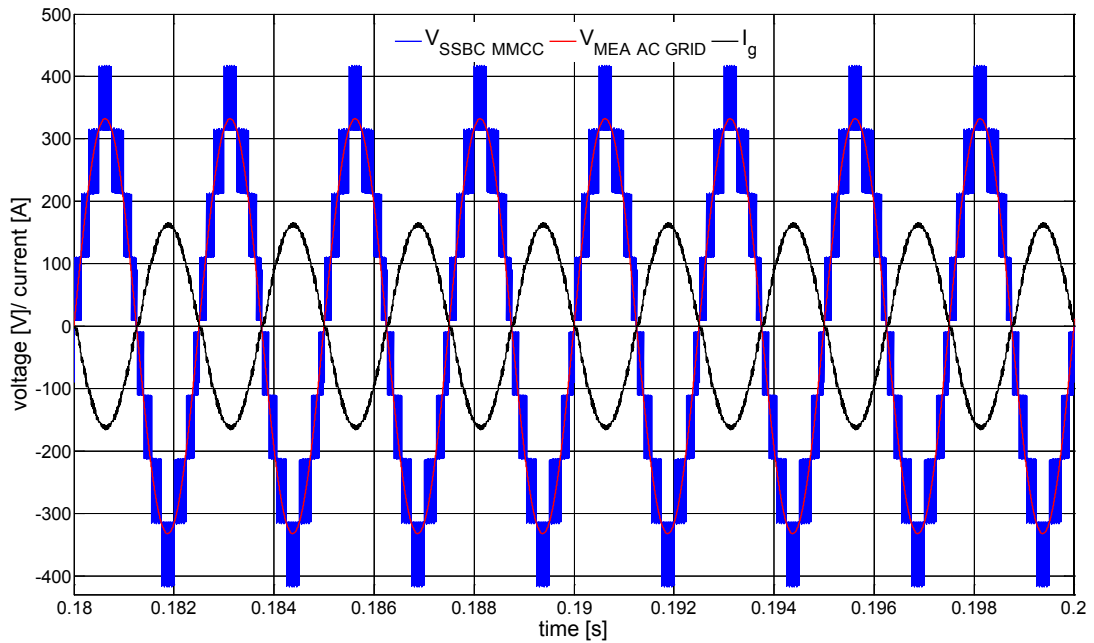


Fig. 3.11: MEA AC voltage, 9-levels voltage of the SSBC MMCC, AC current in case  $f=400$  Hz.

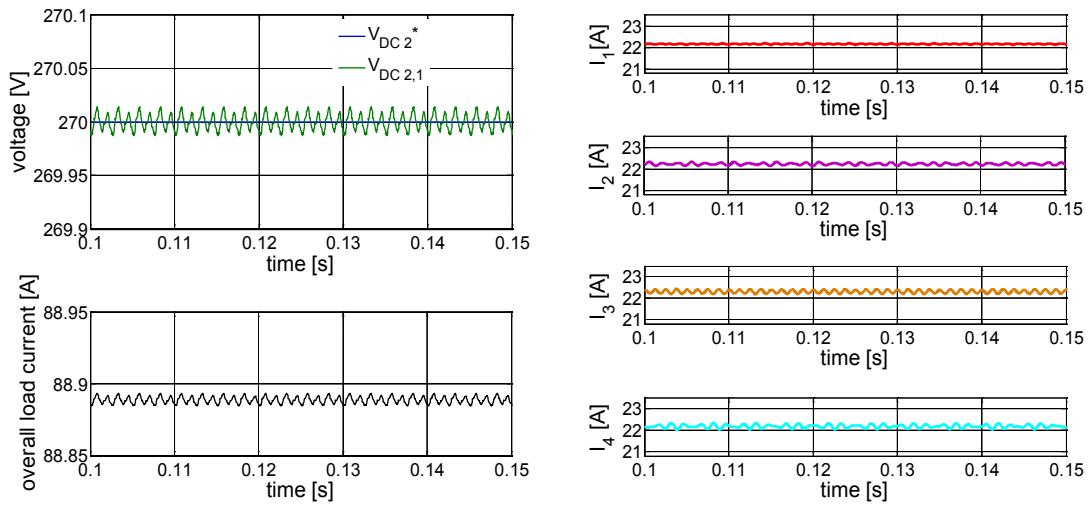


Fig. 3.12: DAB converters output voltages and currents in case all the DC buses are connected in parallel supplying a single load of 24 kW.

### 3.3.2 Load variations

Load variations at one or more buses involves imbalance of the power absorbed by the cells of the SSBC MMCC. With the aim to test the robustness of the control system, the performances of the system have been analyzed in case of load variations. The DC buses operate with one load of 12 kW shared by the DC bus 1 and the DC bus 2 and

another load, of the same power, supplied together by the DC bus 3 and the DC bus 4, as in Fig. 3.12.

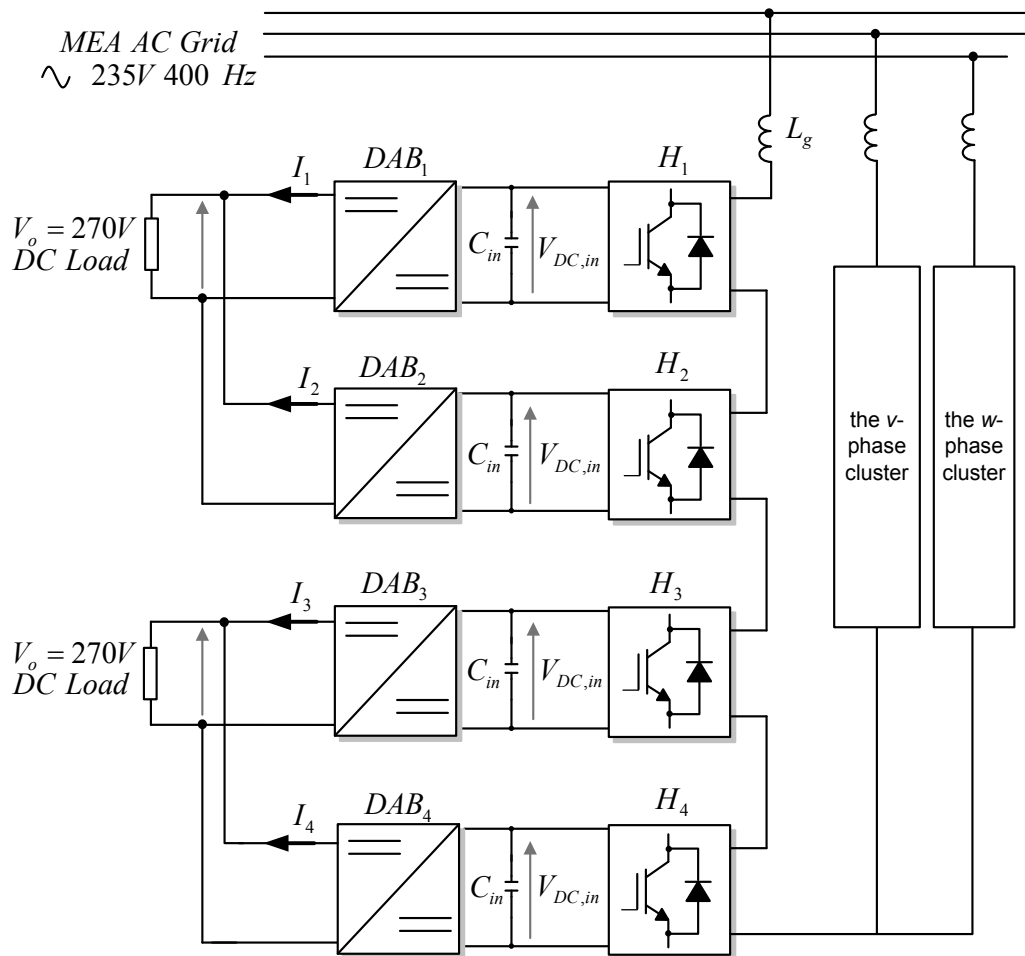


Fig. 3.12: SSBC MMCC and DAB converters with two 12 kW loads shared among two DC buses.

Just some selected results are reported in Fig. 3.13 and Fig. 3.14. A load reduction of 10% is applied at the first load (DC bus 1 and DC bus 2) at  $t_1=0.3$  s. At  $t_2=0.7$  s a load increment of 10% is applied at the second load (DC bus 3 and DC bus 4). High performances are obtained due to the proper action of the DC voltage adjustment, related to every power conversion cell of the SSBC MMCC. The DC-links voltages of the SSBC MMCC, in the described perturbed conditions, are shown in Fig. 3.13. It is possible to observe that the transient behavior is extinguished in less than  $0.06$  s. The DAB converters output voltages and currents are shown in Fig. 3.14; it is verified that the DABs control guarantees correct operation also in case of power variations respect

to the rated conditions: the tuning of the parameters  $K_1$  and  $K_2$  allows to limit the voltage overshoot up 2%. This result is coupled to a very fast dynamics.

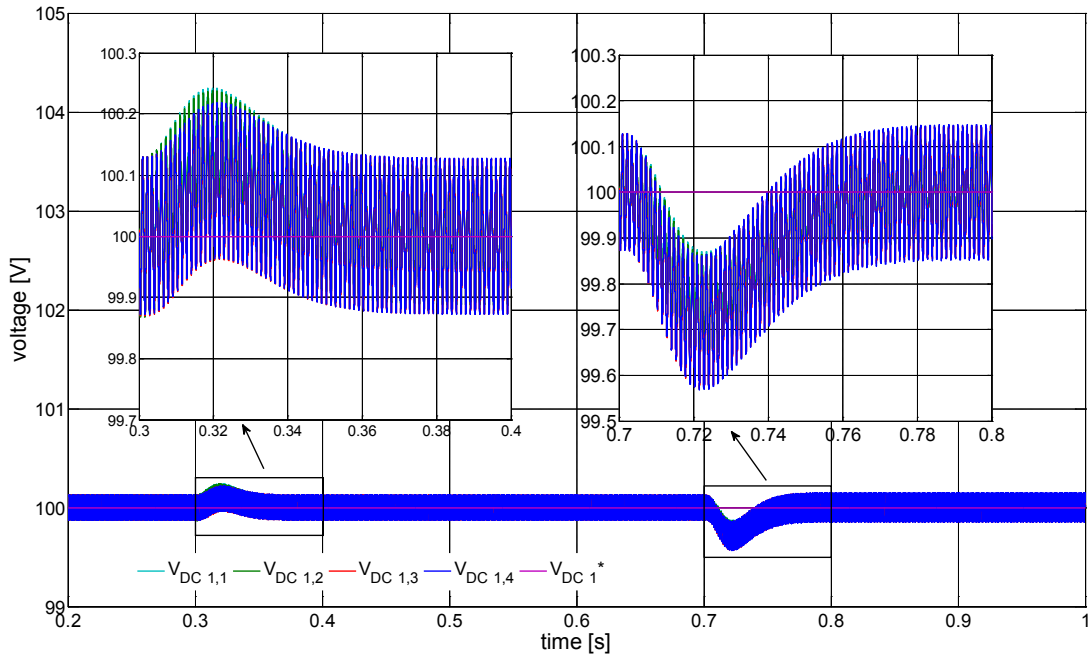


Fig. 3.13: SSBC MMCC DC-links voltages in case of 10% load reduction applied at the first load (bus 1 and bus 2) and in case of 10% load increase applied at the second load (bus 3 and bus 4) at different times.

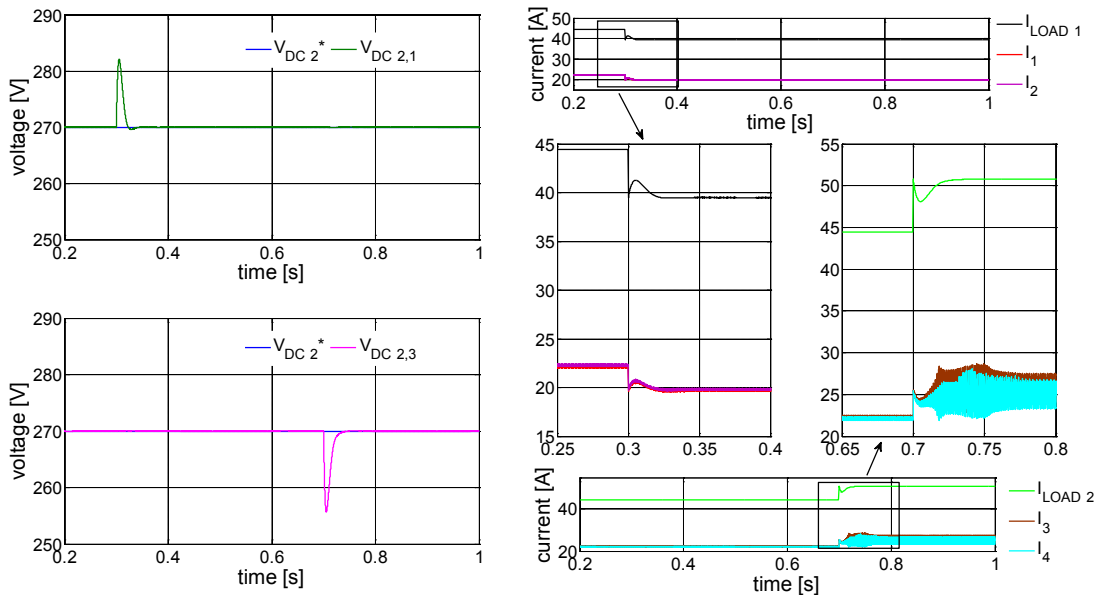


Fig. 3.14: DAB output voltages and currents in case of 10% load reduction applied at the first load (bus 1 and bus 2) and in case of 10% load increase applied at the second load (bus 3 and bus 4) at different times.

### 3.3.3 Frequency variations

The performances of the system have been investigated in case of fundamental frequency variations in the range 360-800 Hz. In Tab. 3.3 there listed the u-phase  $i_g$  current harmonic components, classified as in standard RTCA DO-160G. For all the considered frequencies, almost the totality of the components are in compliance with the same standard limits. The harmonics over the limits are marked in bold.

Tab. 3.3: Grid Current harmonic components for frequency varying from 360 to 800 Hz.

			$f_{sw}=10440\text{Hz}$	$f_{sw}=10000\text{Hz}$	$f_{sw}=10000\text{Hz}$	$f_{sw}=10200\text{Hz}$	$f_{sw}=10500\text{Hz}$	$f_{sw}=10400\text{Hz}$
	harmonic order	RTCA DO-160G Limits	$f=360\text{Hz}$	$f=400\text{Hz}$	$f=500\text{Hz}$	$f=600\text{Hz}$	$f=700\text{Hz}$	$f=800\text{Hz}$
	1		107.94	107.94	107.94	107.94	107.94	107.94
EVEN	2	$0.01 * I_l/2 =$ <b>0.54</b>	$\approx 0$	$\approx 0$	$\approx 0$	$\approx 0$	$\approx 0$	$\approx 0$
	4,6,8...40	$0.0025 * I_l =$ <b>0.269</b>	$\approx 0$	$\approx 0$	$\approx 0$	$\approx 0$	$\approx 0$	$\approx 0$
ODD TRIPLEN HARMONICS	3	$0.15 * I_l/3 =$ <b>5.40</b>	2.82	2.73	3.11	3.06	3.20	3.26
	9	$0.15 * I_l/9 =$ 1.800	1.25	1.24	1.21	1.22	1.03	1.32
	15	$0.15 * I_l/15 =$ <b>1.079</b>	0.46	0.39	0.60	0.19	0.67	0.23
	21	$0.15 * I_l/21 =$ <b>0.770</b>	0.57	0.38	0.57	0.23	0.13	0.07
	27	$0.15 * I_l/27 =$ <b>0.600</b>	0.24	0.29	0.25	0.10	0.27	<b>2.23</b>
	33	$0.15 * I_l/33 =$ <b>0.490</b>	0.23	0.11	0.01	<b>1.92</b>	0.12	0.26
	39	$0.15 * I_l/39 =$ <b>0.415</b>	0.07	0.19	<b>1.65</b>	0.08	0.19	0.11
ODD NON TRIPLEN HARMONICS	5	$0.3 * I_l/5 =$ <b>6.476</b>	1.38	1.37	1.46	1.28	1.45	1.04
	7	$0.3 * I_l/7 =$ <b>4.626</b>	1.07	1.20	0.95	0.95	0.68	0.67
	11	$0.3 * I_l/11 =$ <b>2.940</b>	1.14	0.10	1.34	1.11	1.31	1.44
	13	$0.3 * I_l/13 =$ <b>2.490</b>	0.73	0.59	0.97	0.52	0.93	0.73
	17	$0.3 * I_l/17 =$ <b>1.900</b>	0.15	0.29	0.21	0.28	0.41	0.09
	19	$0.3 * I_l/19 =$ 1.700	0.52	0.35	0.74	0.16	0.12	0.10
	23	$0.3 * I_l/23 =$ <b>1.400</b>	0.56	0.32	0.17	0.19	0.10	0.32
	25	$0.3 * I_l/25 =$ <b>1.295</b>	0.56	0.33	0.17	0.18	0.09	<b>2.47</b>
	29	$0.3 * I_l/29 =$ <b>1.116</b>	0.28	0.10	0.25	0.06	<b>2.10</b>	0.13
	31	$0.3 * I_l/31 =$ <b>1.046</b>	0.28	0.09	0.17	0.21	<b>1.92</b>	0.13
	35	$0.3 * I_l/35 =$ <b>0.925</b>	0.19	0.07	0.03	<b>1.77</b>	0.17	0.18
37	$0.3 * I_l/37 =$ <b>0.875</b>	0.14	0.12	0.18	0.07	0.29	0.15	
THD %			<b>3.73</b>	<b>3.53</b>	<b>4.19</b>	<b>4.35</b>	<b>4.67</b>	<b>4.9</b>

It should be noticed that, for these tests, also the switching frequency has been varied (around the value of  $10\text{kHz}$ ) in order to guarantee an integer ratio  $R$  between the switching frequency and the fundamental frequency. It is verified that the lowest harmonic sideband is centered at  $2Hf_{sw\_SSBC}$  and that the very few harmonics over the limits are always located at  $2R\pm 1$ .

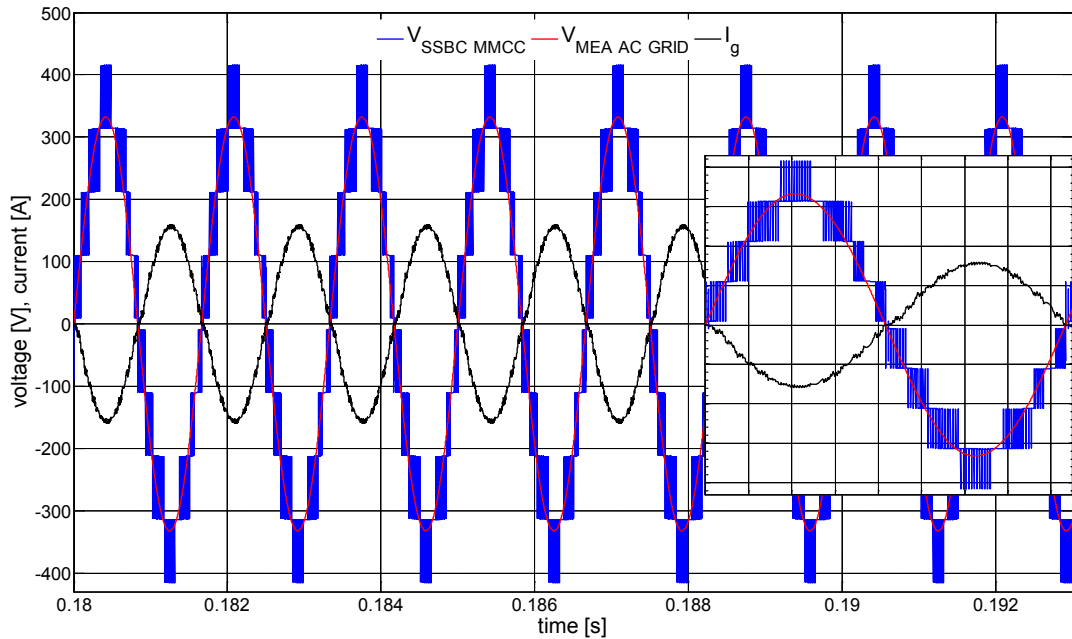


Fig. 3.15: MEA AC voltage, 9-levels voltage of the SSBC MMCC, AC current in case  $f=600\text{ Hz}$ .

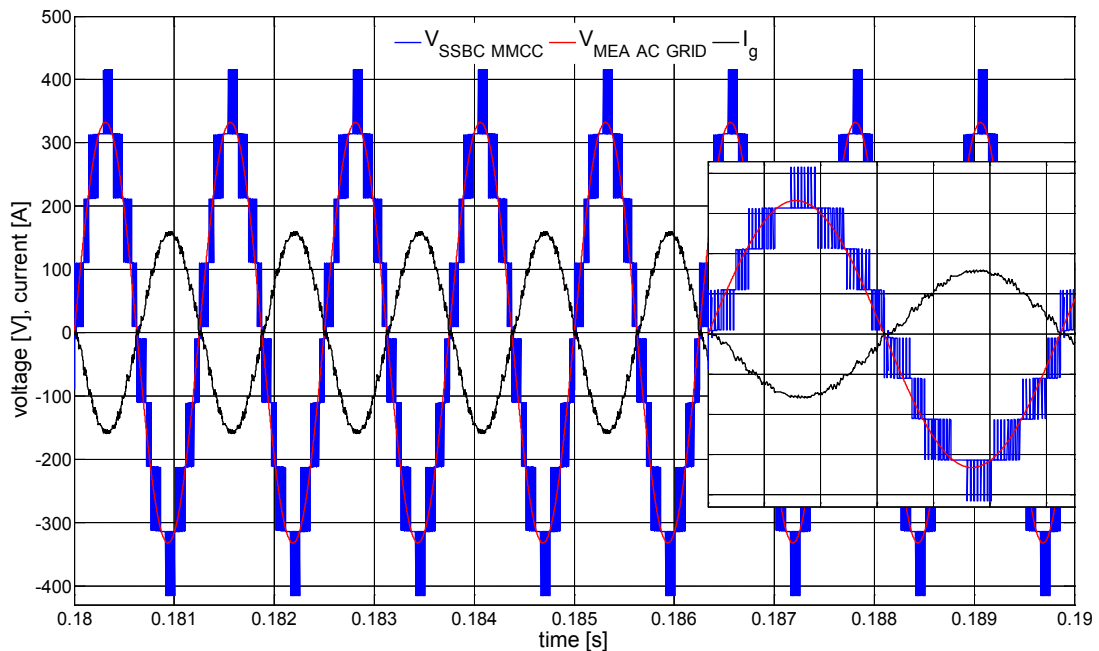


Fig. 3.16: MEA AC voltage, 9-levels voltage of the SSBC MMCC, AC current in case  $f=800\text{ Hz}$ .

Some selected results related to the 9-levels voltage waveform of the MMCC SSBC, the MEA AC grid voltage and the AC current, in case the fundamental frequency is equal to 600 Hz and 800 Hz, are shown respectively in Fig. 3.15 and Fig. 3.16.

An advanced active rectifier for a MEA has been proposed in this Chapter. It is based on a SSBC MMCC consisting of four single-phase H-Bridge cells for each phase. The system is coupled to four DAB converters providing output voltage equal to 270V in compliance with the aircraft standards. The proposed topology exhibits high power quality performances since the power conversion stage operation is characterized by a virtual switching frequency of 80kHz in case of rated conditions ( $f=400$  Hz). High performances are guaranteed also in case of load variations and frequency variations in the range 360-800 Hz.

### 3.4 270V/28V DAB for Onboard MEA Applications

Due to the continuous increase of electric power installed on-board, the new MEA adopts a  $\pm 270V$  power distribution standard providing advantages in terms of weight reduction [13].

Higher voltages match with lower currents and, as a consequence, cables size reduction. However some equipments in MEA still require low-voltage supply at 28V. It implies the need of DC/DC power conversion stages designed to comply with this voltage constraint and to achieve high efficiency.

Besides high efficiency, high power density is another of the main goals related to the power generation and distribution in MEA. As a consequence, the number of the power conversion stages has to be reduced at the least in order to reach this target. Isolated DC/DC converters topologies can provide the required high voltage gain: 270V/28V. However isolated DC/DC converters are characterized by lower efficiency than non-isolated DC/DC converters due to transformer and inductance losses and high number of power devices.

A harsh environment often characterizes the power converters for MEA due to close integration with the electrical machines. Since cooling systems and passive components

are major portions of the volume, demands for low losses and high-switching-frequency power devices are increasing to achieve the higher power density.

In this scenario wide bandgap power devices, characterized by high thermal durability at high temperature, represent the new frontier for MEA applications. The use of wide bandgap power devices in isolated DC/DC converters can also contribute to improve the efficiency and the power density thanks to low switching losses. Both GaN and SiC devices are promising technologies but GaN rated currents are currently lower than SiC. Hence, at present SiC devices result more proper than GaN for MEA applications.

Silicon carbide (SiC) power devices have been actively developed as next-generation power devices owing to their superior performances compared to those of Si ones, as shown in Fig. 3.17; in particular:

- the higher breakdown field leads to lower on state resistance and higher blocking voltage;
- the higher thermal conductivity improves heat spreading and increases power density, because it improves power dissipation;
- the higher saturation velocity allows very high switching frequency;
- the wide band gap (which means that more energy is needed to excite electrons from the valence band into the conduction band) leads to lower leakage currents and high thermal durability operating at high temperature (above 200°C) [14]-[15].

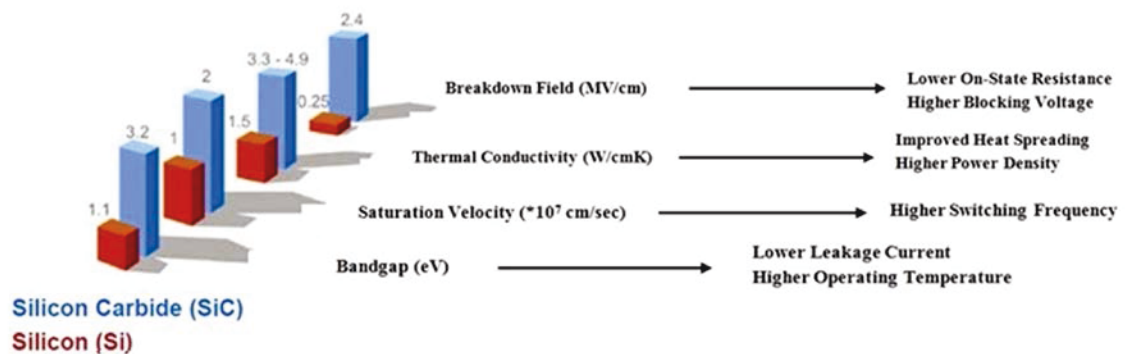


Fig. 3.17: Silicon and Silicon Carbide features comparison

The use of SiC power devices allows realizing highly compact converters with low conduction and switching losses. The conduction losses of the SiC devices depend on

the chip area, consequently the efficiency comparison between SiC and Si devices should be also dependent on the chip area. The low switching losses of the Silicon Carbide components enable power converters to operate at higher switching frequencies and higher junction temperatures. Operating at high switching frequencies enables to reduce volume and weight of passive component. Higher switching frequencies with lower switching losses are particularly advantageous for DC/DC converters since they allow to reduce the size of the inductor and High Frequency Transformers in case of isolated topologies, as DAB converters.

As previously discussed, the thermal conductivity is another property that contributes to the superior thermal performances of SiC devices. The relationship between the thermal resistance  $R_{th\_jc}$  (junction to case) and the material thermal conductivity  $\lambda$  is:

$$R_{th\_jc} = \frac{d}{\lambda A} \quad (3.19)$$

where  $d$  is the length and  $A$  is the cross-section area of the SiC power device. From this equation, it can be noticed that SiC higher thermal conductivity gives the devices a lower thermal resistance. The heat generated at the junction during the switching, can be easily transmitted to the case and the junction temperature will rise more slowly. Consequently, both the slowing rising junction temperature and the high thermal durability lead to the overwhelming performance of SiC device over Si ones [16].

Operating at high junction temperature helps reducing size and weight of the cooling system or even enables the use of natural cooling system instead of liquid cooling system. Hence SiC are preferred for harsh environment applications.

Among SiC power devices, SiC MOSFETs have become recently widely available and some of their advantages have been already demonstrated. Because of the higher doping and current densities of SiC material, the SiC MOSFETs have smaller area and capacitance; therefore they are more efficient than Si MOSFETs. Fig. 3.18 shows the equivalent schematic model of the SiC MOSFET. It reveals that three variable capacitances appear on the MOSFET model. The switching performance of the MOSFET transistor is determined by how quickly the voltages can be changed across

these capacitors. Therefore, in high speed switching applications, the most important parameters are the parasitic capacitances of the device. The variable gate capacitances set the gate requirement to deliver a dynamic charge during the turn-on and rapidly remove this charge to ensure a fast turn-off process. Unlike SiC JFET, there is no requirement for the on-state current for the gate of SiC MOSFET, since the gate is isolated.

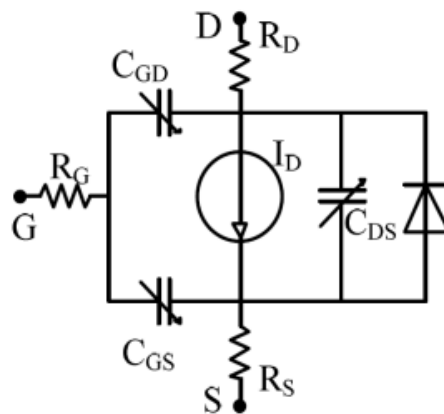


Fig. 3.18: Equivalent schematic model of the SiC MOSFET.

The present study is focused on SiC DAB converter performance optimization, based on a different modulation technique and based on a proper choice of the adopted power devices. Starting from the analysis of the power devices currently available on the market, the feasibility of the proposed topology is proven. In order to evaluate the power dissipation in a semiconductor device, a controllable switch is connected in the simple circuit shown in Fig. 3.19.

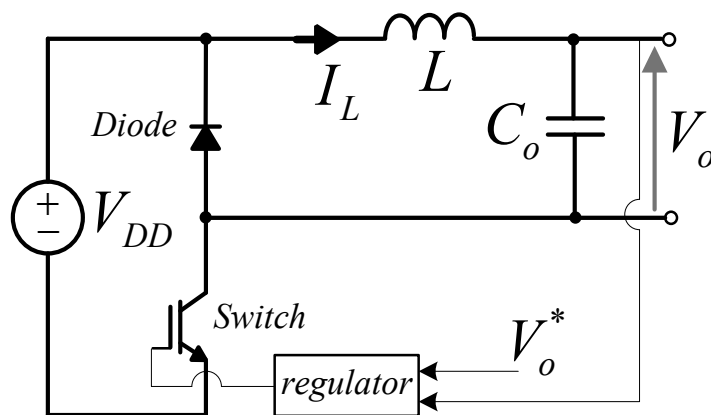


Fig. 3.19: Switch-mode DC power supply.

This circuit models a very commonly encountered situation in power electronics; the current flowing through a switch also must flow through some series inductance(s). The diode is assumed to be ideal because the focus is on the switch characteristics, though in practice the diode reverse-recovery current can significantly affect the stresses on the switch [17].

Fig. 3.20 shows the waveforms of the current through the switch and the voltage across the switch when it is being operated at  $T$  switching time period. The switching waveforms are represented by linear approximations to the real waveforms in order to simplify the discussion. When the switch has been off for a while, it is turned on by applying a positive control signal to the switch. During the turn-on transition, the current buildup consists of a short delay time  $t_{d(on)}$  followed by the current rise time  $t_{ri}$ . Only after that the current  $I_L$  flows entirely through the switch can the diode become reverse biased and the switch voltage falls to a small on-state value of  $V_{on}$  with a voltage fall time of  $t_{fv}$ . The waveforms in Fig. 3.20 indicate that large values of switch voltage and current are present simultaneously during the turn-on crossover interval  $t_{c(on)}$ . The energy dissipated in the device during this turn-on transition can be approximated with the left grey area:

$$W_{C(on)} = \frac{1}{2} V_{DD} I_L t_{c(on)} \quad (3.20)$$

Once the switch is fully on, the on-state voltage  $V_{on}$  will be on the order of a volt or so depending on the device, and it will be conducting a current  $I_L$ . The switch remains in conduction during the on interval  $t_{on}$ , which in general is much larger than the turn-on and turn-off transition times. The energy dissipation  $W_{on}$  in the switch during this on-state interval can be approximated as:

$$W_{on} = V_{on} I_L t_{on} = I_L^2 R_{DS(on)} t_{on} \quad (3.21)$$

where  $R_{DS(on)}$  is the resistance of channel in the on-state, and it is an important parameter because it determinates the voltage drop across the device and conduction losses. The value of  $R_{DS(on)}$  depends from the junction temperature  $T_j$  and from the value of  $V_{GS}$ .

In order to turn the switch off, a zero control signal is applied to the gate of the switch. During the turn-off transition period, the voltage build-up consists of a turn-off delay time  $t_{d(off)}$  and a voltage rise time  $t_{rv}$ . Once the voltage reaches its final value of  $V_{DD}$ , the diode can become forward biased and begin to conduct current. The current in the switch falls to zero with a current fall time  $t_{fi}$  as the current  $I_L$ , commutates from the switch to the diode. Large values of switch voltage and switch current occur simultaneously during the crossover interval  $t_{c(off)}$  and the energy dissipated in the switch during this turn-off transition can be calculated as:

$$W_{C(off)} = \frac{1}{2} V_{DD} I_L t_{c(off)} \quad (3.22)$$

The goal is to reduce the losses by acting with soft switching.

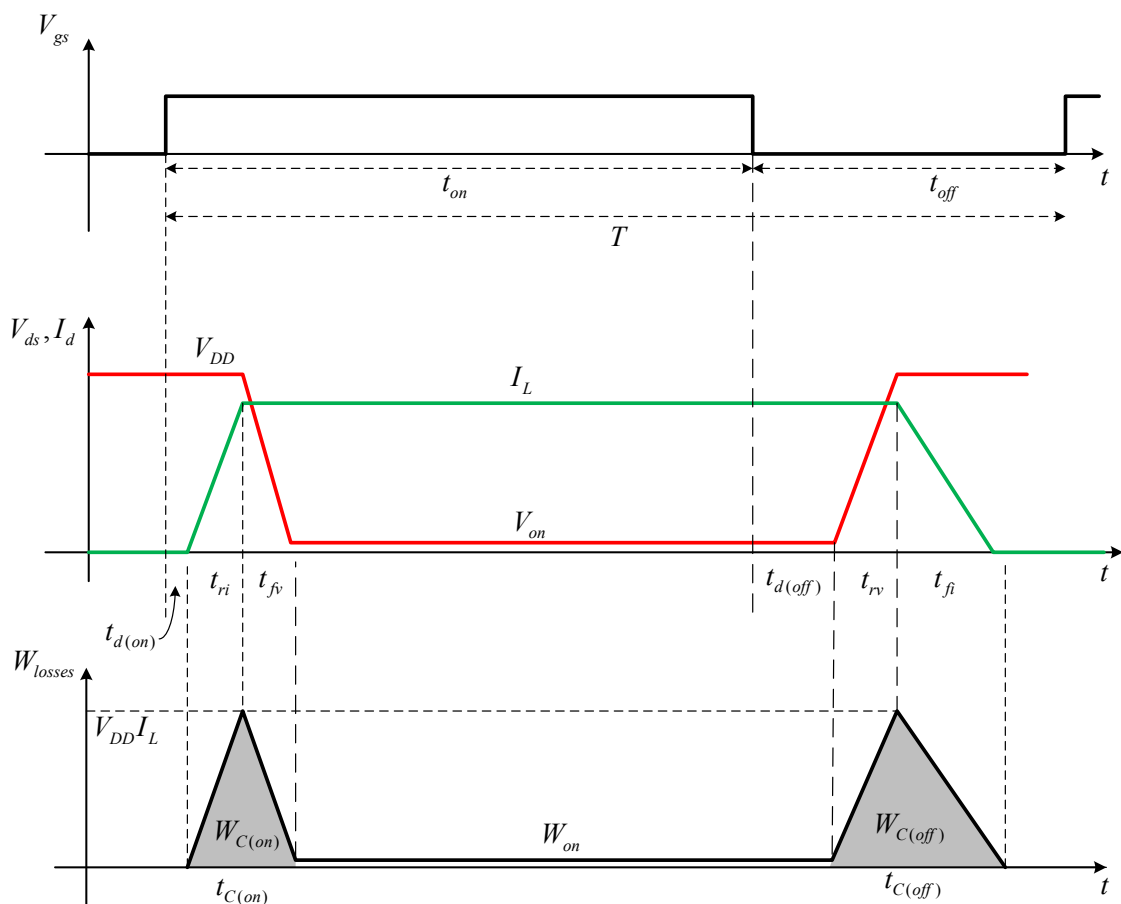


Fig. 3.20: Switching characteristics (linearized): simplified clamped inductive-switching circuit, switch waveforms, instantaneous switch power loss.

In order to study the efficiency of the proposed 270V/28V DAB in case of varying operating temperatures, in case of different modulating techniques and different MOSFETs (SiC or/and Si), a thermal model of the switches has been implemented in PLECS simulation. PLECS is qualified for thermal analysis and switching/conducting losses estimation in high-speed system-level simulation. Instead of determining semiconductor switching losses from current and voltage transients, PLECS records the semiconductor's operating condition (forward current, blocking voltage, junction temperature) before and after each switch operation. It then uses these parameters to read the resulting dissipated energy from a 3D look-up table. During the on-state, the dissipated power is computed from the device current and temperature. The required data tables are entered via PLECS' integrated visual editor.

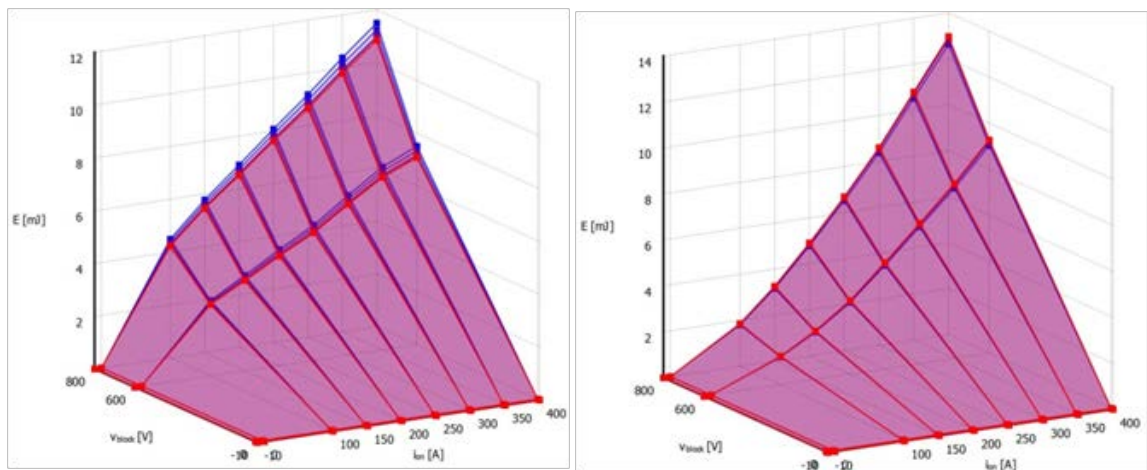


Fig. 3.21: Wolfspeed CAS300M12BM2 turn-on (right) and turn-off (left) losses at different  $T_j$ .

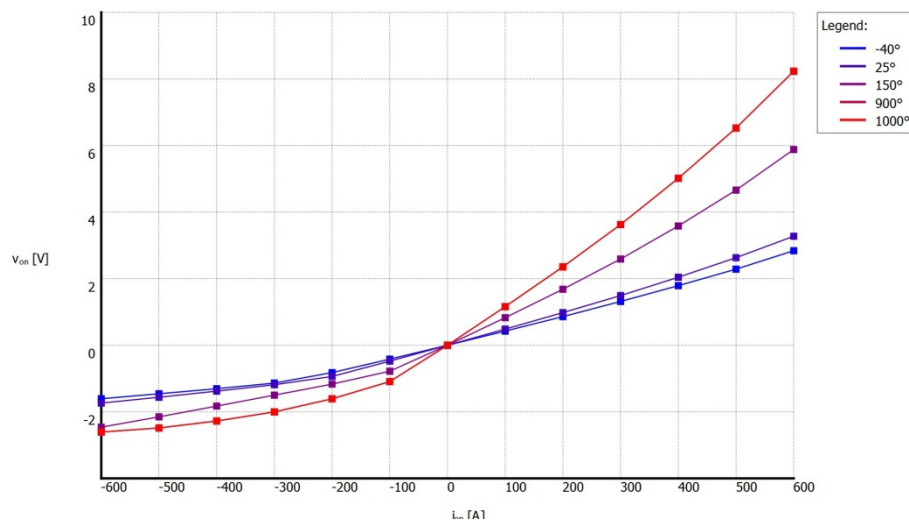


Fig. 3.22: Wolfspeed CAS300M12BM2  $V_{ON} - i_{ON}$  characteristics at different  $T_j$ .

In Fig. 3.21 are represented the turn-on and turn-off 3D look-up-tables of the SiC CAS300M12BM2 MOSFET (SiC MOSFET candidate for aerospace DAB) at different junction temperatures  $T_j$ . The three dimensions ( $X, Y, Z$ ) are respectively the ON-current  $i_{ON}(A)$ , the blocking voltage  $V_{block}(V)$  and the losses energy  $E(mJ)$ . In Fig. 3.22 are represented the  $V_{ON}-i_{ON}$  characteristics of CAS300M12BM2 at different  $T_j$ . These diagrams are necessary to evaluate the conduction losses in all the operative area of the semiconductor. When the manufacturing datasheet does not include the before specified data tables, the best way to derive them it is the software implementation of the Double Pulse (DBP) test in PSpice environment. This software is the most appropriate simulation environment when power devices switching transients must be taken into account; in this case the power devices models are achieved by fitting simulated data with static and dynamic characterization results. An example of DBP test is represented in Fig. 3.23, where the Device Under Test (DUT) is the Si AUIRLB3036 MOSFET (Si MOSFET candidate for aerospace DAB).

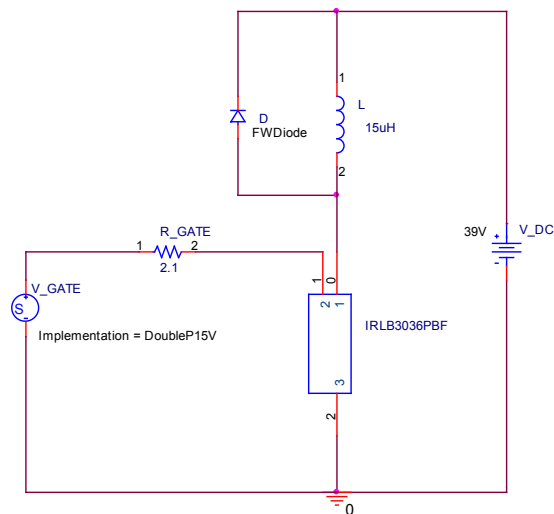


Fig. 3.23: DBP Test circuit, with IRLB3036 as DUT in PSpice.

The DBP test is the best method to analyze the switching characteristics and basically it is based on an inductive load buck converter consisting of the DUT and one freewheeling diode (Fig. 3.23). A two-pulse train of amplitude 15V is sent to the gate of the DUT as shown in Fig. 3.24 with the blue line. The first pulse is used to build up the current in the inductor and its width is adjusted for the desired drain current  $I_D$

(indicated in figure with the green line,  $I_D=130A$ ). At the end of this pulse,  $I_D$  commutates from the MOSFET to the freewheeling diode, while the drain-source voltage  $V_{DS}$  (indicated in figure with the red line) increases from zero to its steady-state value of  $39V$ . This transition is used to measure the MOSFET turn-off characteristics (Fig. 3.25). There is a delay between the first and second pulse, whose duration is set long enough for the voltage and currents to settle out. When the second narrow pulse occurs, current is commutated from the freewheeling diode back into the MOSFET and its turn-on characteristics are measured at this time (Fig. 3.26). The high-side freewheeling diode used in the simulations is an ideal diode with fast reverse recovery effect, thus limiting the MOSFET current spike at the turn-on.

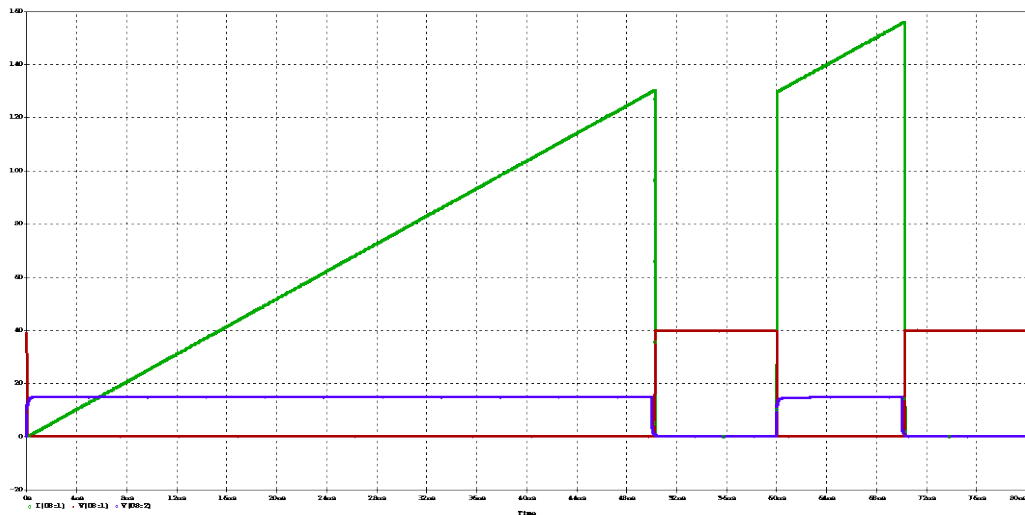


Fig. 3.24: AUIRLB3036 DBP test- typical switching waveforms,  $I_D = 130A$ ,  $V_{GS} = 15V$ ,  $V_{DD} = 39V$ .

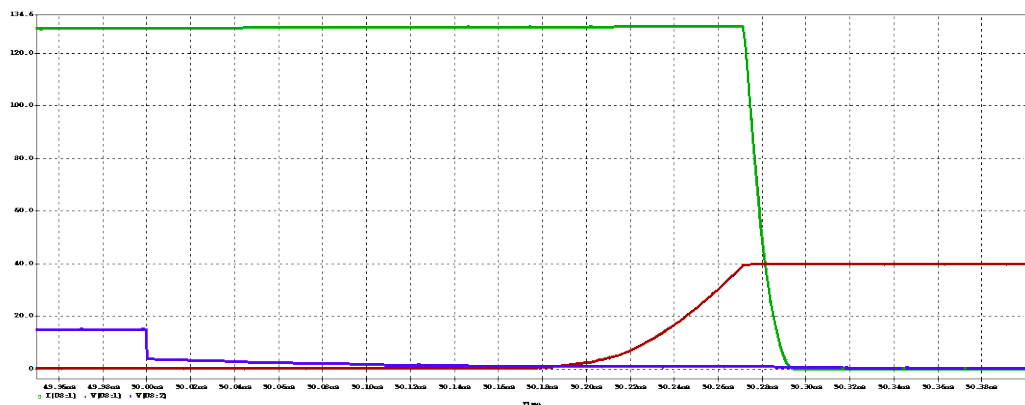


Fig. 3.25: AUIRLB3036 MOSFET turn-OFF characteristics,  $I_D = 130A$ ,  $V_{GS} = 15V$ ,  $V_{DD} = 39V$ .

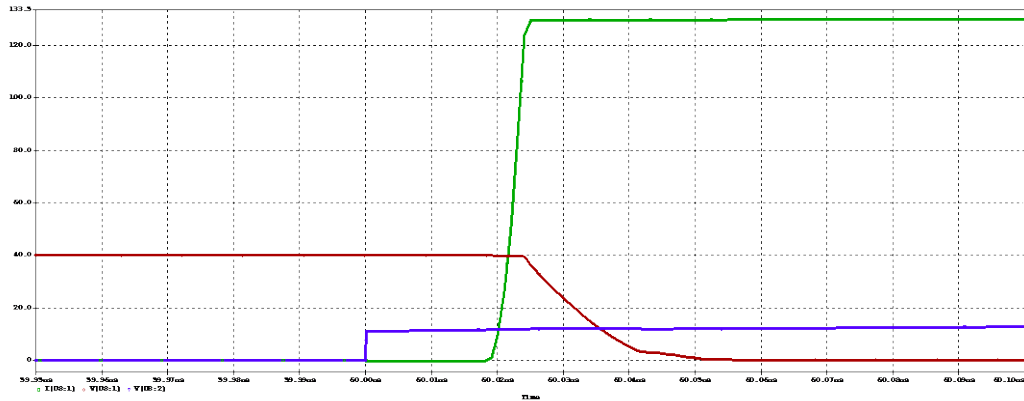


Fig. 3.26: AUIRLB3036 MOSFET turn-ON characteristics,  $I_D = 130\text{A}$ ,  $V_{GS} = 15\text{V}$ ,  $V_{DD} = 39\text{V}$ .

Under the condition of clamped inductive load shown in Fig. 3.23, the load inductance is sufficient enough to maintain a nearly constant load current throughout the switching cycle: this means, during the MOSFET switching transients, the load inductor current keeps unchanged, while the switching current commutates from MOSFET to the freewheeling diode during the MOSFET turn-off, or the opposite during the MOSFET turn-on. Si MOSFET switching behaviors have been tested in order to derive the  $E_{ON}$  and  $E_{OFF}$  switching losses at different  $I_D$  current values. The  $E_{ON}$  and  $E_{OFF}$  switching losses of the AUIRLB3036 at  $T_j = 25^\circ$ ,  $V_{block} = 39\text{V}$  and in the current range of  $0 \div 200\text{A}$  are reported in Fig. 3.27. PLECS uses linear interpolation to derive the complete 3D look-up table in correspondence of blocking voltage values in the range  $0 \div 39\text{V}$ . In Fig. 3.28 are represented the  $V_{ON}$ - $i_{ON}$  characteristics of AUIRLB3036 at  $T_j = 25^\circ$  and  $T_j = 175^\circ$ .

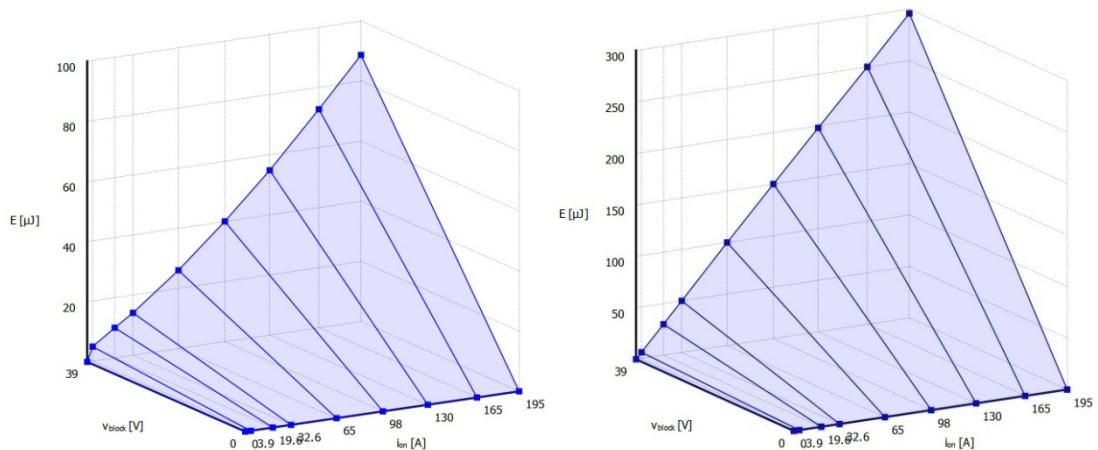


Fig. 3.27: IR AUIRLB3036 turn-on (left) and turn-off (right) losses at  $T_j = 25^\circ$ .

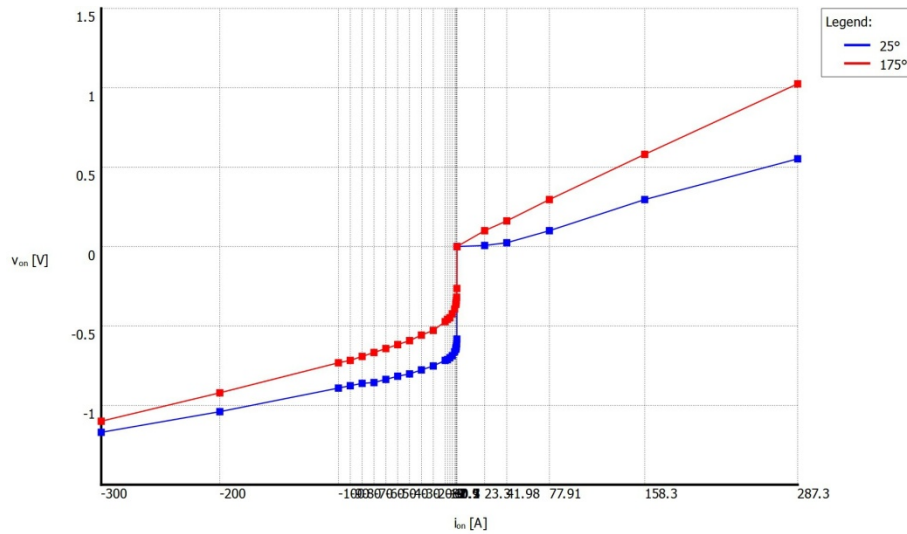


Fig. 3.28: IR AUIRLB3036  $V_{ON}$ - $i_{ON}$  characteristics at  $T_j = 25^\circ$  and  $T_j = 175^\circ$ .

The DAB converter can be used also to achieve a 270V/28V SiC MOSFET DC/DC converter for MEA applications as depicted in Fig. 3.29.

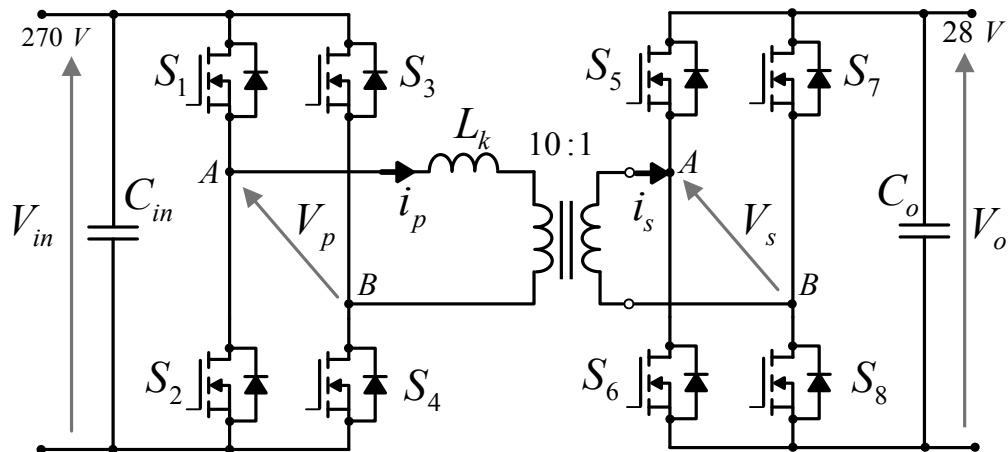


Fig. 3.29: 270V/28V aerospace DAB converter.

In the DAB converter the power exchanged between the bridges denoted as  $H_1$  and  $H_2$  (Fig. 3.29) is defined as:

$$P_{DAB} = \frac{nV_{in} V_o \varphi(1-\varphi)}{2L_k f_{sw}} \quad n = 10 \quad (3.23)$$

where  $L_k$  is the overall inductance (which includes the equivalent inductance of the transformer),  $f_{sw}$  is the switching frequency,  $n$  is the transformer turns ratio and  $\varphi$  is the phase shift angle between the two AC voltages  $V_p$  and  $V_s$ .

The standard Phase Shift Modulation (PSM) is the most used technique for DAB converters [18] and it has been described in Chapter II. Simplicity is the main advantage of PSM, but it implies also some disadvantages such as limited Zero Voltage Switching (ZVS) range at light load and high reactive current circulation in the same condition. In particular, in case of significant power variations respect to the rated power or wide voltage variations in input or in output, these effects are not negligible and the performances of the DAB converter are degraded [19]. In order to optimize the performance of the proposed DAB converter alternative modulation techniques can be applied. In this particular case-study Trapezoidal Modulation (TM) is investigated aiming to reduce the switching losses thanks to ZVS and Zero Current Switching (ZCS) operation. Both names imply that either voltage or current within the transistor is zero before switching occurs [20].

- For ZVS, the transistor will be turned in at zero  $V_{DS}$  voltage to reduce the turn on switching loss (Fig. 3.30)
- For ZCS, the transistor will be turned off at zero  $I_{DS}$  current to reduce the turn off switching loss (Fig. 3.30).

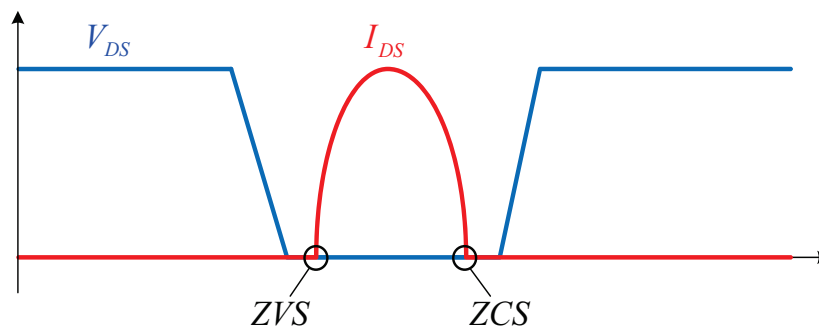


Fig. 3.30: Soft switching “MOSFET” current and voltage waveform

In case of TM, the two legs of each H-Bridge of the DAB converter are driven independently in order to generate a three-levels voltage waveform as in Fig. 3.31. In particular the two AC voltages  $V_p$  and  $V_s$  (at the primary and the secondary side of the transformer) are two quasi-square waves. Hence the 0-level in the voltage waveforms allows to control the current zero-crossing and the current slope. Assuming a constant duty cycle  $d=0.5$ , the TM implementation is represented in Fig. 3.31 where the

difference between a sawtooth carrier and the modulating signal is evaluated by a comparator.

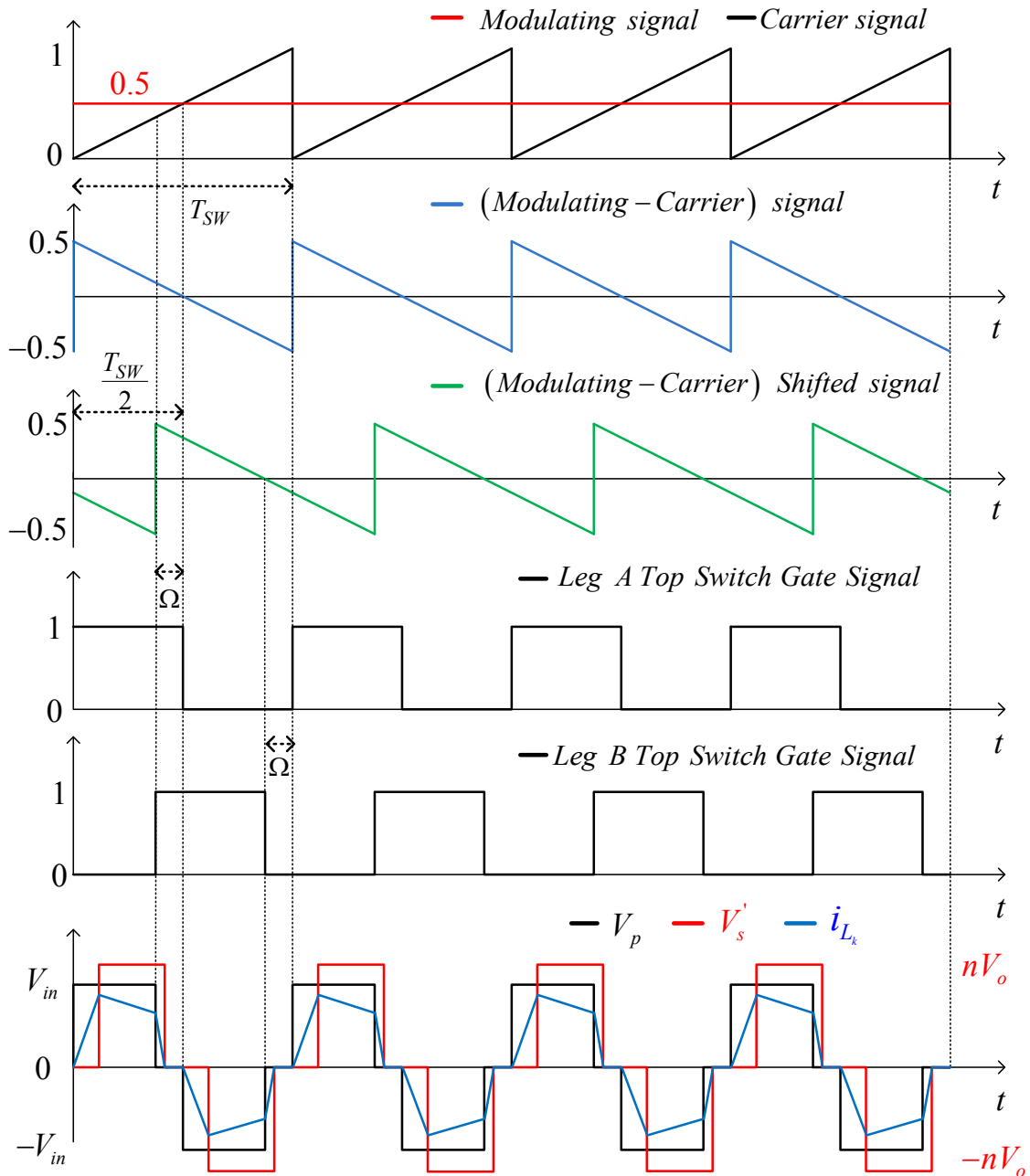


Fig. 3.31: DAB – HFT three level voltage waveform.

Considering the power stage parameters reported in Tab. 3.4, the gate signals and the AC voltages and currents at the primary and the secondary side, in case of TM, are depicted in Fig. 3.32 – Fig. 3.33. The difference signal is used to drive the top switch of

the leg A when it is greater than zero. The gate signal of the leg B top switch is phase-shifted of  $[(T_{sw}/2) - \Omega]$ , where  $\Omega$  sets the 0-level duration. Adjusting  $\Omega$  it is possible to modify  $V_p$  and  $V_s$  in order to ensure ZVS and ZCS operations. As a consequence, Soft Switching (SW) operation is achieved. The  $i_p$  and  $i_s$  currents waveforms result trapezoidal and the current zero-crossing occurs when both  $V_p$  and  $V_s$  are null.

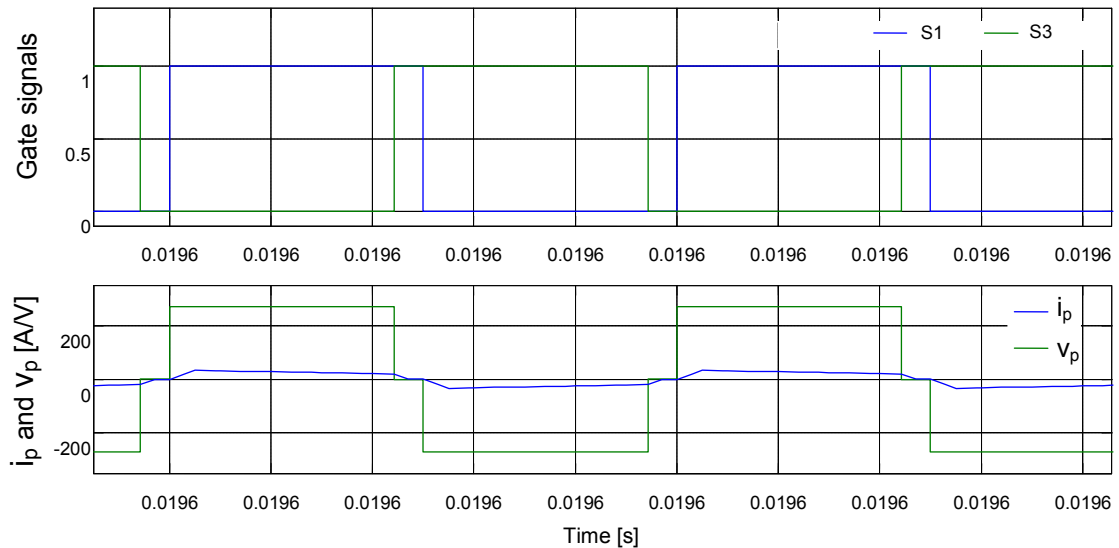


Fig. 3.32: Gate signal of the switches  $S_1$  and  $S_3$ , AC voltage and current at the primary side in TM.

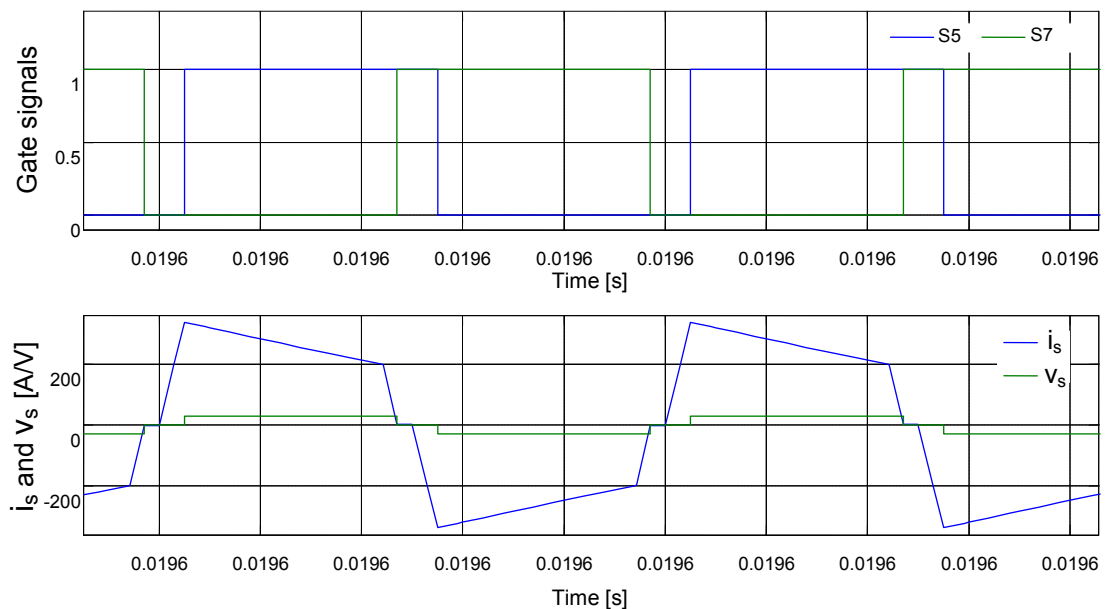


Fig. 3.33: Gate signal of the switches  $S_5$  and  $S_7$ , AC voltage and current at the secondary side in TM.

The MOSFETs couples  $S_1$ - $S_2$  and  $S_7$ - $S_8$  operate with ZVS and ZCS, also in case of power variation respect to the rated value, as shown in Fig. 3.34. Hence no switching

losses are associated to  $S_1$ ,  $S_2$ ,  $S_7$  and  $S_8$  both in turn-on and in turn-off for the entire switching period. In Fig. 3.34, the particular case of  $S_7$  is represented with the correspondent drain-source current  $I_{DS}$  and voltage  $V_{DS}$  when TM is used.

Tab. 3.4: 270V/28V DAB Power Stage Parameters.

<i>Symbol</i>	<i>Description</i>	<i>Value</i>
$V_{in}$	Input DC Voltage	270 V
$V_o$	Output DC Voltage	28 V
$L_k$	Leakage Inductance	10 $\mu H$
$n$	Transformer turns ratio	10
$C_o$	Output DC Capacitor	450 $\mu F$
$R_o$	Passive Load	12.5 $\Omega$
$f_{sw}$ DAB	DAB Switching Frequency	40/60 kHz
$P_n$	Nominal Power	4 kW

When  $S_7$  is turned on, the current is zero, and no switching losses are produced; during all the ON state, the current  $I_{DS}$  is negative and flows through body-diode; during the turn off, the current  $I_{DS}$  across the zero value without switching losses. For the couples  $S_3$ - $S_4$  and  $S_5$ - $S_6$  the switching losses depend on the sign of the current which circulates inside them during the turn-off. In Fig. 3.35, during the turn-on the current of the switch  $S_5$  flows through the antiparallel-body diode and ZVS occurs; during the turn-off the  $S_5$  current flows through the MOSFET and not null switching losses are verified.

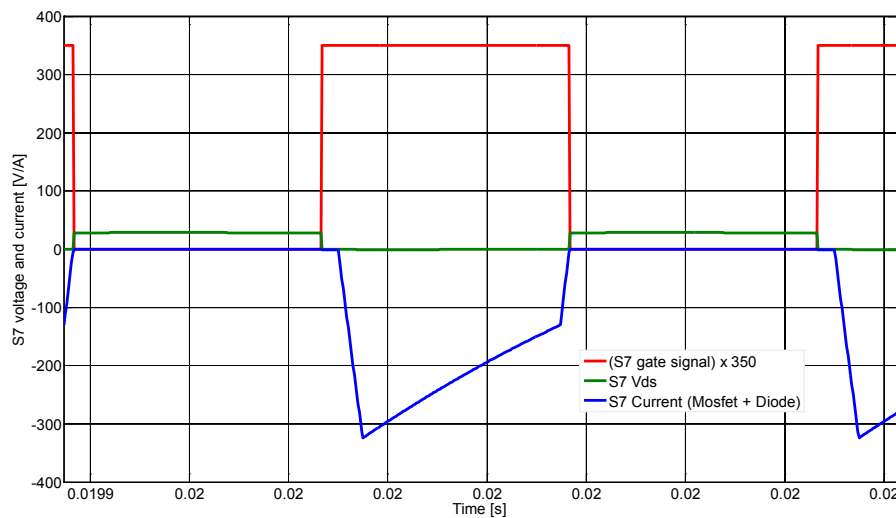


Fig. 3.34:  $S_7$  Gate signal, drain-source voltage and current in case of TM.

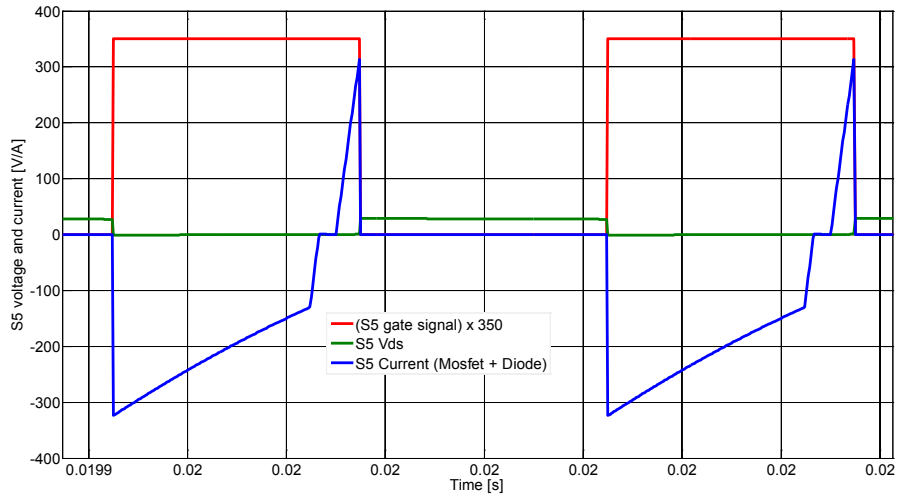


Fig. 3.35: S<sub>5</sub> Gate signal, drain-source voltage and current in case of TM.

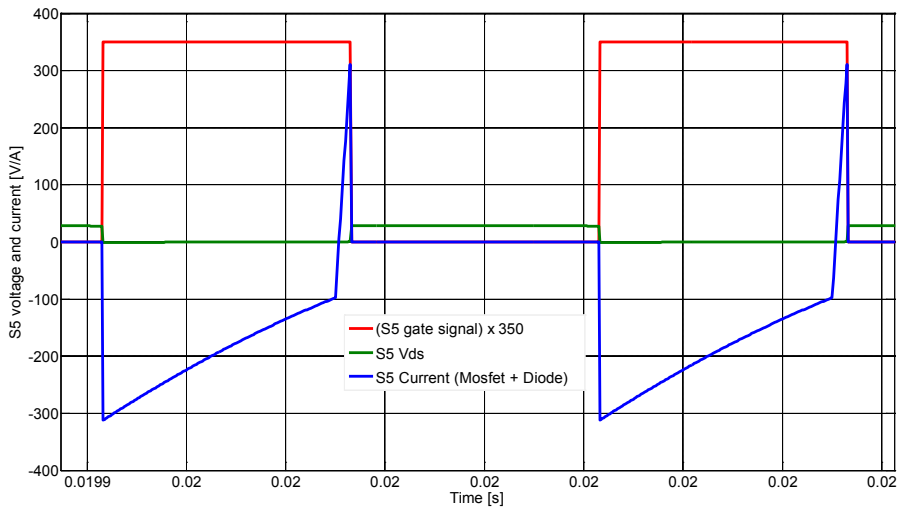


Fig. 3.36: S<sub>5</sub> Gate signal, drain-source voltage and current in case of PSM.

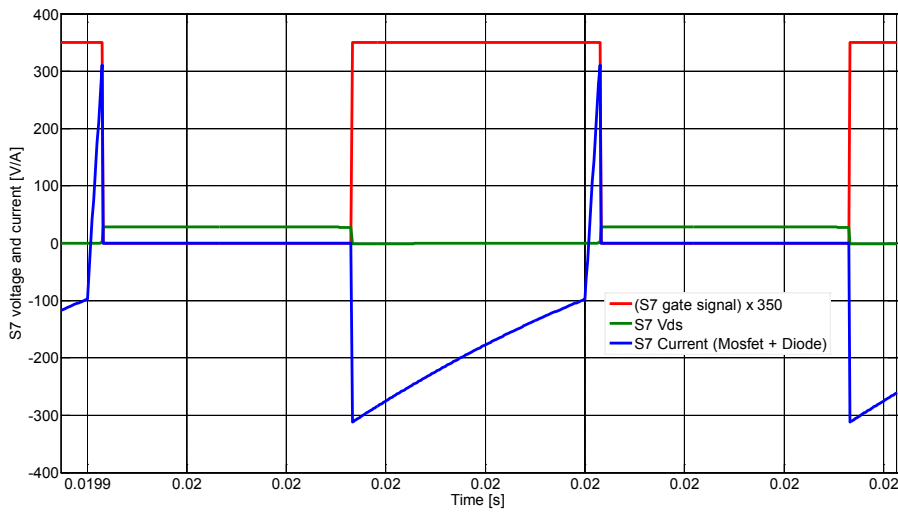


Fig. 3.37: S<sub>7</sub> Gate signal, drain-source voltage and current in case of PSM.

In Fig. 3.36 – Fig. 3.37, the particular case of MOSFET  $S_5$  and  $S_7$  is represented with the correspondent drain-source current  $I_{DS}$  and voltage  $V_{DS}$ , when the PSM is used. When  $S_5$  or  $S_7$  are turned on, the current  $I_{DS}$  is negative and flows through body-diode without switching losses; during the turn off, a current  $I_{DS}$  flows through the MOSFET and no null switching losses are verified. Comparing both the PSM and the TM in terms of switching losses, those of PSM are double respect to TM. Tab. 3.5 highlights the most important differences between PSM and TM at different power conditions.

Tab. 3.5: DAB converter operation with PSM and TM.

		PSM				TM			
		H1		H2		H1		H2	
POWER	4 kW	Turn ON	ZVS	Turn ON	ZVS	Turn ON	ZVS	Turn ON	ZVS
		Turn OFF	$\neq 0$	Turn OFF	$\neq 0$	Turn OFF	ZCS for $S_1$ and $S_2$	Turn OFF	ZCS for $S_7$ and $S_8$
	2 kW	Turn ON	$\neq 0$	Turn ON	ZVS	Turn ON	ZVS	Turn ON	ZVS
		Turn OFF	ZCS	Turn OFF	$\neq 0$	Turn OFF	ZCS for $S_1$ and $S_2$	Turn OFF	ZCS for $S_7$ and $S_8$

A preliminary design of the 270V/28 V SiC MOSFET DAB converter has been presented in [21], however in [21] parallel connection of several SiC MOSFETs is assumed for the Low Voltage (LV) side H-Bridge in order to fulfill the rated current. Parallel connection of several MOSFET should be avoided in order to reduce the volume of the overall converter and also to increase the efficiency. Besides, due to some light differences among the MOSFETs overloads can be experienced.

Avoiding the MOSFETs parallel connection, no wide bandgap power device, currently available on the market, satisfies current specifications of the DAB LV-side H-Bridge apart from the SiC CAS300M12BM2 device ( $I_D @ 100^\circ\text{C} = 285 \text{ A}$ ) produced by CREE.

Alternative solutions rely on the use of high performance Si MOSFETs for the H-Bridge connected to the transformer LV-side and SiC MOSFETs at the primary side. In fact the rated current at the primary side (HV side) is fully covered by several SiC

power devices available on the market. Among the Si MOSFETS, the automotive qualified AUIRLB3036 device, produced by International Rectifier, matches the LV-side H-bridge current requirement.

The model of the 270V/28V SiC MOSFET DAB converter has been developed through PLECS to emulate the real and detailed characteristics of Si and SiC MOSFETs on the basis of their datasheets. The performances of the system have been tested both in case of PSM and TM. The performances of the DAB converter have been compared in case it is built with SiC MOSFETs for both the primary and the secondary side and in case Si MOSFETs are used for the LV-side H-Bridge.

If the 270V/28V DAB converter is all-based on SiC CAS300M12BM2 MOSFETs, the performances in terms of efficiency are summarized in Fig. 3.38, where two different values of the case temperature,  $T_{case}$ , are considered: 50°C and 100°C respectively. The efficiency is measured considering a fixed switching frequency  $f_{sw} = 40 \text{ kHz}$  and varying the required power and the modulation technique. It can be observed that negligible efficiency variations are registered moving from 50°C to 100°C due to optimal thermal durability of SiC MOSFETs. If the load power is comparable to the converter rated power, the efficiency is almost the same in case of TM and PSM while significant improvements are verified for light loads when TM is applied instead of PSM.

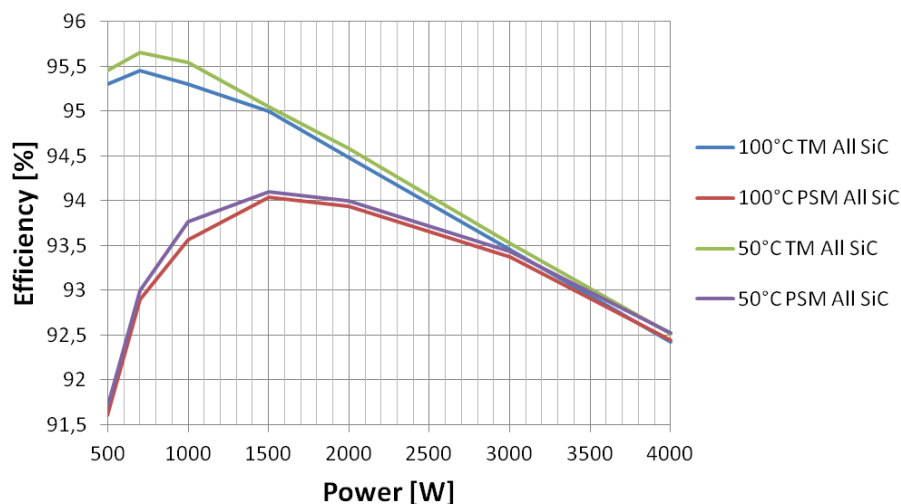


Fig. 3.38: All-SiC MOSFETs DAB converter: efficiency at different load powers and case temperatures in case of TM and PSM.

In Tab. 3.6 – Tab. 3.7 the measured losses are report in details and it can be noticed that TM allows high reduction of the switching losses respect to PSM due to SW operation. The switching losses in TM are about half respect to the switching losses in case the PSM is adopted. However, at the rated power, conduction losses are dominant respect to the switching losses and not significant improvements can be appreciated. It is also due to higher RMS current values associated to the TM respect to the PSM. If the load power is low (e.g.,1 kW), an increase up to 2.5% of the efficiency is obtained.

Tab. 3.6: Performance of the DAB converter based on SiC MOSFETs CAS300M12BM2 and TM for  $f_{sw}=40$  kHz ( $R_{dsON} = 6.5$  m $\Omega$ ,  $T_{case} = 100^{\circ}\text{C}$ ).

$P_{LOAD}$ (kW)	$\mu$ (%)	H1 SL (W): Leg A	H1 SL (W): Leg B	H2 SL (W): Leg A	H2 SL (W): Leg B	H1 CL(W)	H2 CL (W)	Total losses (W)	H2 $I_{RMS}$ (A)	H2 $T_J(^{\circ}\text{C})$
4	92.42	0.152	2.474	25.7	0.08	5.526	294.22	328.1	183.48	106.2
3	93.45	0.063	1.147	19.45	0.17	3.114	186.48	210.4	142.2	104.1
2	94.48	0.103	0.123	13.03	0.014	1.418	102.26	116.9	101.1	103
1	95.3	0.155	0.187	7.564	1.012	0.423	39.964	49.305	60.9	101.1

Tab. 3.7: Performance of the DAB converter based on SiC MOSFETs CAS300M12BM2 and PSM for  $f_{sw}=40$  kHz ( $R_{dsON} = 6.5$  m $\Omega$ ,  $T_{case} = 100^{\circ}\text{C}$ ).

$P_{LOAD}$ (kW)	$\mu$ (%)	H1 SL (W): Leg A	H1 SL (W): Leg B	H2 SL (W): Leg A	H2 SL (W): Leg B	H1 CL(W)	H2 CL (W)	Total losses (W)	H2 $I_{RMS}$ (A)	H2 $T_J(^{\circ}\text{C})$
4	92.44	1.278	1.278	26.08	26.08	4.873	267.54	327.1	181.5	106.4
3	93.37	0.2368	0.2368	20	20	2.778	169.7	212.9	142.2	104.9
2	93.94	1.42	1.42	13.846	13.846	1.336	97.108	129	103.6	102.6
1	93.56	3.1	3.1	8.354	8.354	0.479	45.482	68.865	66.4	101.6

In case the DAB converter is made of SiC MOSFETs at the primary side and Si MOSFETs at the secondary side, higher efficiency can be registered if Si MOSFETS are automotive qualified as in case of the AUIRLB3036 device. Assuming the same switching frequency ( $f_{sw}=40$  kHz), the efficiencies are shown in Fig. 3.39 and Tab. 3.8. The results are coherent with Fig. 3.38 even if more than 2% of efficiency increase is achieved with the hybrid DAB based on SiC and Si MOSFETs. Lower drain-source

resistance of the AUIRLB3036 device ( $R_{dsON} = 3\text{m}\Omega$ ) than the SiC CAS300M12BM2 MOSFET ( $R_{dsON} = 6.5\text{m}\Omega$ ) is responsible of lower conduction losses and higher efficiency. On the contrary SiC MOSFETs exhibit a lower junction-case thermal resistance ( $R_{JC\_SiC} = 0.07^\circ\text{C/W}$ ) than Si MOSFETs ( $R_{JC\_Si} = 0.4^\circ\text{C/W}$ ), hence the junctions of the all-SiC DAB converter maintain lower temperatures than the hybrid SiC/Si DAB converter.

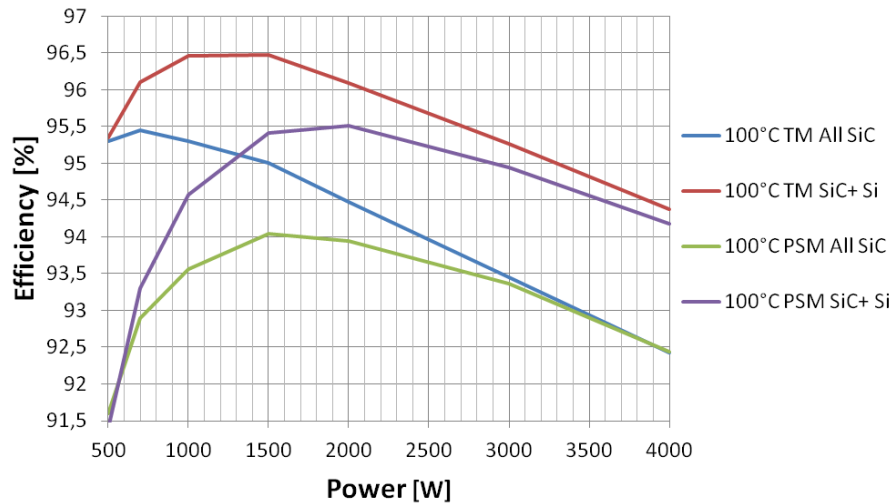


Fig. 3.39: Hybrid SiC/Si MOSFETs DAB converter and all-SiC DAB converter: efficiency at different

Tab. 3.8: Performance of the DAB converter based on SiC MOSFETs + SI MOSFETs AUIRLB3036 and TM for  $f_{sw}=40\text{ kHz}$  ( $R_{dsON}=3\text{ m}\Omega$ ,  $T_{case} = 100^\circ\text{C}$ ).

$P_{LOAD}$ (kW)	$\mu$ (%)	H1 SL (W): Leg A	H1 SL (W): Leg B	H2 SL (W): Leg A	H2 SL (W): Leg B	H1 CL (W)	H2 CL (W)	Total losses (W)	H2 $I_{RMS}$ (A)	H2 $T_J$ ( $^\circ\text{C}$ )
4	94.37	0.017	5.03	26.46	0.016	5	203.7	238.72	175.85	129.8
3	95.27	0.01	2	20.94	0.02	2.72	123.2	148.95	133.2	120.3
2	96.09	0.1	0.55	15.57	0.1	1.2	64.81	81.33	92.36	111.5
1	96.46	0.007	0.01	10.43	1.596	0.36	24.29	36.68	54.6	105.3

In order to optimize the weight and the volume onboard, some hints can be provided about the heat-sink of the DAB converter in case of CAS300M12BM2 and AUIRLB3036 devices. Considering a power load of 4kW and a  $T_{case}$  of  $100^\circ\text{C}$ , it is estimated that the heat dissipated by the single MOSFET is about 80W, and the junction temperature reached by the MOSFET CAS300M12BM2 and AUIRLB3036 are respectively around

107 °C and 128 °C. Setting a maximum junction temperature of 130 °C and an environment temperature of 25 °C, by means of a Cauer Network it is possible to estimate the thermal resistance between heat sink and environment  $R_{th(h-e)}$  needed to dissipate  $4 \cdot 80W$ , the heat of the entire H-Bridge, in both the analyzed case: when the H-Bridge is made with CAS300M12BM2 the thermal resistance  $R_{th(h-e)} = 0.35$  K/W while, with AUIRLB3036, the thermal resistance  $R_{th(h-e)} = 0.23$  K/W. With reference to the fin anodized black aluminum in Fig. 3.39 (MaccAL black anodized aluminum Heat Sink Series P300 83A) and its thermal resistance (K/W) – length (mm) characteristic in Fig. 3.40, the weight of the heat sink for the H-Bridge with AUIRLB3036 can be estimated around twice than that of H-Bridge with CAS300M12BM2. It implies lower weight and volume of the cooling system remaining inside the Safe Operating Area (SOA) which is highly advantageous for aerospace applications.

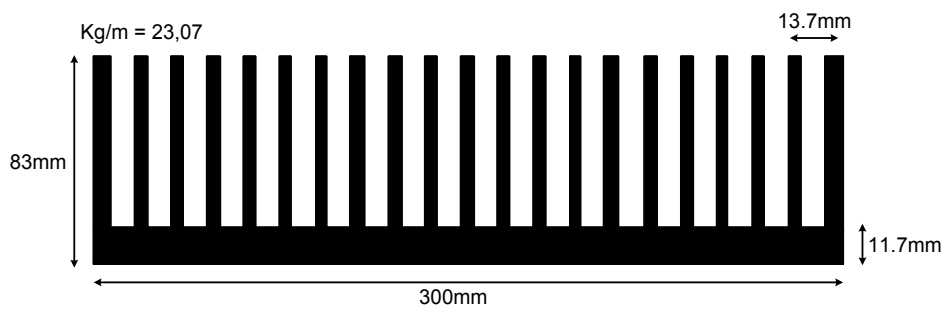


Fig. 3.39: MaccAL black anodized aluminum Heat Sink Series P300 83A.

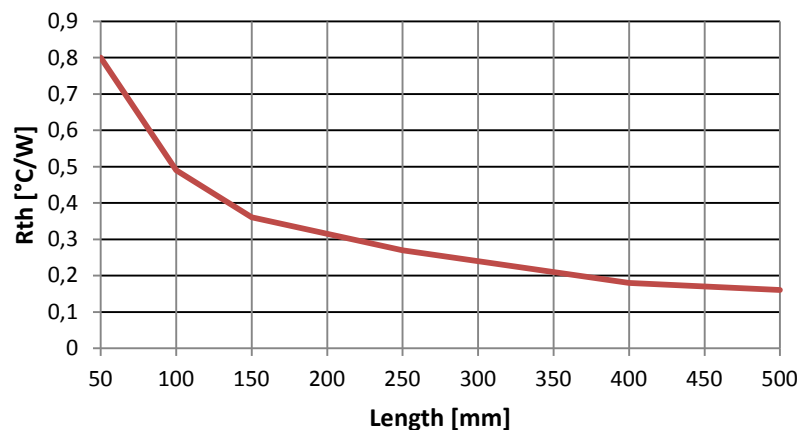


Fig. 3.40: Thermal Resistance – Length of Series P300 83A Heat Sink.

Since SiC MOSFETs allow high-frequency operation, the performances at 60 kHz have been also evaluated and the results are reported in Tab. 3.9. High efficiency are

guaranteed also at  $f_{sw}=60 \text{ kHz}$  thanks to the adoption of SiC MOSFETs. SiC MOSFETs are advantageous for MEA applications due to high thermal capability and high switching frequency operation. SiC MOSFETs can be applied to DAB converters allowing efficiency increase and reduced weight and volume.

Tab. 3.9: Performance of the DAB converter based on SiC MOSFETs CAS300M12BM2 and TM for  $f_{sw}=60 \text{ kHz}$  ( $R_{dsON} = 6.5 \text{ m}\Omega$ ,  $T_{case} = 100^\circ\text{C}$ ).

$P_{LOAD}$ (kW)	$\mu$ (%)	H1 SL (W): Leg A	H1 SL (W): Leg B	H2 SL (W): Leg A	H2 SL (W): Leg B	H1 CL(W)	H2 CL (W)	Total losses (W)	H2 $I_{RMS}$ (A)	H2 $T_J$ ( $^\circ\text{C}$ )
4	92.17	0.202	6.568	30	0.102	5.38	297.7	340	175.16	107.8
3	92.66	0.148	3.92	21.6	0.08	3.312	208.72	237.8	133.22	105.3
2	93.74	0.014	1.668	14.1	0.002	1.493	116.3	133.6	91.34	102.4
1	96.16	0.09	0.104	7.592	0.24	0.334	31.57	39.928	50.3	101.1

Concluding, a significant efficiency improvement at light load is obtained through the TM technique instead of the traditional PSM. A further improvement is achieved in case of a hybrid realization based on SiC MOSFETs plus Si automotive qualified MOSFETs instead of an all-SiC DAB converter. However, when specifications require high switching frequencies together to reduced size of the cooling system and harsh operation, the all-SiC DAB converter is the preferable choice. These remarks are summarized in Tab. 3.10.

Tab. 3.10: All-SiC DAB converter VS hybrid SiC/Si DAB converter.

	All-SiC DAB converter	Hybrid SiC/Si DAB converter
Efficiency	+	++
High temperature operation	++	+
Switching Frequency	++	+

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# Chapter IV

## SSBC and DAB Converters for Smart Transformer Application

Today the power generation and distribution system involve a high degree of distributed sources interconnected to the grid by means of power converters. The interface converters between the source and the grid are required to add functionalities, such as voltage regulation and reactive power compensation, intelligent power management and plug-and-play features. The distributed power generation systems (DPGS) based on renewable energy sources challenge the grid management due to the time-varying nature of the power injection. The ST, is a power electronics based transformer with additional control and communication capability which represents a possible solution to manage and to increase further the hosting capacity of the grid [1]. An open point in the ST technology is to achieve high quality of service together with high reliability. In terms of reliability, traditional transformers are hard to outperform because their lifetime is in the range of several decades and they have a low maintenance requirement, a target hardly achievable with the present power semiconductor technology. Besides, a traditional transformer efficiency is expected to be higher than a ST one, especially in three-stage architecture [2]. Due to this issues ST has not yet achieved market breakthrough even in traction and ships applications, where it can reduce space requirements and raise efficiency compared with low-frequency transformers [3]. However, applying the ST in the distribution system would be justified, and its higher cost paid, by its increased functionalities which allow connection of hybrid AC and DC sources and Smart Grids to the main power system.

Modular power converters allow to employ standard power semiconductors, hence they represent the right candidates for the ST achievement. Modular power converters fault tolerance capability can increase the ST availability. Among the different possible

topologies, the SSBC MMCC where each power conversion cell is connected to a DAB converter, represents a promising solution [4]-[5].

As an innovative concept for improving the reliability of the system, it was proposed to distribute the power among the modular cells of the ST by routing the power in the modular ST based on the condition of the building blocks [6]-[7]. Thereby, components with low remaining useful lifetime are loaded less to maximize the time to the next maintenance. In [6] has been introduced the concept of power routing in modular STs to implement active thermal control through unevenly loading the cells of the modular architecture. The aim is to avoid, or to delay as much as possible, the failures shifting the load from the cells whose components are older to the cells based on new components. In standard operation scheme, the cells process the same amount of power; therefore  $P_1 = P_2 = P_3$ . Power routing is the optimization technique in which each cell processes a specified amount of power with the aim of improving the system efficiency and reliability. The result can be  $P_1 \neq P_2 \neq P_3$ . In Fig. 4.1 the effect of the power routing technique on the expected-lifetime is illustrated considering as starting point that one of the cells is close to the end of its life.

Power routing can also influence the efficiency, which is typically the most well-known drawback of the active thermal control [8].

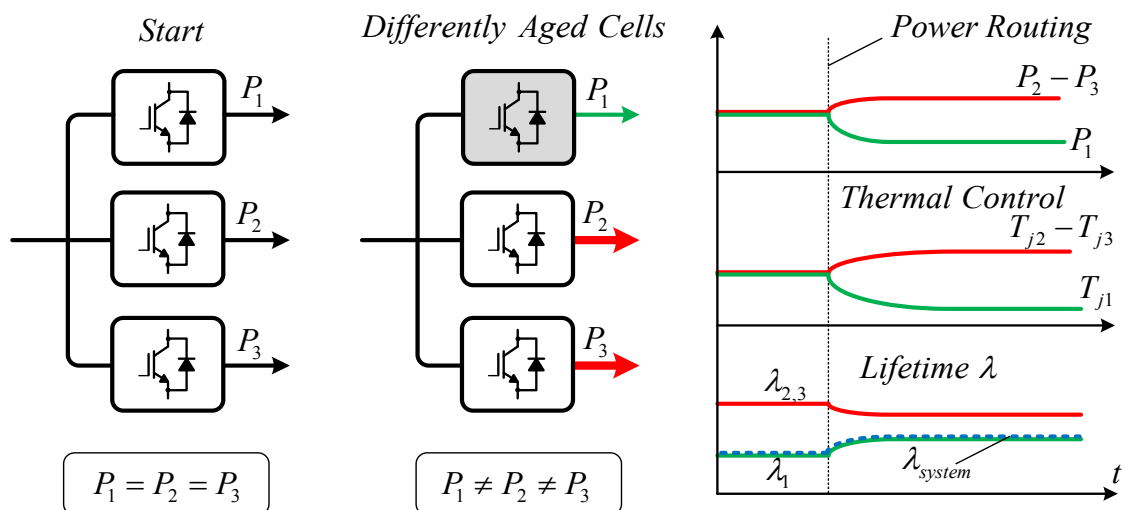


Fig. 4.1: An example of power routing impact on the lifetime of a modular topology.

The power routing techniques can provide different power references for each cell, however, it should be considered that the design and the correct operation of the inner control loops takes on a high importance in order to track the set power references. For this reason the present Chapter is focused in the inner control loops design and in the introduction of a new start-up procedure oriented to enhance the ST performances.

## 4.1 ST Average Model

The considered ST topology consists of an AC/DC converter in the Medium Voltage (MV) stage connected to several DAB converters which are series-connected in the MV stage and parallel-connected in the Low Voltage (LV) stage. Finally the LV DC-bus is connected to a DC/AC converter providing in output the LV AC voltage. In the present Chapter just the first two stages are analyzed and it is assumed that the rectified is 5-level SSBC MMCC. The LV DC bus is connected to a load in order to obtain a closed current path, as shown in Fig. 4.2. The traditional 50 Hz transformer is replaced by a high frequency transformer plus solid state devices, which is the key to achieve size and weight reduction.

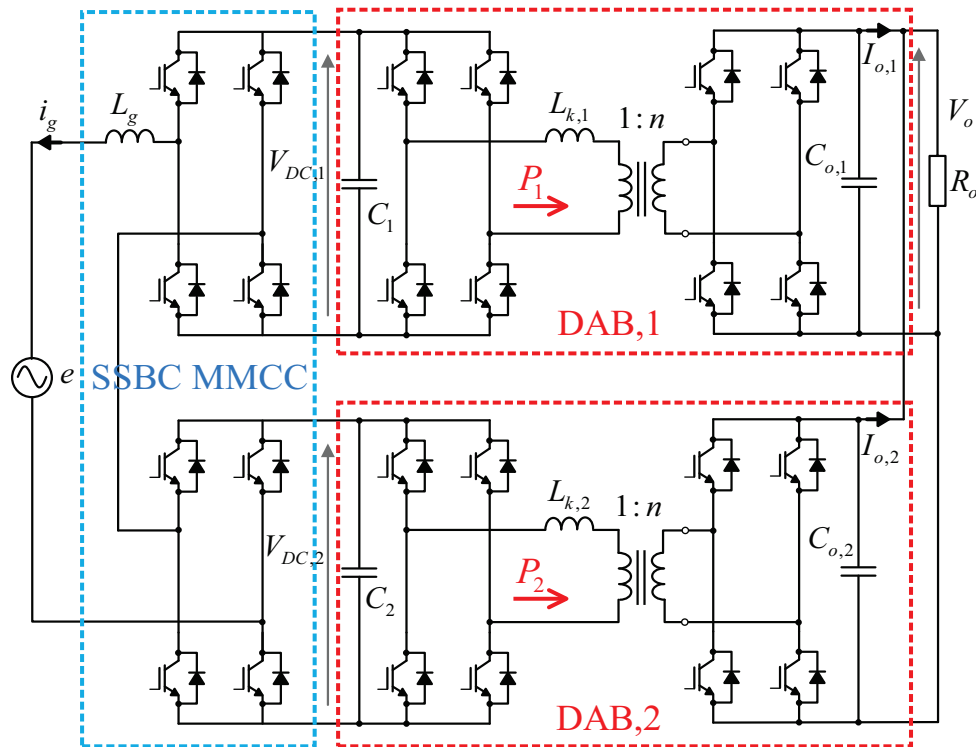


Fig. 4.2: Smart transformer: AC/DC, and DC/DC stages.

The average model of the ST is represented in Fig. 4.3 and it obtained by cascading the average model of the SSBC MMCC and DABs, analyzed respectively in Chapter I and in Chapter II.

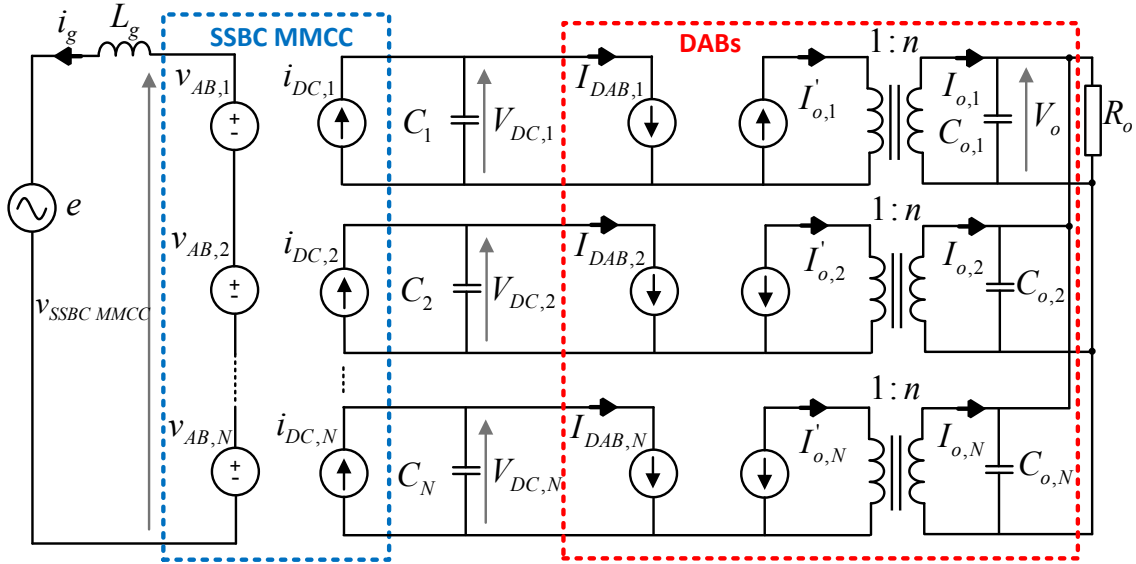


Fig. 4.3: Average model of ST.

The output voltage of each SSBC MMCC power cell is modeled in the AC side with (4.1),

$$v_{AB,i} = m_i V_{DC,i} \quad \text{with} \quad i = 1, 2, \dots, N \quad (4.1)$$

where  $V_{DC,i}$  is the corresponding DC-link voltage and  $m_i$  the corresponding modulating signal.

The  $i$ -th DC-side current of the SSBC MMCC is denoted as  $i_{DC,i}$  and it is expressed as:

$$i_{DC,i} = m_i i_g \quad \text{with} \quad i = 1, 2, \dots, N \quad (4.2)$$

The DAB converters are represented in MV-side and LV-side as current sources denoting the MV-side current as  $I_{DAB,i}$  and the LV-side current as  $I_{o,i}$ :

$$I_{DAB,i} = \frac{V_o T_{DAB} \varphi_i (1 - \varphi_i)}{2L_{k,i} n} \quad \text{with} \quad i = 1, 2, \dots, N \quad (4.3)$$

$$I_{o,i} = \frac{V_{DC,i} T_{DAB} \varphi_i (1 - \varphi_i)}{2L_{k,i} n} \quad \text{with} \quad i = 1, 2, \dots, N \quad (4.4)$$

In the previous equations:  $T_{DAB}$  represents the DAB switching period,  $\varphi$  ( $-0.5 < \varphi < 0.5$ ) is the phase-shift between the primary and secondary voltage of the HFT,  $n$  is the HFT turn ratio,  $L_k$  is the transformer leakage inductance,  $V_{DC}$  and  $V_o$  are respectively the input and output DAB voltages.

## 4.2 ST Small Signal Model

The average model can be linearized around a steady-state point and the small signal model can be derived. Based on the linearized small signal model, the main open-loop transfer functions of the converters can be obtained. Hence a feedback control structure can be designed on the basis of the small-signal model. Finally the control parameters can be tuned in order to achieve a good trade-off between stability and dynamic performances.

The sole small signal model of the considered ST can be achieved starting from the small signal models obtained separately for SSBC MMCC and DAB converter. In the overall model, the cross-coupling terms between the two stages have to be considered. Assuming that all the DAB converters are perfectly identical in their parameters and considering equations (2.10) - (2.11), it results:

$$\tilde{I}_{DAB} = \frac{T_{DAB}}{2L_k n} \left[ \tilde{\varphi} (1 - 2\bar{\Phi}) \bar{V}_o + \tilde{V}_o (1 - \bar{\Phi}) \bar{\Phi} \right] \quad (4.5)$$

$$\tilde{I}_o = \frac{T_{DAB}}{2L_k n} \left[ \tilde{\varphi} (1 - 2\bar{\Phi}) \bar{V}_{DC} + \tilde{V}_{DC} (1 - \bar{\Phi}) \bar{\Phi} \right] \quad (4.6)$$

where the notation  $\tilde{x}$  represents the small variation of the variable  $x$  around the steady-state value indicated with  $\bar{X}$ . With this assumption  $\tilde{\varphi}$  represents the small variation of the phase shift around the steady-state value  $\bar{\Phi}$ ;  $\tilde{V}_o$  represents the small variation of the output voltage around the steady-state value  $\bar{V}_o$ ;  $\tilde{V}_{DC}$  represents the small variation of

the input voltage around the steady-state value  $\bar{V}_{DC}$ . Considering  $n=1$ ,  $\bar{V}_{DC} = \bar{V}_o$  and defining the following constant parameters:

$$G_\varphi = \frac{T_{DAB}}{2L_k n} (1 - 2\bar{\Phi}) \bar{V}_{DC} \quad G_V = \frac{T_{DAB}}{2L_k n} (1 - \bar{\Phi}) \bar{\Phi} \quad (4.7)$$

the small signal model of the input  $\tilde{I}_{DAB}$  and output current  $\tilde{I}_o$  results in following:

$$\tilde{I}_{DAB} = [G_\varphi \tilde{\varphi} + G_V \tilde{V}_o] \quad (4.8)$$

$$\tilde{I}_o = [G_\varphi \tilde{\varphi} + G_V \tilde{V}_{DC}] \quad (4.9)$$

Applying the Kirchhoff's voltage law to output port of the DAB converters, it is obtained:

$$\tilde{V}_o = \left( \frac{NR_o}{R_o C_o s + 1} \right) [G_\varphi \tilde{\varphi} + G_V \tilde{V}_{DC}] \quad (4.10)$$

where  $C_o$  is defined as:

$$C_o = \sum_{i=1}^N C_{o,i} \quad (4.11)$$

Substituting (4.10) in (4.8), it results in:

$$\tilde{I}_{DAB} = \left[ G_\varphi \tilde{\varphi} + NG_V \left( \frac{R_o}{R_o C_o s + 1} \right) (G_\varphi \tilde{\varphi} + G_V \tilde{V}_{DC}) \right] \quad (4.12)$$

Eq.(4.12) can be rearrange as:

$$\tilde{I}_{DAB} = \left( \frac{G_\varphi (1 + NR_o G_V + R_o C_o s)}{R_o C_o s + 1} \right) \tilde{\varphi} + \left( \frac{NR_o G_V^2}{R_o C_o s + 1} \right) \tilde{V}_{DC} \quad (4.13)$$

which shows the relation between the input current of each DAB and the voltage on the MV side. Hence the ST plant (limited to the SSBC MMCC connected to the DAB converters) can be described by:

$$\tilde{V}_{DC} = \frac{(\bar{I}_g L_g s + N\bar{V}_{DC} \bar{M})}{(2N\bar{V}_{DC} C s + N\bar{I}_g \bar{M})} \tilde{I}_g - \frac{2N\bar{V}_{DC}}{(2N\bar{V}_{DC} C s + N\bar{I}_g \bar{M})} \tilde{I}_{DAB} \quad (4.14)$$

$$\begin{aligned} \tilde{V}_{DC} = & \frac{(\bar{I}_g L_g s + N\bar{V}_{DC}\bar{M})}{(2N\bar{V}_{DC}C s + N\bar{I}_g\bar{M})} \tilde{I}_g + \\ & - \frac{2N\bar{V}_{DC}}{(2N\bar{V}_{DC}C s + N\bar{I}_g\bar{M})} \left[ \left( \frac{G_\varphi (1 + NR_o G_V + R_o C_o s)}{R_o C_o s + 1} \right) \tilde{\varphi} + \left( \frac{NR_o G_V^2}{R_o C_o s + 1} \right) \tilde{V}_{DC} \right] \end{aligned} \quad (4.15)$$

Developing (4.15) it results:

$$\begin{aligned} \tilde{V}_{DC} = & \frac{(\bar{I}_g L_g s + N\bar{V}_{DC}\bar{M})(R_o C_o s + 1)}{(2N\bar{V}_{DC}C s + N\bar{I}_g\bar{M})(R_o C_o s + 1) + 2\bar{V}_{DC}R_o (NG_V)^2} \tilde{I}_g + \\ & - \frac{2N\bar{V}_{DC}G_\varphi (1 + NR_o G_V + R_o C_o s)}{(2N\bar{V}_{DC}C s + N\bar{I}_g\bar{M})(R_o C_o s + 1) + 2\bar{V}_{DC}R_o (NG_V)^2} \tilde{\varphi} \end{aligned} \quad (4.16)$$

The last equation can be rewritten denoting as:

$$\begin{aligned} N_{I_g}(s) &= (\bar{I}_g L_g s + N\bar{V}_{DC}\bar{M})(R_o C_o s + 1) \\ N_\varphi(s) &= 2N\bar{V}_{DC}G_\varphi (1 + NR_o G_V + R_o C_o s) \\ D(s) &= (2N\bar{V}_{DC}C s + N\bar{I}_g\bar{M})(R_o C_o s + 1) + 2\bar{V}_{DC}R_o (NG_V)^2 \end{aligned} \quad (4.17)$$

Finally it is obtained:

$$\tilde{V}_{DC} = \frac{N_{I_g}(s)}{D(s)} \tilde{I}_g - \frac{N_\varphi(s)}{D(s)} \tilde{\varphi} \quad (4.18)$$

$$\tilde{V}_{DC,i} = \frac{N_{I_g}(s)}{D(s)} \tilde{I}_g - \frac{N_\varphi(s)}{D(s)} \tilde{\varphi}_i \quad \text{with } i = 1, 2, \dots, N \quad (4.19)$$

Eq. (4.19) represents the small signal model of the  $i$ -th power cell of the ST and in particular it is the model of the  $i$ -th H-Bridge of the SSBC MMCC connected to a DAB converter.

Fig. 4.4 shows the small signal model of the ST, with particular focus to the cross coupling terms between the SSBC MMCC stage and the DAB converters. Indeed, it can be observed that the model of the SSBC MMCC depends on  $\tilde{\varphi}$ , which is the actuating signal in DAB control loop, (eq. 4.19).

Differently the model of the DAB converter (eq. 2.11) depends on  $\tilde{V}_{DC}$ , which is the DC-link voltage controlled in SSBC MMCC voltage loop.

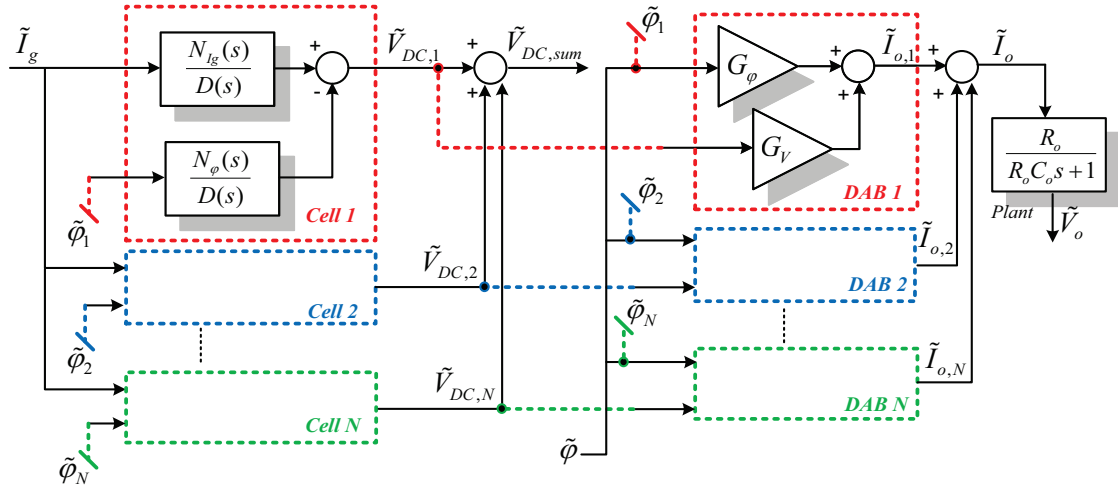


Fig. 4.4: ST small signal model.

### 4.3 ST: SSBC MMCC and DAB Converters Control

#### System

In case of a 5-levels SSBC MMCC ( $N=2$ ), the ST small signal model shown in Fig. 4.4 becomes the model represented in Fig. 4.5 where are clearly visible the total voltage control loop and the DAB converter output voltage loop.

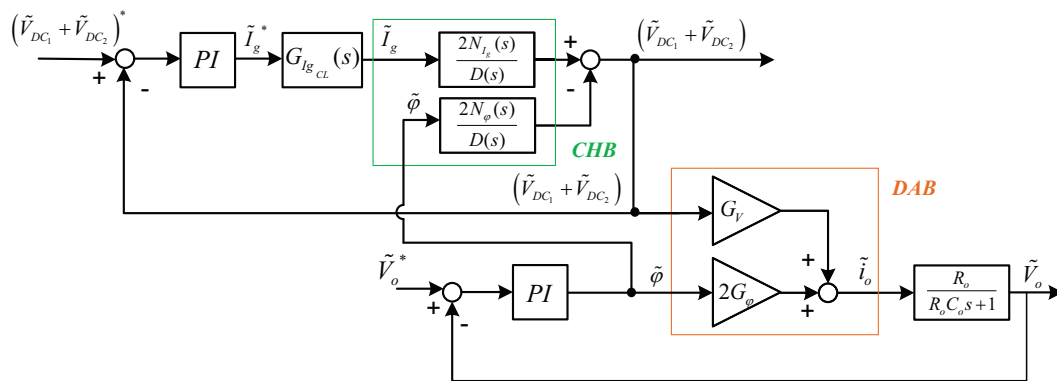


Fig. 4.5: ST small signal model in case of a 5-levels SSBC MMCC.

The outer DC voltage control loop provides the reference to an internal current control loop as shown in Fig. 4.6. Also in this case, the inner current loop is tuned to achieve

short settling times, while the outer loop is tuned in order to ensure optimum voltage regulation and stability. If the current control loop is adjusted to be optimally damped, it can be described by a second-order transfer.

The parameters of the SSBC MMMCC voltage regulator can be tuned in order to achieve a closed loop dynamic which is at least ten times slower than the current loop (as discussed in Chapter I). In this particular application, the control of each cell provides also a different correction action in the modulating signal generation. Indeed, the correction action depends on the difference between the power reference  $P_i^*(T_{junction,i})$  of the  $i$ -th cell and the corresponding measured power (where it is assumed that the power reference is calculated through the power routing technique). The DABs converter output voltage loop is shown in Fig. 4.7.

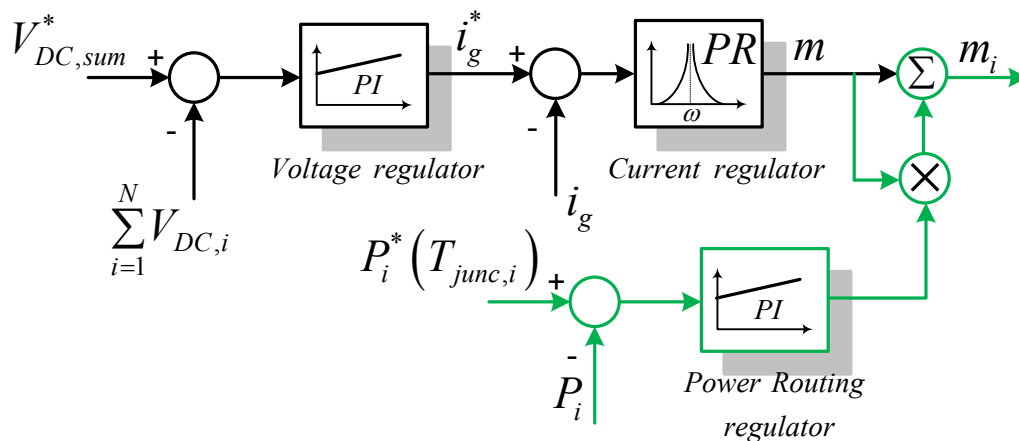


Fig. 4.6: Control scheme of the SSBC MMCC.

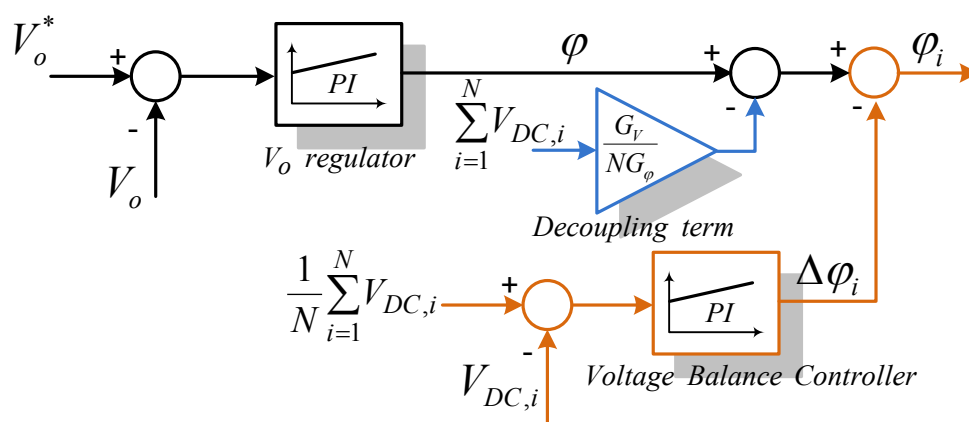


Fig. 4.7: Control scheme of the DAB converters.

Starting from the DAB converter equations, analyzed in Chapter II, a control law can be defined considering  $\varphi$  as the control variable and  $V_{DC}$  as a measurable disturbance. To decouple the DABs output voltage loop from variations of the DC-link voltages, a compensation term has been added to the actuating signal  $\varphi$ , as shown in Fig. 4.7. The generation of the phase shift angle for each DAB converter is corrected subtracting the contribution  $\Delta\varphi_i$  which is provided by a PI processing the voltage error between the voltage average value and the measured voltage for each DC link (see Fig. 4.7). Hence, in case of a ST with two power channels  $P_1$  and  $P_2$ , the phase shift for each DAB converter can be calculated as:

$$\varphi_i = \varphi - K_{pBAL,i} \left( 1 + \frac{1}{T_{BAL,i}s} \right) \left( \left( \frac{V_{DC,1} + V_{DC,2}}{2} \right) - V_{DC,i} \right) \quad (4.20)$$

where  $K_{pBAL,i}$  is the balance proportional gain related to the  $i$ -th DC-link and  $T_{BAL,i}$  is the correspondent balance integral time constant needed to guarantee a zero balance error in steady-state. The effectiveness of the proposed control scheme is proven in Fig. 4.8 and Fig. 4.9. In Fig. 4.8, at  $t=1s$  a small variation of  $\Delta V_{DC,sum}^* = 20V$  is applied to the overall DC voltage reference. As shown in Fig. 4.8, the ST small signal model provides the same response obtained through the ST switching model, developed with the PLECS toolbox. Thanks to the decoupling term, the effect of the variation in the DC-link voltages is negligible in the output DABs voltage profile  $V_o$ .

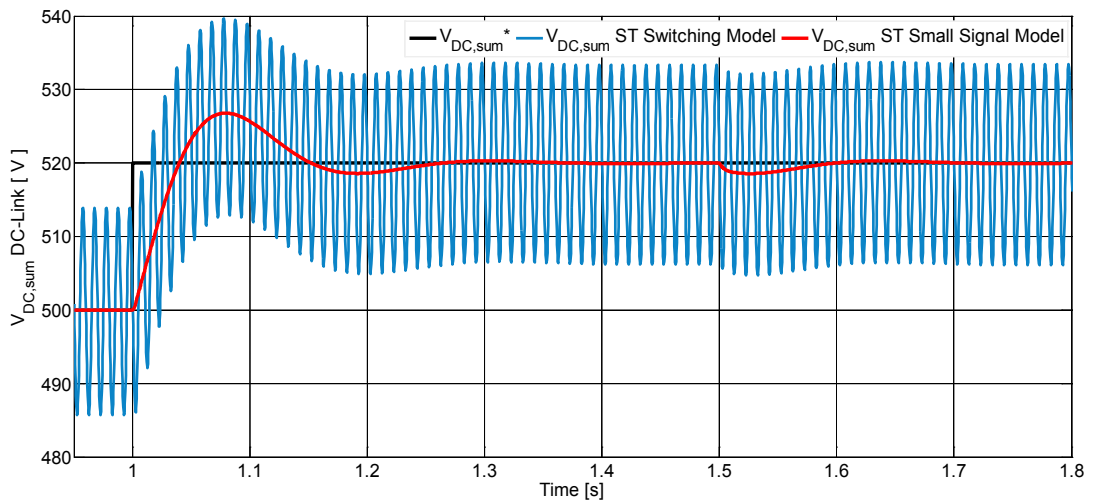


Fig. 4.8: Comparison of the ST switching model with the ST small signal model in  $V_{DC,sum}^*$  variation.

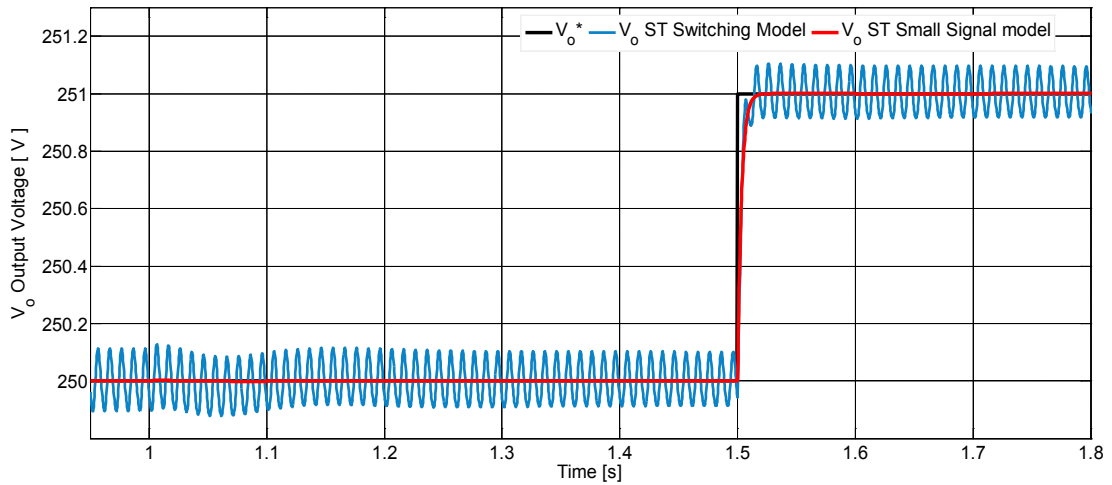


Fig. 4.9: Comparison of the ST switching model with the ST small signal model in  $V_o^*$  variation.

At  $t=1.5s$  an output voltage reference variation  $\Delta V_o^* = 1V$  is applied and the models match each other also in this case (see Fig. 4.9). Besides a small variation in the DABs output voltage reference affect as a disturbance the DC-links dynamic. The simulation results are completed by the current and voltage waveforms of the SSBC MMCC related to the case of 2kW of load power and steady-state operation. Finally the voltages at the primary and secondary of the HFT are shown in Fig. 4.10 - 4.11. Considering the power stage parameters reported in Tab. 4.1, experimental tests have been performed in order to confirm the simulation results.

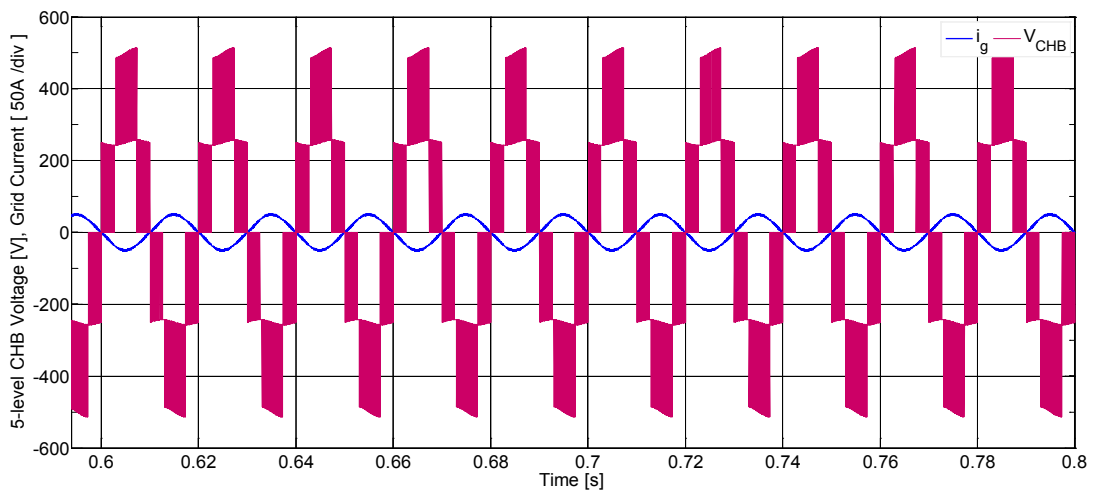


Fig. 4.10: 5-level SSBC MMCC voltage and grid current in steady-state operation.

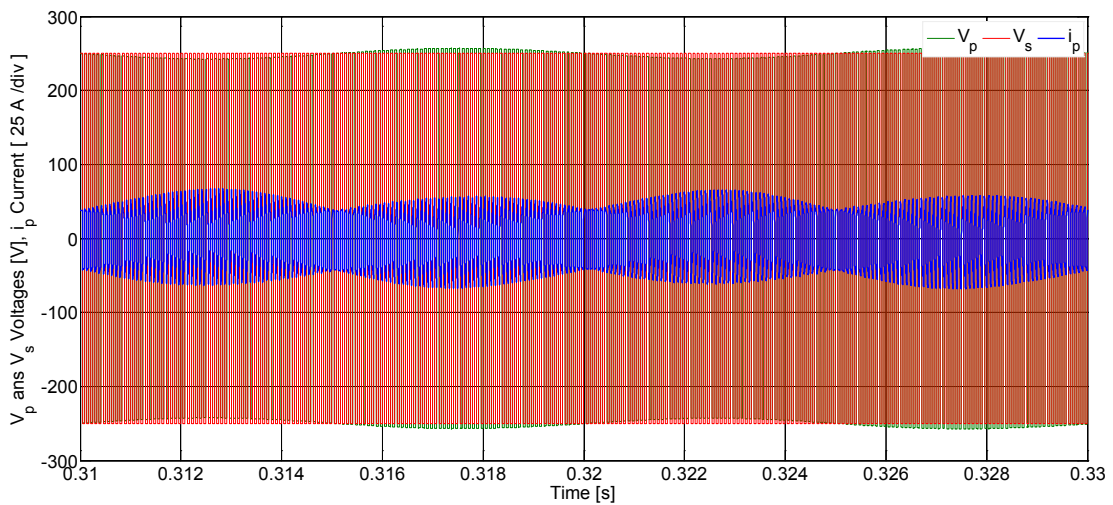


Fig. 4.11: HFT Primary and Secondary Voltage, Primary Leakage Current with  $P_{DAB} = 1\text{kW}$ .

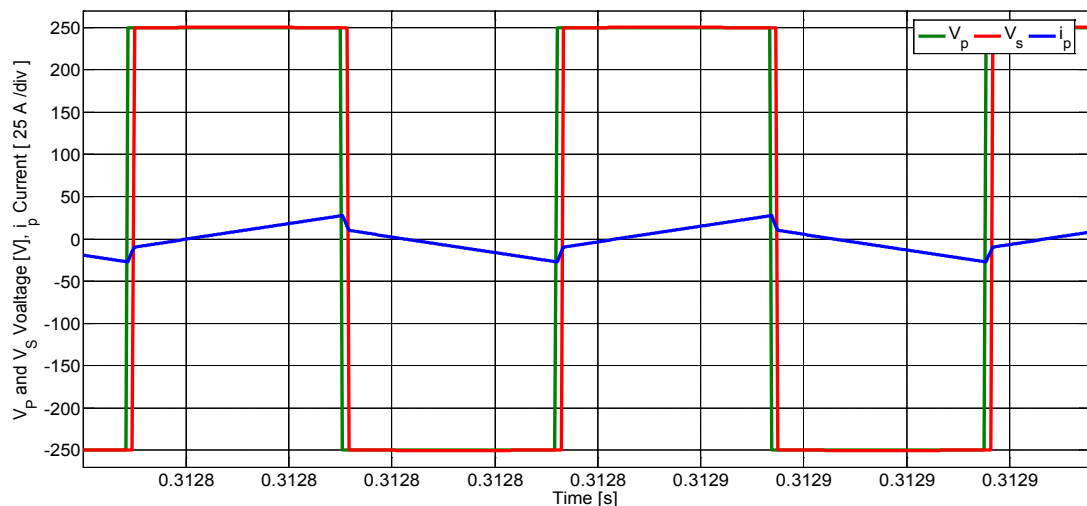


Fig. 4.12: Zoom of the HFT Primary and Secondary Voltage, Primary Leakage Current,  $P_{DAB} = 1\text{kW}$ .

The experimental setup of the ST is shown in Fig. 4.13. It consists of a 5-levels SSBC MMCC active rectifier connected to the MV stage and of two DABs converters, feeding a common passive load in the LV stage. Both the SSBC MMCC and DAB converters have been assembled with the same IGBT Danfoss module DP25H1200T101616 (Fig.4.14). The system has been controlled with a dSPACE SCALEXIO platform based on three DS2655 FPGA baseboards (Fig. 4.15); each board has been programmed with a FPGA Xilinx Blockset Toolbox and controlled with the software dSPACE Control Desk.

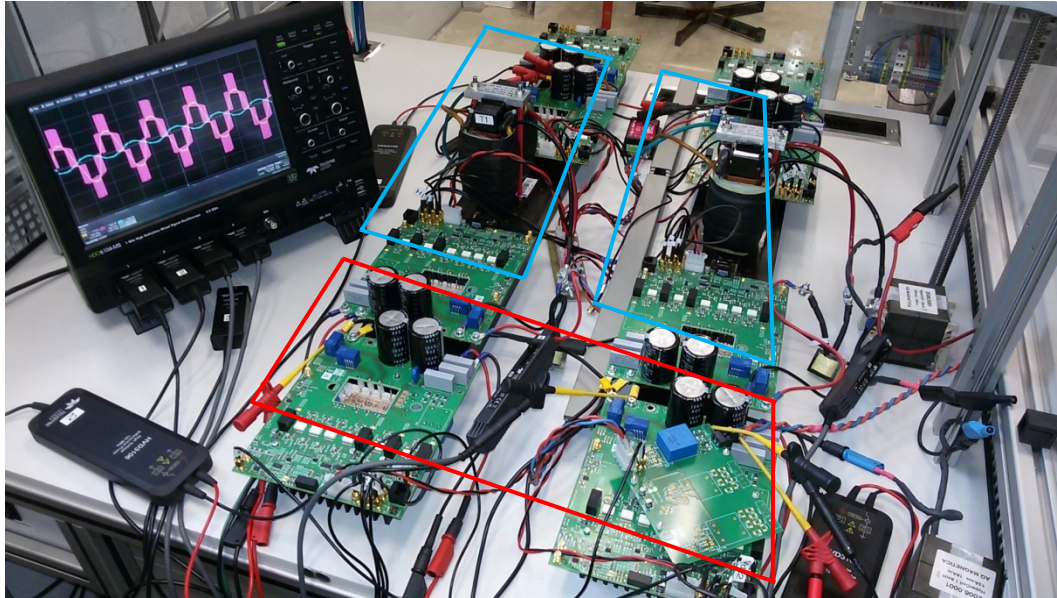


Fig. 4.13: ST setup: SSBC MMCC (limited by the red rectangle) and DAB converters (blue rectangles).

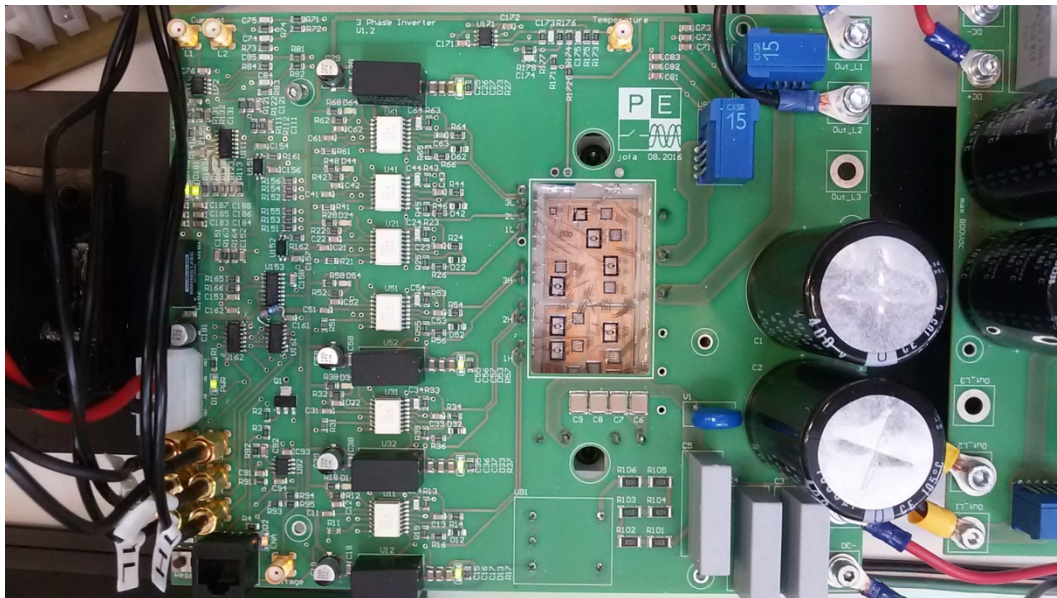


Fig. 4.14: IGBT Danfoss open module DP25H1200T101616



a)



b)

Fig. 4.15: a) dSPACE SCALEXIO system based on three DS2655 FPGA; b): Control Desk platform.

Due to the presence of an infrared camera for thermal monitoring, the IGBT modules are open and isolation-less; therefore experimental results have been executed in low voltage and low power conditions. In rated and balanced condition the power delivered by the SSBC MMCC active rectifier is equal to  $P_n = P_{DAB,1} + P_{DAB,2} = 2kW$ , equally divided between the two DC-buses:  $P_{DAB,1} = P_{DAB,2} = 1 kW$ . In Fig. 4.16 - 4.18, there

are reported all the current and the voltage waveforms of the system in case of steady-state operation. It is possible to verify the match among the simulation and the experimental results.

Tab. 4.1: ST Power Stage Parameters.

<i>Symbol</i>	<i>Description</i>	<i>Value</i>
$V_g$ (RMS)	RMS grid Voltage	220 V/ 50 Hz
$L_g$	AC Inductor filter	3.8 mH
$V_{DC,1} \sim V_{DC,2}$	DC Voltage in each cell	250 V
$V_o$	DC Output Voltage	250 V
$C_{Cell,1} \sim C_{Cell,2}$	MV Capacitor	930 $\mu$ F
$C_o$	LV Capacitor	920 $\mu$ F
$R_o$	Passive Load	32 $\Omega$
$L_{k,1} \sim L_{k,2}$	Leakage Inductance MFT	63 $\mu$ H
$n$	MFT turns ratio	1
$f_{sw}$ SSBC MMCC	SSBC Switching Frequency	3 kHz
$f_{sw}$ DAB	DAB Switching Frequency	12 kHz

In Fig. 4.16 - 4.18, are represented the small scale ST prototype waveforms in steady-state operation, when all the modules are equally loaded with a rated power of 1kW.

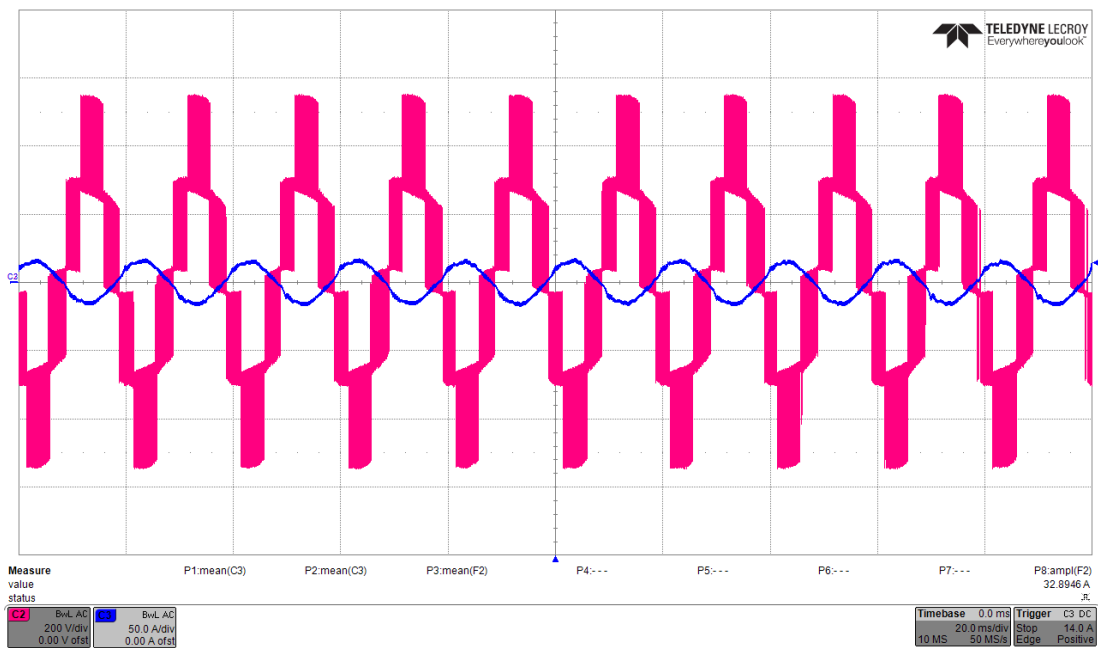


Fig. 4.16: Experimental results: 5-level SSBC MMCC Voltage and Grid Current in steady-state operation.

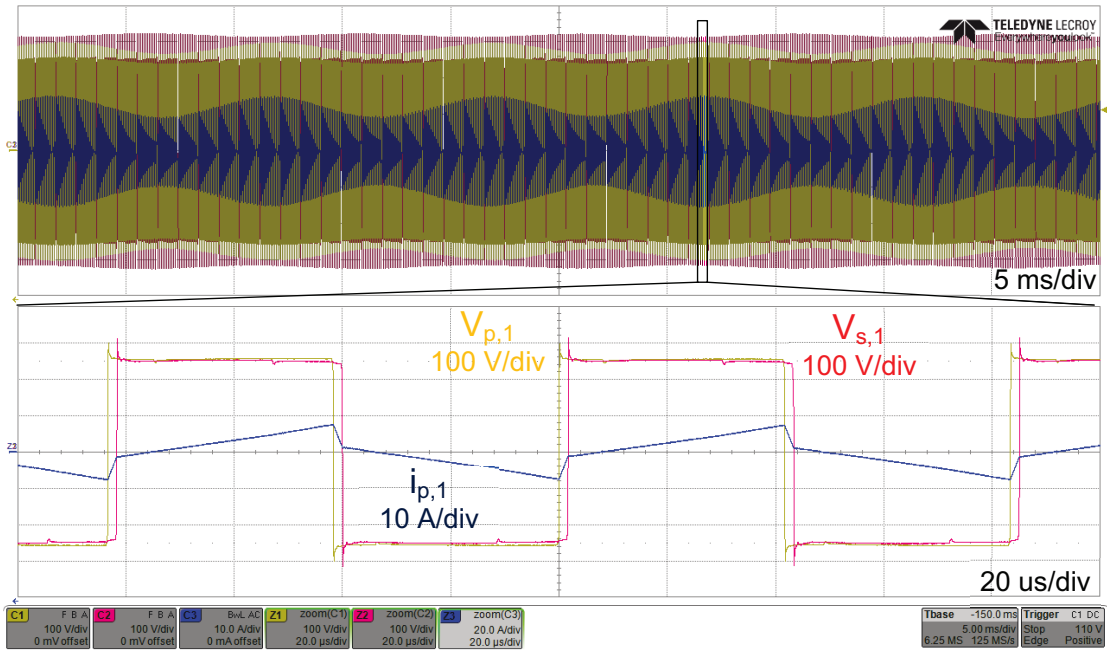


Fig. 4.17: Experimental results: HFT Primary and Secondary Voltage, Primary Current with  $P_{DAB} = 1kW$ .

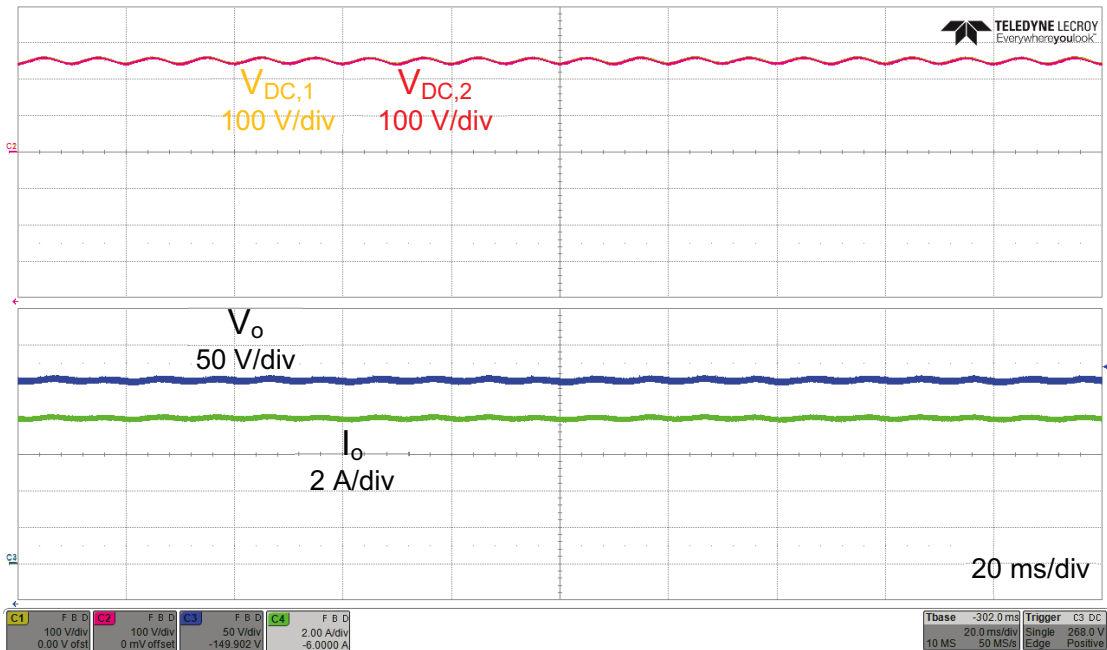


Fig. 4.18: Experimental results:  $V_{DC,1}$  and  $V_{DC,2}$  DC-Link voltages (yellow-red);  $V_o$  output voltage (blue) and  $I_o$  current (green).

### 4.3.1 Comparison of different Voltage Balance methods

Differently from the voltage balance control scheme shown in Fig. 4.7, the DC-links voltage balance control is commonly in charge of the MV power conversion stage of the ST as shown in Fig. 4.19, where  $V_{DC,i}$  denotes the  $i$ -th output voltage of the AC/DC power conversion stage and  $V_o$  denotes the LV DC link voltage

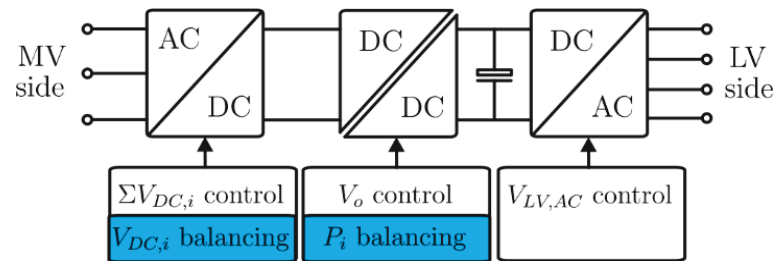


Fig. 4.19: Possible control scheme of a ST: voltage balance in the MV-stage and power control in isolation stage

However, it should be considered that, for high number of cells or high power systems, the AC/DC power conversion stage is characterized by low switching frequency. As a consequence also the voltage balance control is operated at low switching frequencies. In order to obtain a voltage balance control with higher dynamic performances, in the previous section it has been proposed a balance controller operated at the DC/DC power conversion stage. The related ST control scheme is summarized in Fig. 4.20. It is possible to observe that if the voltage balance control is in charge of the DC/DC power conversion stage, a stress balancing control can be performed by the AC/DC power conversion cell in addition to its basic control functionalities. The stress balancing control does not balance the power flowing to the DC/DC power conversion stage, but the stress for the components in the system.

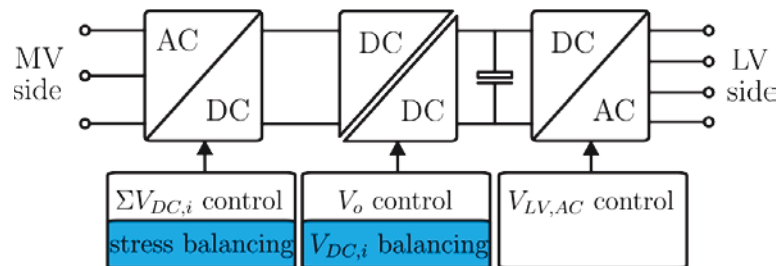


Fig. 4.20: Voltage balancing in the isolation stage and stress balancing in MV-stage.

The ability to impose a different power reference in the DABs is closely related to the concept of DC-link voltage balance. The control scheme is shown in Fig. 4.7, and it has been studied in case of a ST with two power channels,  $P_1$  and  $P_2$ .

Looking at Fig. 4.7, and considering the coupling transfer function between the SSBC MMCC and DAB stage:

$$G_{SSBC\_DAB}(s) = \frac{1}{C \left( s + \frac{\bar{I}_g \bar{M}}{2\bar{V}_{DC} C} \right)} \quad (4.21)$$

considering the acquisition and the PWM delay transfer function:

$$G_{PWM}(s) = \frac{1}{\left( s + \frac{1}{1.5T_{DAB}} \right)} \quad (4.22)$$

and considering the coupling term between the two balancing loops through the plant transfer function:

$$G_{V_{DC,1\_DC,2}}(s) = \frac{G_\varphi \left( s + \frac{1+2G_V R_o}{R_o C_o} \right)}{\left( s + \frac{1+G_V R_o}{R_o C_o} \right)} \quad (4.23)$$

the open loop transfer function of the  $i$ -th voltage balance loop can be derived as:

$$V_{DC,i} = \frac{2G_\varphi}{3T_{DAB} C} \frac{1}{\left( s + \frac{\bar{I}_g \bar{M}}{2\bar{V}_{DC} C} \right) \left( s + \frac{1}{1.5T_{DAB}} \right)} \frac{\left( s + \frac{1+2G_V R_o}{R_o C_o} \right)}{\left( s + \frac{1+G_V R_o}{R_o C_o} \right)} \varphi_i \quad (4.24)$$

Considering the PI controller, the total open loop transfer function results:

$$G_{BAL,i}(s) = \frac{2G_\varphi}{3T_{DAB} C} \frac{K_{pBAL,i} \left( s + \frac{1}{T_{BAL,i}} \right)}{s \left( s + \frac{\bar{I}_g \bar{M}}{2\bar{V}_{DC} C} \right) \left( s + \frac{1}{1.5T_{DAB}} \right)} \frac{\left( s + \frac{1+2G_V R_o}{R_o C_o} \right)}{\left( s + \frac{1+G_V R_o}{R_o C_o} \right)} \quad (4.25)$$

In order to delete the slower pole, the time constant of the PI is tuned as:

$$T_{BAL,i} = \frac{2\bar{V}_{DC} C_{in}}{\bar{I}_g \bar{M}} \quad (4.26)$$

The value of proportional constant is chosen considering as final transfer function the following:

$$G_{BAL,i}(s) = \frac{K_{pBAL,i} G_\phi}{C s \left( s + \frac{1}{1.5T_{DAB}} \right)} \frac{\left( s + \frac{1 + 2G_V R_o}{R_o C_o} \right)}{\left( s + \frac{1 + G_V R_o}{R_o C_o} \right)} \approx \frac{K_{pBAL,i} G_\phi}{C s (1.5T_{DAB} s + 1)} \quad (4.27)$$

In Fig. 4.21 it is represented the voltage response for different values of  $K_{pBAL}$  and in case of a step variation in the power references imposed by the power routing control. It results in a fast second order system where the limitation in the bandwidth is in the presence of the very high switching frequency pole (from 10kHz up to 100kHz). Increasing the proportional gain, the balancing became faster. The larger is the bandwidth, the faster is the balancing response and the smaller is the effect of the unbalanced power in the slope of the  $V_{DC,i}$ .

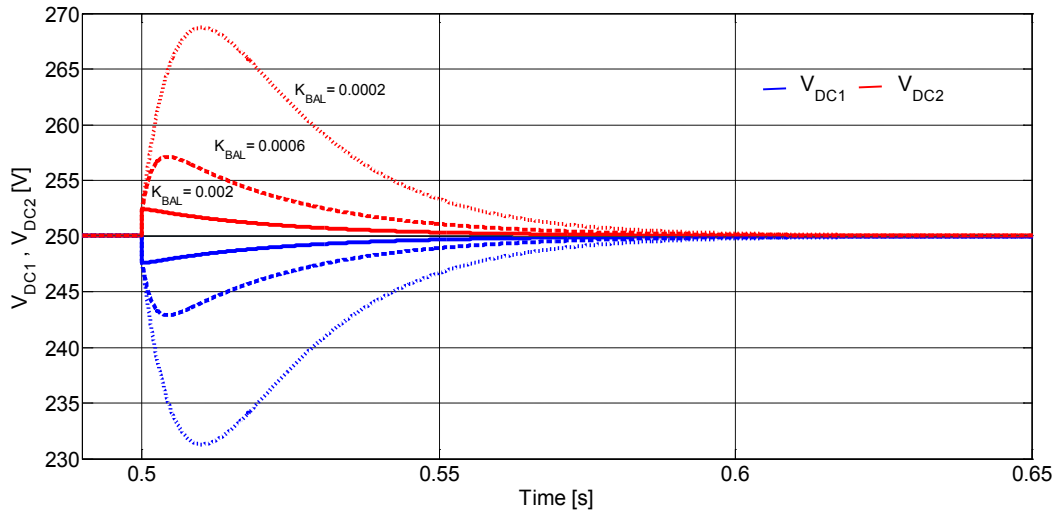


Fig. 4.21:  $V_{DC1}$  and  $V_{DC2}$  balancing waveforms at different  $K_{pBAL}$  values.

It is assumed that, as effect of the power routing technique, at  $t=0.5s$  the power in  $DAB_1$  is increased with a  $\Delta P_1^* = +500$ , while the power in the  $DAB_2$  is reduced,  $\Delta P_2^* = -500W$ , maintaining the same output power (Fig. 4.22 - 4.23). It can be seen that the step in the

power references implies a transient variation of the DC-link voltages (Fig. 4.24) and that the average model fits well the switching model developed by PLECS toolbox.

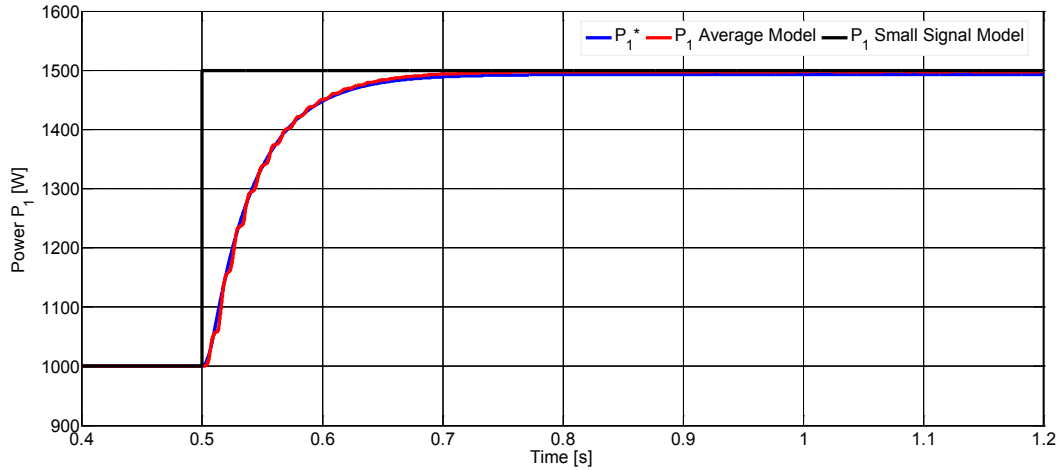


Fig. 4.22: Power step in the first branch of the ST from 1kW to 1.5kW.

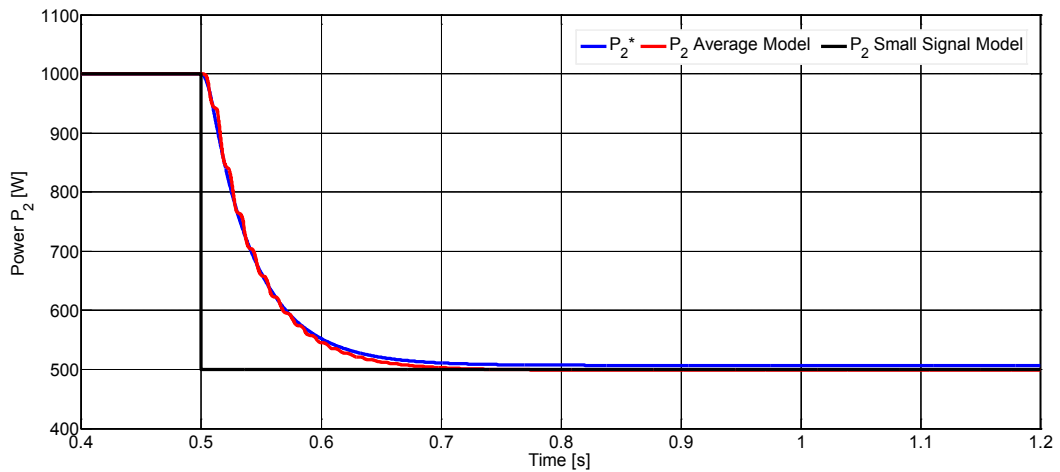


Fig. 4.23: Power step in the first branch of the ST from 1kW to 0.5kW.

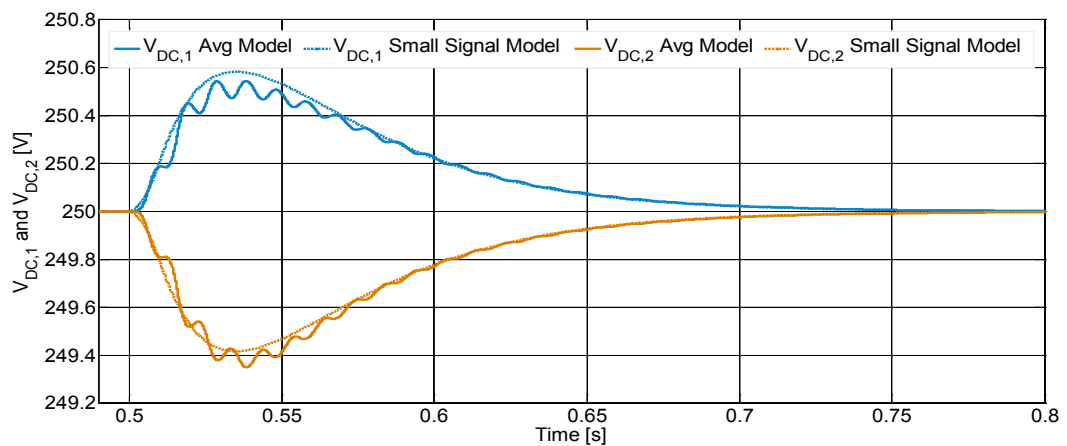


Fig. 4.24: DAB converters voltages in case of a power variation in both the converters.

The performances of the proposed voltage balance control in the DC/DC power conversion stage can be compared with the performances obtained in case the voltage balance is operated at the AC/DC power conversion stage.

In the last case the open loop transfer function becomes:

$$G_{BAL,i}(s) = K_{sys} K_{pBAL,i} \left( 1 + \frac{1}{T_{BAL,i}s} \right) \left( \frac{1}{1.5T_{SSBC}s + 1} \right) \left( \frac{1}{L_g s + R_g} \right) \left( \frac{R_i}{R_i C_i s + 1} \right) \quad (4.28)$$

where the model of SSBC MMCC PWM delay, the inductive filter and the DC-Link model are taken in account. The corresponding Bode diagrams considering both the voltage balance methods are represented in Fig.4. 25. The crossover frequency in both the models is derived setting the phase margin value at  $PM=75^\circ$ , showing a significantly difference in the bandwidth value ( $BW_{SSBC\_MMCC}=4Hz$ ,  $BW_{DAB}=160Hz$ ) and as a consequence a different disturbance rejection capability. It can be concluded that the voltage balance control in charge of the DC/DC power conversion stage provides higher performances in terms of dynamics and rejection capability respect to the voltage balance operated at the AC/DC power conversion stage. It is due to the higher switching frequencies of the DC/DC converters respect to the AC/DC converter.

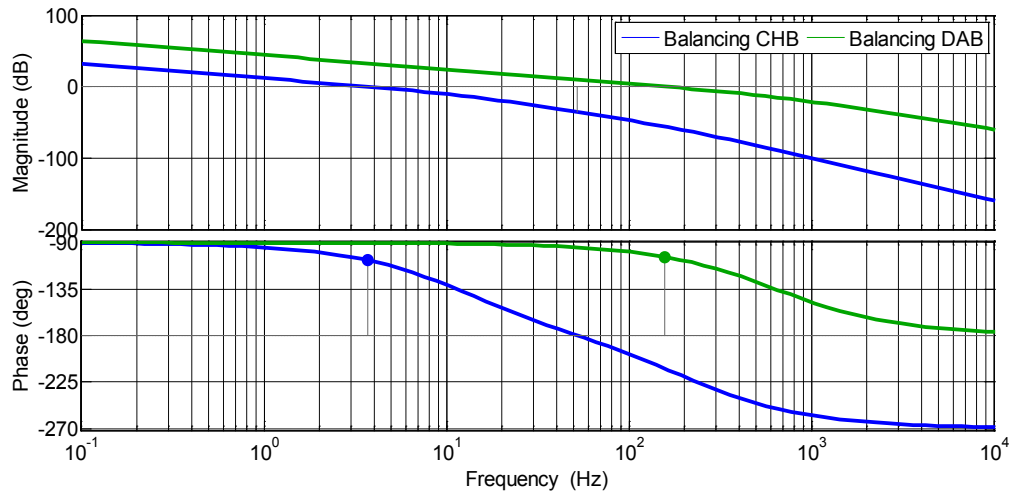


Fig. 4.25: SSBC MMCC and DAB voltage balance Bode Diagram.

The dynamics of the two voltage balance methods has been evaluated when an unbalanced power condition is required from a secondary controller (e.s. active thermal control). In particular it is assumed that the power references are:

$$P_n = P_{DAB,1} + P_{DAB,2} = 2kW \quad P_{DAB,1} = 3P_{DAB,2} \quad (4.29)$$

Considering a  $P_n = 2kW$  then  $P_{DAB,1} = 1.5 kW$  and  $P_{DAB,2} = 0.5 kW$ .

As it expected from the Bode diagrams, the voltage response in presence of the power variations is faster in case the voltage balance is performed by the DABs converters (Fig. 4.26) than by the SSBC MMCC (Fig 4.27) and also a lower voltage ripple is verified.

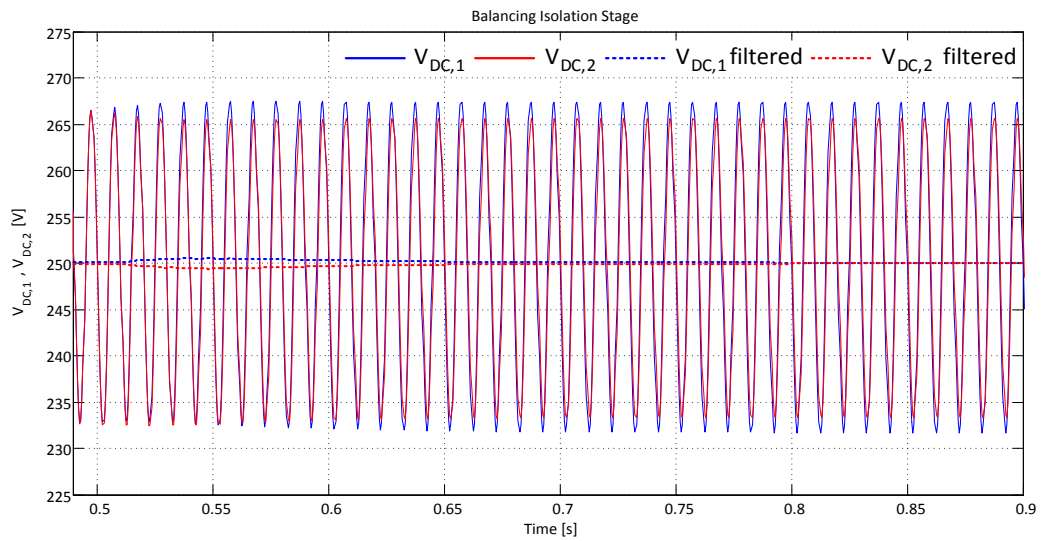


Fig. 4.26: DAB voltage balance control: DC-link voltages in case of a power step for  $P_1$  and  $P_2$  (Simulation results)

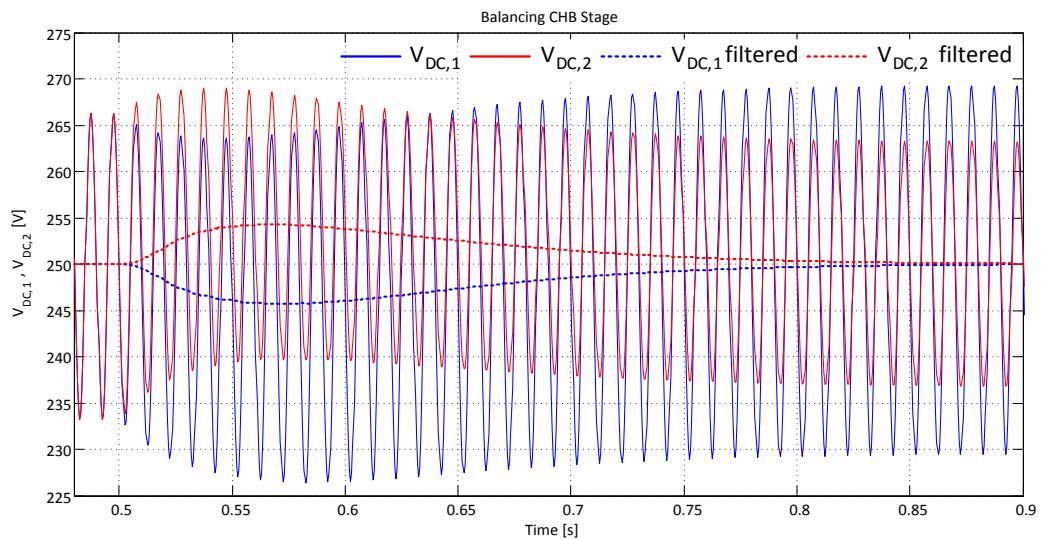


Fig. 4.27: SSBC MMCC voltage balance control: DC-link voltages in case of a power step for  $P_1$  and  $P_2$  (Simulation results)

The results have been confirmed experimentally (Fig. 4.28 and Fig. 4.29), proving the validity of proposed voltage control technique. This suggests to use the voltage balancing method in the DAB stage, because of the large bandwidth of the DAB compared with the SSBC MMCC, and to replace the power control loop in the slower SSBC MMCC stage.

Referring to the voltage balance control operated by the DC/DC power conversion stage, Fig. 4.30 - 4.33 show the output currents of the two DAB converters before and after the power change. Before the change in the reference, the DAB converters provides the same current and their ripples are canceling out each other resulting in a constant overall output current  $I_o = 8A$ . After the variation in the output reference, the output current of the DAB converters are  $I_{o,1} = 6A$  and  $I_{o,2} = 2A$ . As a result of the unequal power sharing between the DAB converters, the currents exhibit high harmonic distortion.

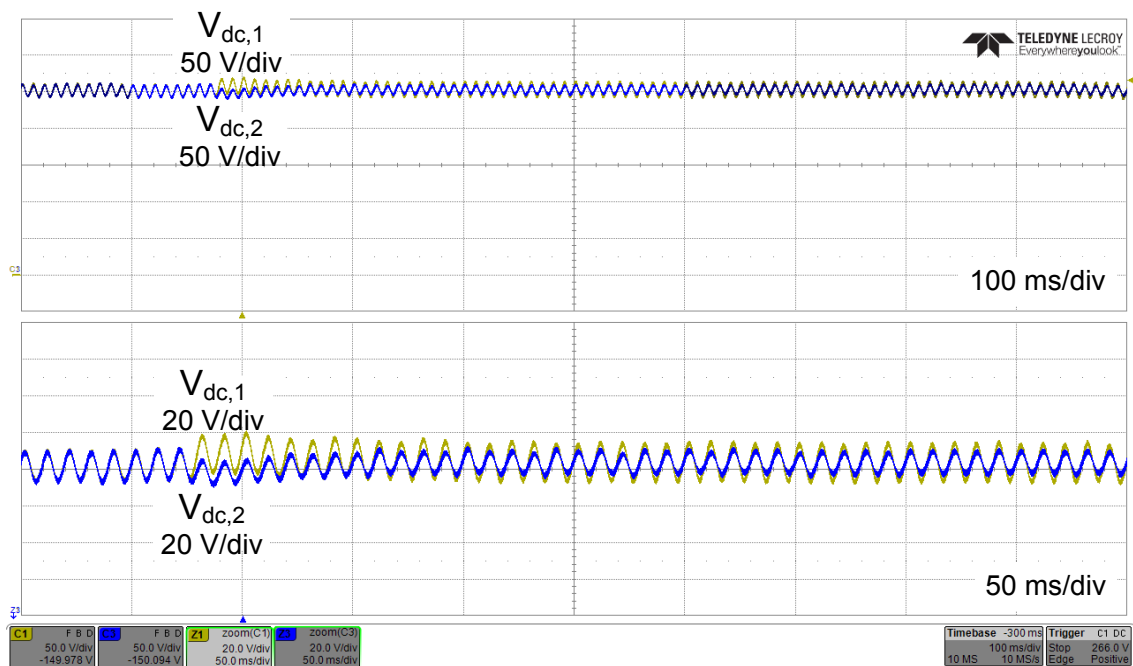


Fig. 4.28: DAB voltage balance control: DC-link voltages in case of a power step for  $P_1$  and  $P_2$   
(Experimental results)

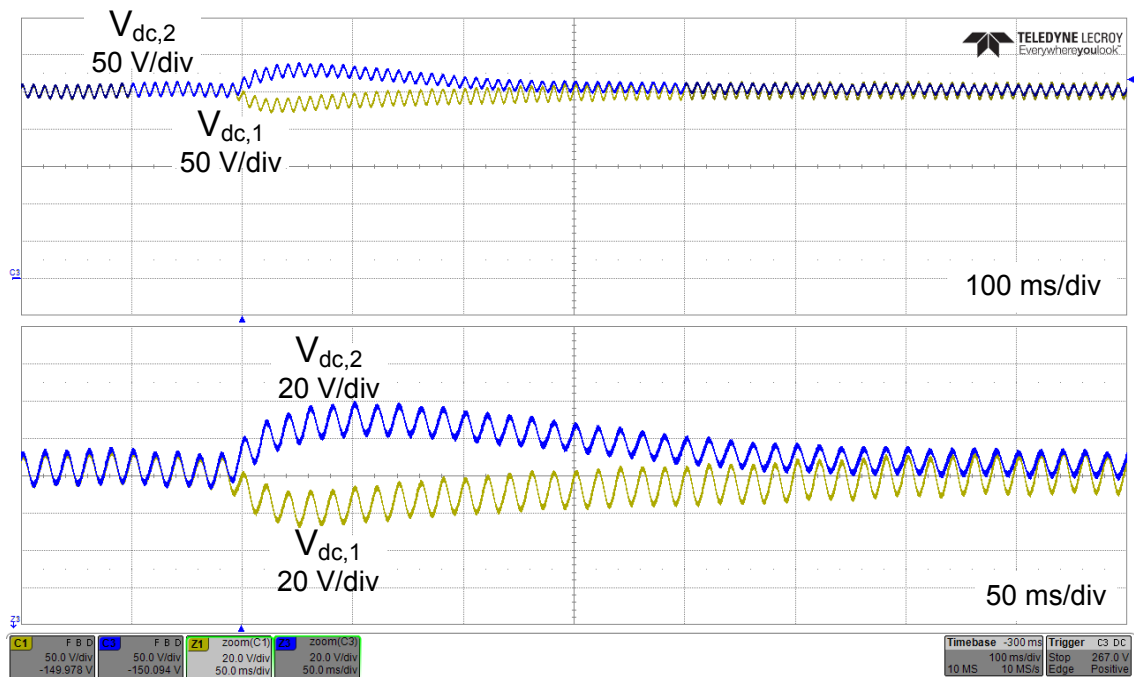


Fig. 4.29: SSBC MMCC voltage balance control: DC-link voltages in case of a power step for  $P_1$  and  $P_2$  (Experimental results)

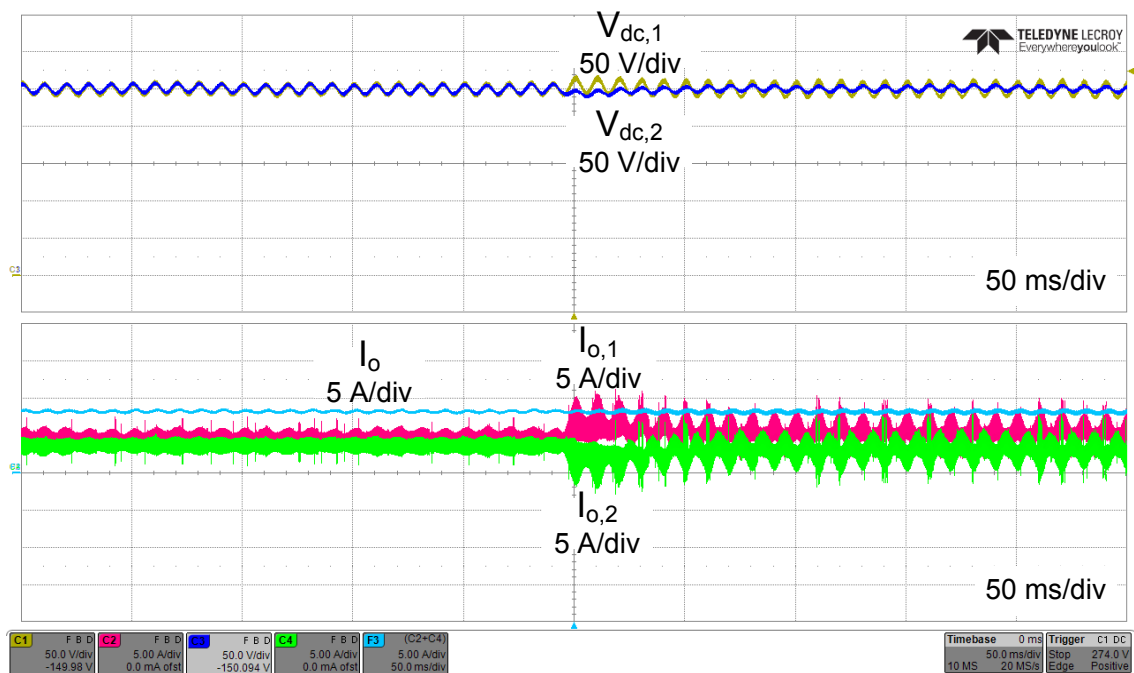


Fig. 4.30: DAB voltage balance control: DAB<sub>1</sub> output current  $I_{o,1}$  (red), DAB<sub>2</sub> output current  $I_{o,2}$  (green), total output current  $I_o$  (light blue).

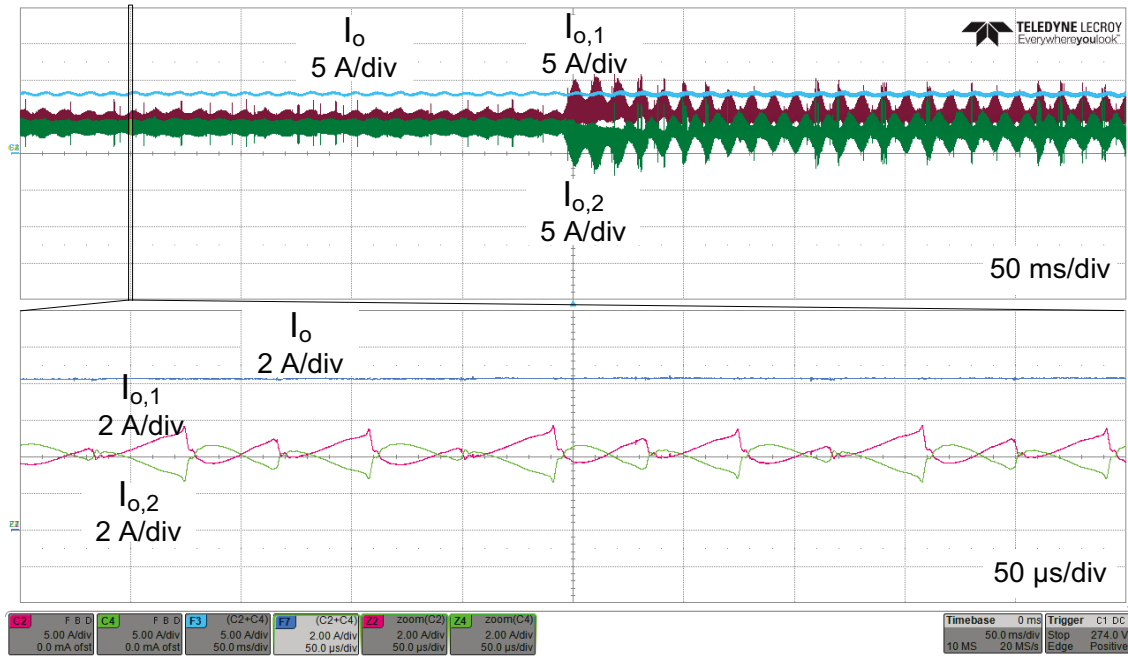


Fig. 4.31: Zoom of the output currents  $I_{o,1}$  (red),  $I_{o,2}$  (green),  $I_o$  (light blue) before the power variation.

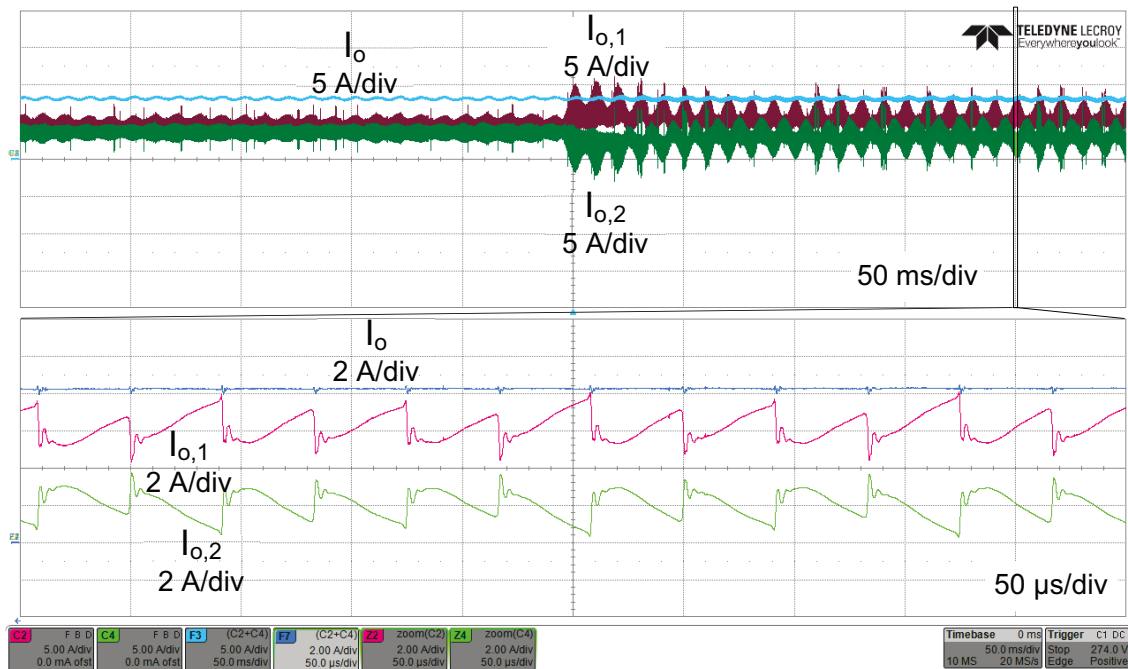


Fig. 4.32: Zoom of the output currents  $I_{o,1}$  (red),  $I_{o,2}$  (green),  $I_o$  (light blue) after the power variation.

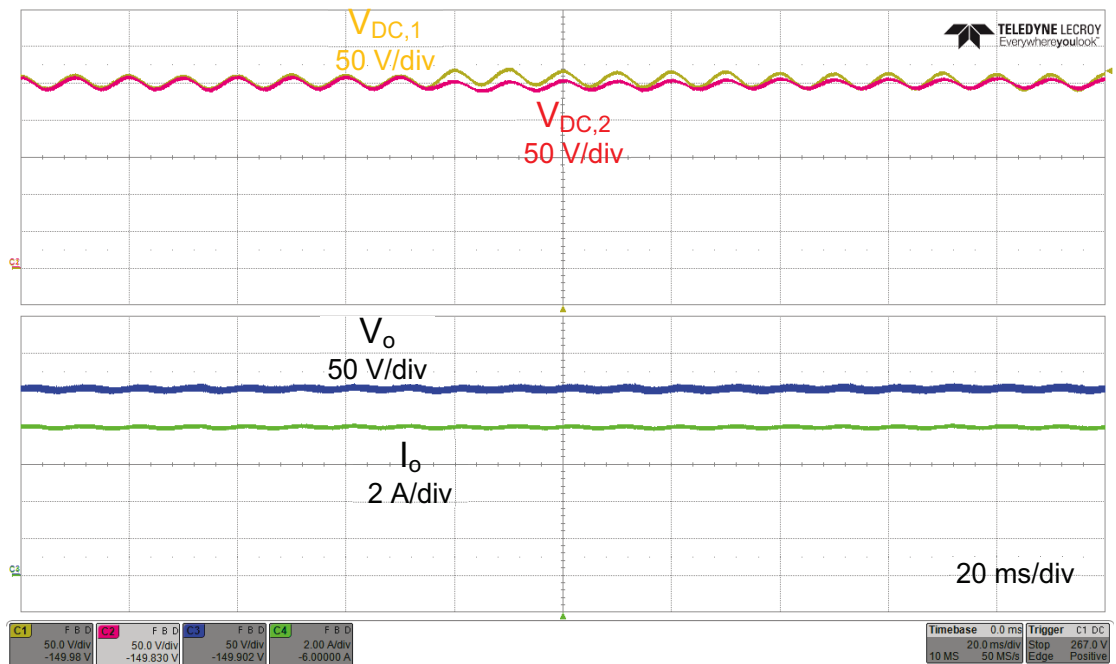


Fig. 4.33:  $V_{DC,1}$  and  $V_{DC,2}$  DC-link voltages (yellow-red);  $V_o$  output voltage (blue) and  $I_o$  current (green) during the power variation.

Finally, the HFT waveforms are represented in Fig. 4.34, where the current in the HFT<sub>1</sub> is compared with that of HFT<sub>2</sub>.

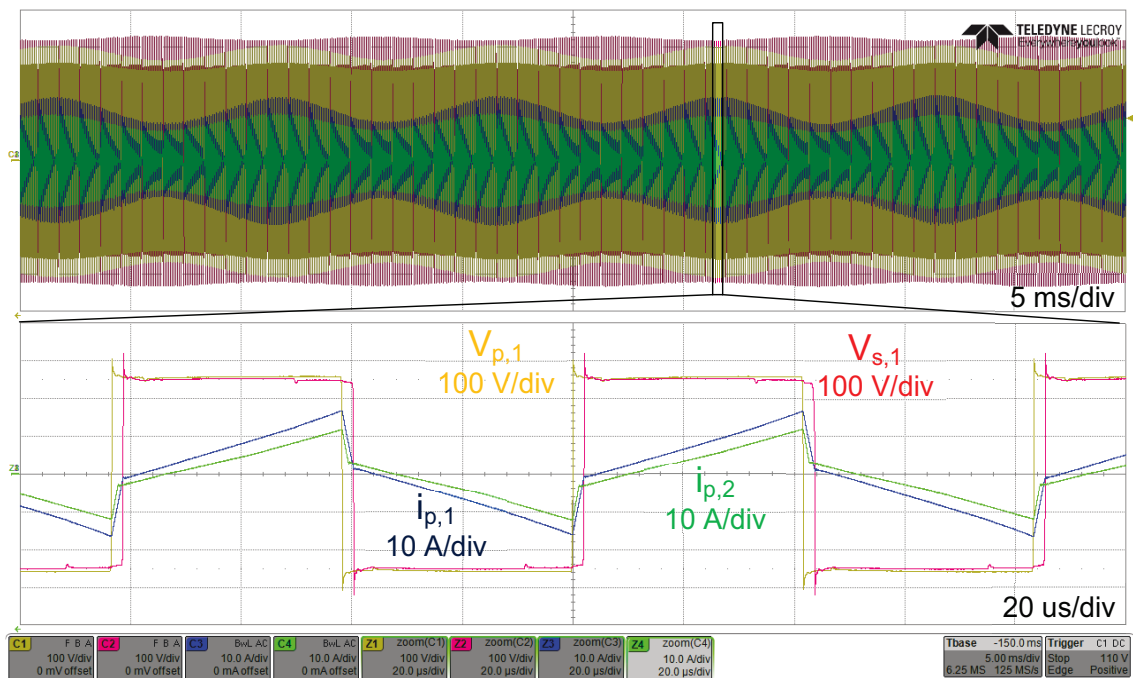


Fig. 4.34:  $V_{p,1}$  primary and  $V_{s,1}$  secondary voltage of HFT<sub>1</sub> (yellow-red), HFT<sub>1</sub> primary side current  $i_{p,1}$  (blue), HFT<sub>2</sub> primary side current  $i_{p,2}$  (green) after the power variation.

#### 4.4 ST: Soft–Start procedure

One of the most important issue in the ST operation is the start-up procedure. In particular, when a ST is turned on, it is required :

1. balancing of the DC-link voltages in the MV side;
2. pre-charging of the capacitors in the LV side;

Due to the mismatch of DC-link MV capacitor parameters, voltage imbalance problems cannot be avoided. If a balance voltage control is not adopted, the deviation of the voltages (and/or currents) may become larger than the IGBT blocking voltage limit and finally may results in the burnout of the IGBT devices. Therefore it is very important to balance the voltage in the ST DC-links. In literature there are many kinds of voltage balancing strategies, but they can essentially classified into two categories:

1. the SSBC MMCC and the DABs are controlled separately; this means that the voltage balance control in MV is demanded in the SSBC MMCC stage, while the DAB converters control the output voltage in the LV side.
2. the ST is controlled as a single converter. None of balance control approaches are adopted by the SSBC MMCC and the MV balance control is demanded to the DABs stage together with the voltage control in LV side.

The first approach to balance the voltage is the most used, but it has several limitations in terms of dynamic response and soft starting capability, compared with the second approach. The traditional start-up control method operates the voltage balance in the SSBC MMCC which starts as first, followed by the DAB converters. Using this procedure, several overvoltages and the capacitor and/or IGBT module burnouts can occur. Indeed, due to the mismatch of the MV resistance and capacitance parameters, the steady state voltages reached by each DC-Link in grid-connected passive rectifier operation, are quite different among them. This means that, before the starting of the SSBC MMCC control, the initial condition in each DC-link is different from the others and the system is in an unbalanced state: the voltage balance condition cannot be achieved before the SSBC MMCC starts. In a such non linear system like the SSBC MMCC, the behavior of the controlled variables during the start-up, depends on its own

particular values in the initial condition. A different initial condition means different and unpredictable behaviors of each DC-Link voltage, which can conduce in unstable and not safe operation.

The second approach, avoid the risk of overvoltages or/and over-currents in the SSBC MMCC because the DAB converters, with integrated voltage balance controller, start before the SSBC MMCC. In this way a perfect voltage balance of the DC-links in MV side is achieved.

Focusing on the second issue, the pre-charging of the capacitors in the LV side is necessary as initial condition to start the control of the DAB converters. When the DAB converters are firstly turned on, the uncharged capacitors act as virtual short circuits allowing a fast increase of the current over the rated and safe operating conditions. At this stage, the starting current is not determined by the controlled phase-shift, but only by the peripheral circuit and its maximum value is directly proportional to the equivalent input voltage. To avoid this potentially harmful current, a pre-charging soft-starting procedure for DAB is proposed [9]. Hence a ST soft-start procedure is proposed in the next sections.

#### 4.4.1 *Soft-Start: First Step*

The first step consists in the connection of the SSBC MMCC to the main grid. At the beginning, the SSBC MMCC works as a passive rectifier without any type of control; no signals are sent to the gate of the switches, and the only conducting devices are the anti-parallel freewheeling body diode. In this condition, no loads are connected to the DC-links in the MV side. The power drained from the main grid is limited to that necessary to supply the MV capacitors  $C_i$ , their internal series resistance  $R_{s,i}$  and the parallel resistance  $R_{p,i}$  (in the order of tens of  $k\Omega$ ) used in the project of the PCB.

In Fig. 4.35 there is represented the entire system, where the 5-levels SSBC MMCC operates as a passive rectifier in grid connected operation. The components in black mark the path of the current, while the devices in gray are turned off.

Due to the mismatch of the capacitance and resistance parameter values, the steady state voltage values in the DC-links are different. This initial condition is clearly visible in

the left-side of Fig. 4.36, where  $V_{DC,1}$  and  $V_{DC,2}$  are quite different and the system is unbalanced; in the same figure the grid current is shown in green and it is negligible.

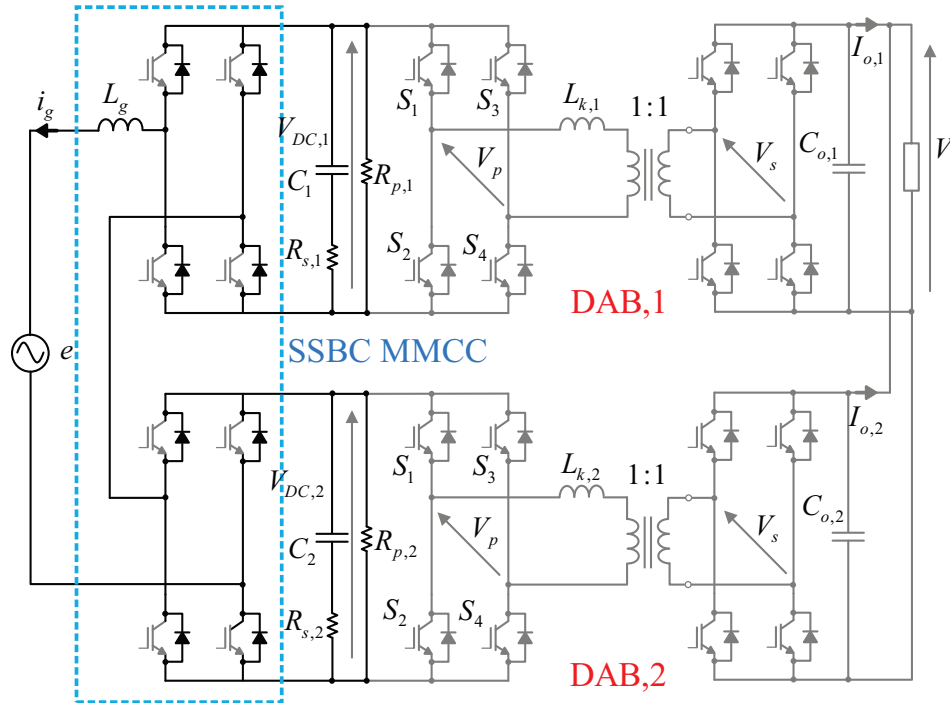


Fig. 4.35: ST with a 5-levels SSBC MMCC passive rectifier in grid connected operation.

The effect of the parameters mismatch is amplified at no load operation and it results in a huge voltage imbalance (Fig. 4.36).

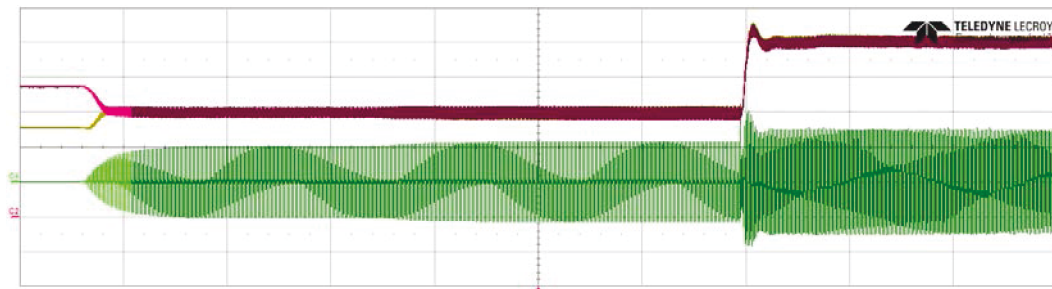


Fig. 4.36: Soft-Start - DC-Link voltages  $V_{DC,1}$  (yellow),  $V_{DC,2}$  (red) and grid current (green) in first step.

#### 4.4.2 Soft-Start: Second Step

The aim of the second step is to reduce the voltage imbalance, which results from the first step, through a balancing procedure operated by DAB converters. In [10] a similar approach has been proposed, without taking into account the occurrence of over current

during the turn on of the DAB converters, in case of no pre-charging of the output capacitor  $C_o$ . As discussed before there is no way to reduce the maximum inrush current value just adjusting the phase shift between the two bridges of the DAB. But controlling the zero state operation in primary and secondary voltages of the HFT is possible to control the current. Considering the configuration shown in Fig. 4.35, the zero voltage state can be obtained applying an independent switching law between two legs of the same H-Bridge, as in Tab. 4.2.

Tab. 4.2: DAB Switching table - Unipolar modulation.

$S_1$	$S_2$	$S_3$	$S_4$	$V_p$
1	0	0	1	$V_{DC}$
0	1	1	0	$-V_{DC}$
1	0	1	0	0
0	1	0	1	0

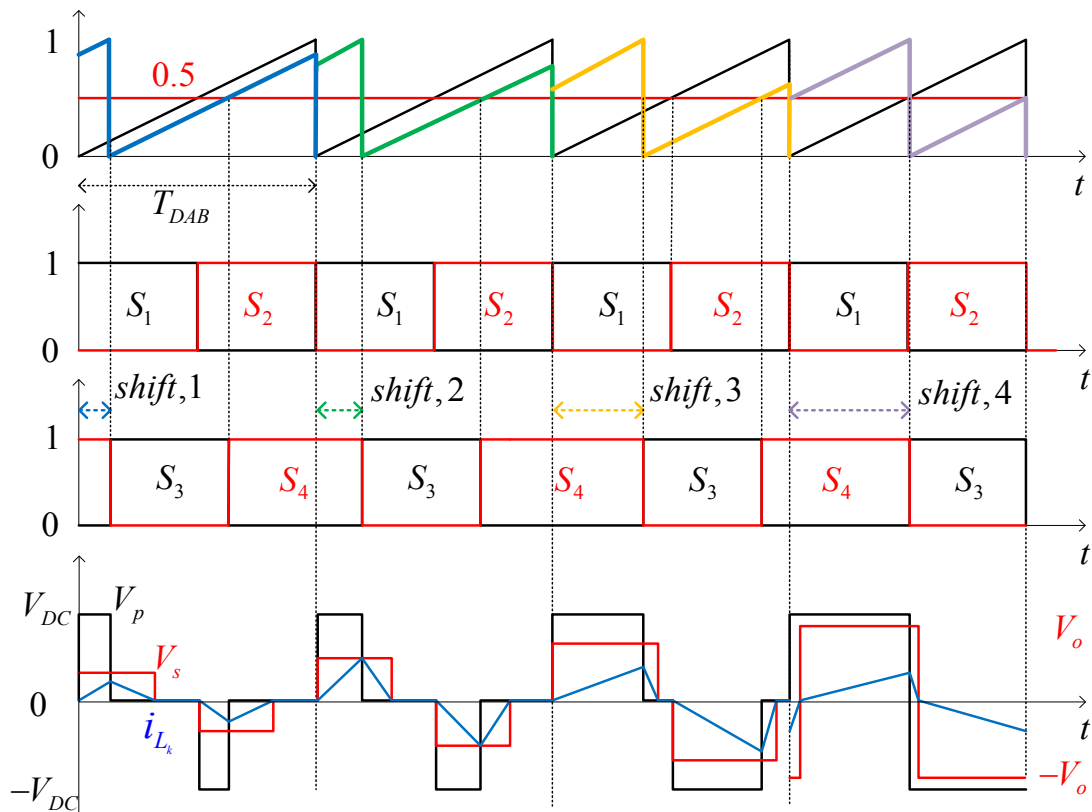


Fig. 4.37: DAB - Typical HFT waveforms during Soft-Shift Start.

The zero voltage state, as shown in Fig. 4.37, can be obtained shifting the carrier of the leg B respect to the carrier of the leg A. In such way, when in a switching period  $T_{DAB}$ , both  $S_1$  and  $S_3$  are turned ON or OFF, the voltage in the primary side of the HFT is zero. In Fig. 4.37, the switching signals related to the first bridge of the DAB converter are represented in four different shift cases; the related primary and secondary voltages and the current during the start-up procedure are shown in the same figure. For each DAB, when the first bridge of the DAB is turned on, the secondary side bridge is kept off. The switches in the primary side are driven as in Fig. 4.37, varying the time shift from zero to  $T_{DAB} / 2$  with a ramp signal. The current through the leakage inductance appears in a discontinuous conducting mode because of the zero voltage stage; the current charges and discharges the inductance very fast and high current value cannot be reached, avoiding the burnout of the IGBTs. During the second step of the soft-start procedure, the second bridge of the DAB works as a full diode bridge rectifier (Fig. 4.38), and the power transferred through the HFT pre-charges the output capacitor up to a voltage value which depends on the value of the input voltage, on the voltage drops across the semiconductor and on the transformer internal resistance.

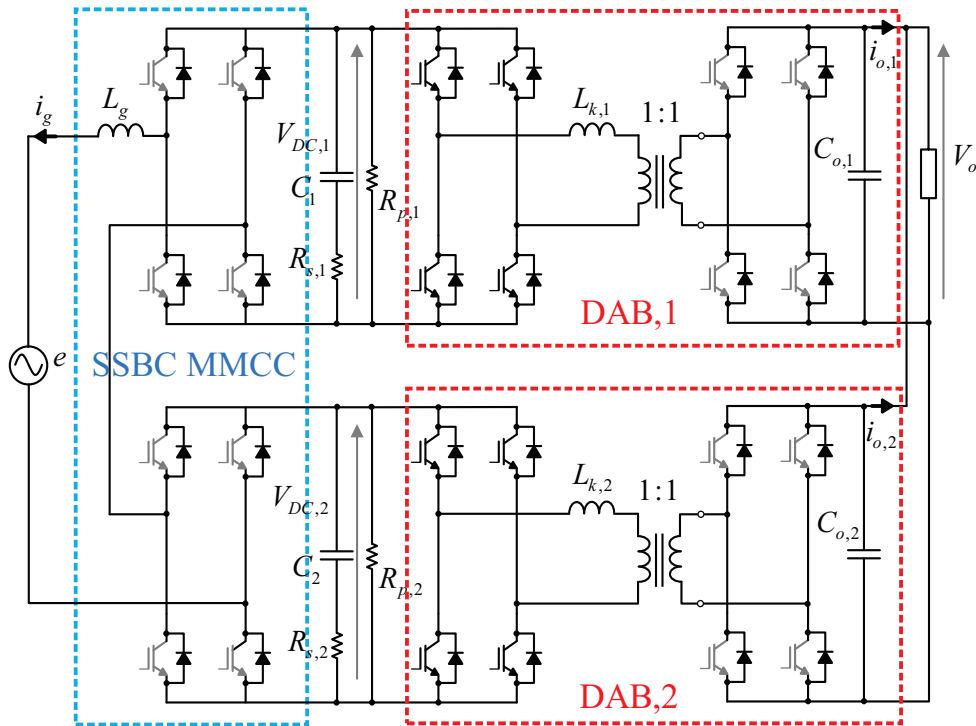


Fig. 4.38: ST during the second step of the Soft-start procedure.

In Fig. 4.38, a DC load is connected in parallel to the output capacitors; the pre-charging voltage induces current circulation into the load and a certain amount of power flows from the grid to the DC load.

In Fig. 4.39, the primary and secondary side voltages of the HFT are represented together with the leakage current for three different values of the time shift.

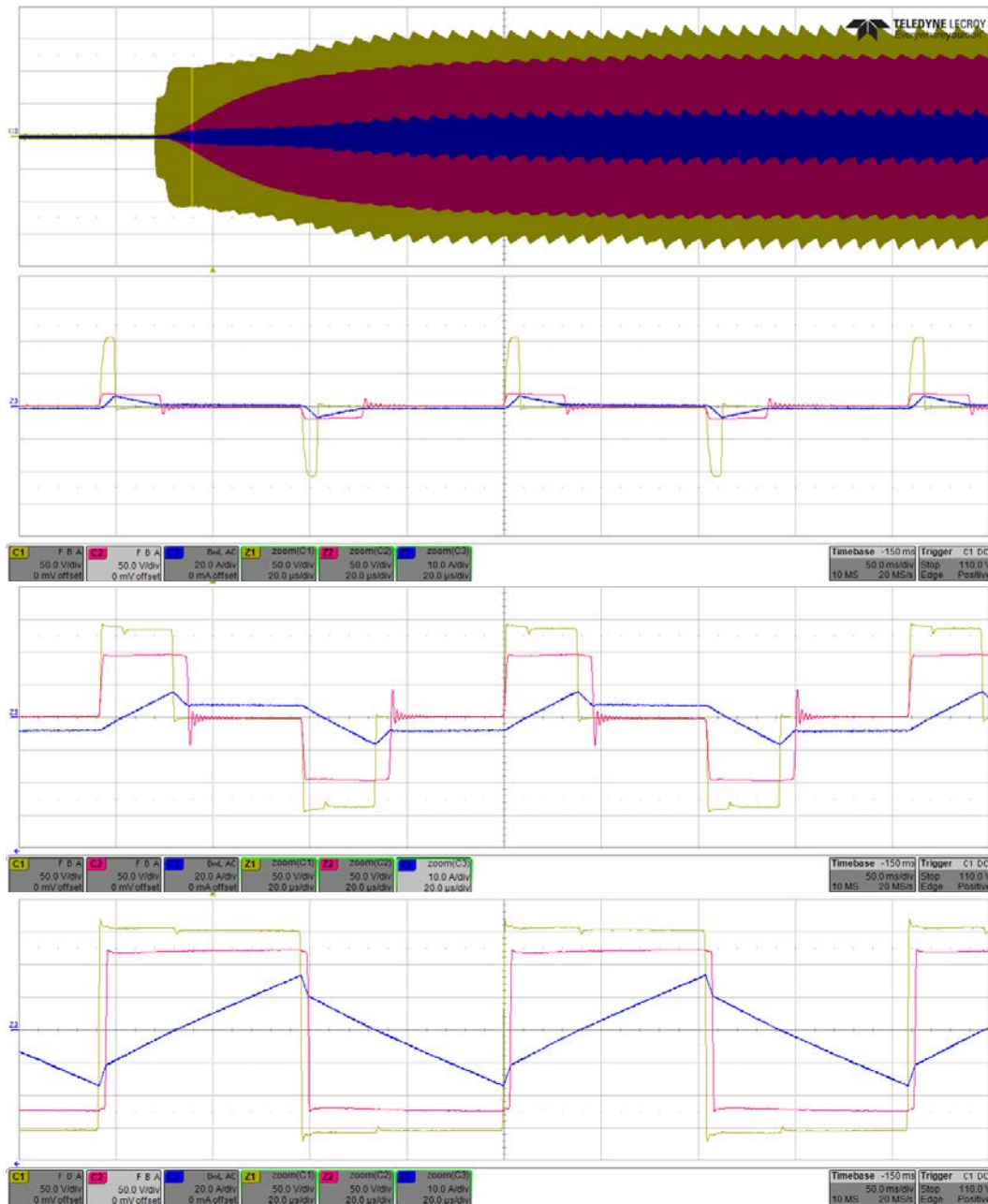


Fig. 4.39: HFT Primary (yellow) and secondary (red) side voltages, leakage current (blue).

The SSBC MMCC in the second step is still working as a passive rectifier and the grid current has the distorted waveform which is typical of a full diode bridge connected to grid (Fig. 4.40). The grid current increases slowly and it avoids overcurrents in the SSBC MMCC converter.

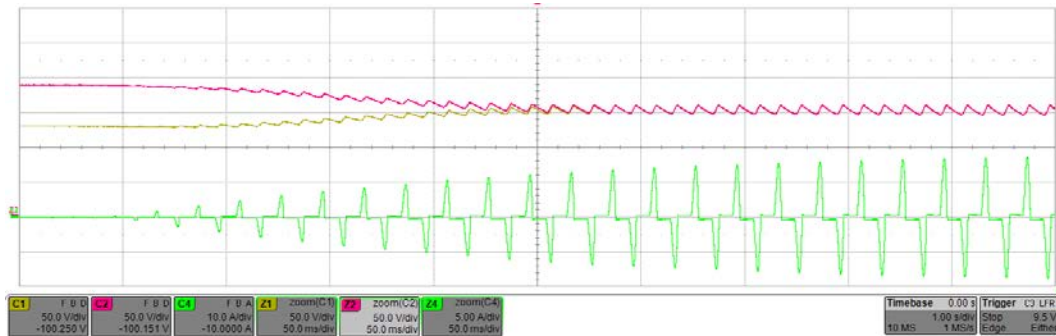


Fig. 4.40: DC-link voltages  $V_{DC,1}$  (yellow),  $V_{DC,2}$  (red) and grid current (green) in second step.

The output voltage in Fig. 4.41 and leakage inductance current have the same behavior of the grid current. The velocity of the pre-charging process depends on the slope of the ramp used to increase the time shift between the two carrier signals of the first H-Bridge in each DAB converter.

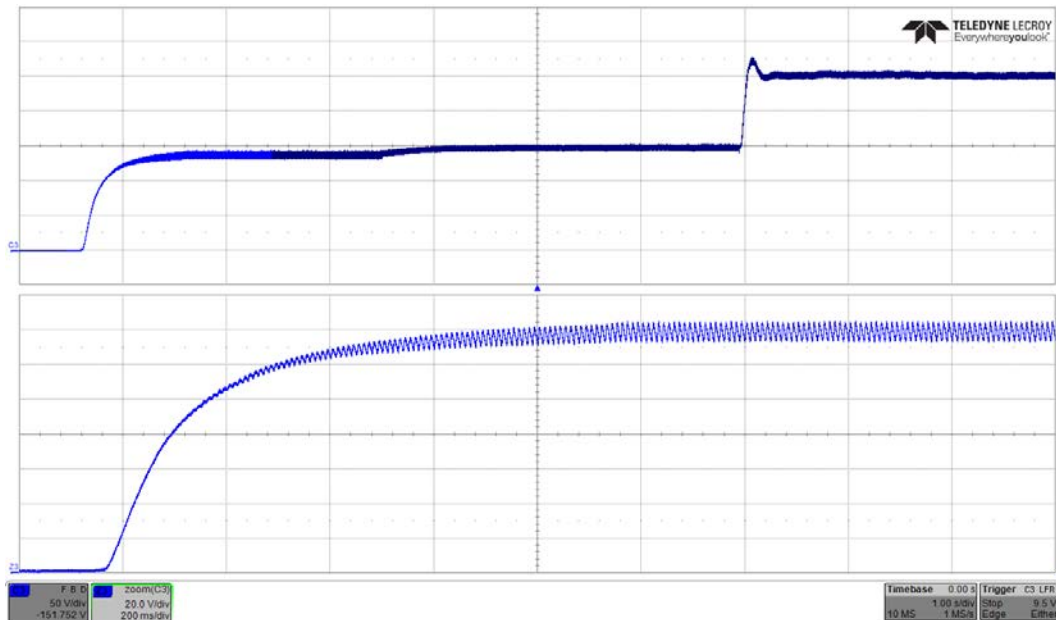


Fig. 4.41: DAB output voltage  $V_o$  during the second step.

Another important effect of this second step is the convergence of the DC-link voltages to a new steady-state point, as shown in Fig. 4.40. In this new load condition, the

parameters mismatch, between the different power modules, corresponds in a smaller voltage imbalance if compared with previous step, where the system was in no-load operation. This new steady-state leads to the next step.

#### 4.4.3 *Soft-Start: Third Step*

Due to the voltage drops across the devices of the first H-Bridge, across the HFT and across the body diodes of the second H-Bridges, the DAB converters output voltage value is lower than the input rectified voltage. In order to compensate this voltage drop, a proper action on the control of the output voltage is required. Turning on the switches in the second H-bridge and adjusting properly the value of  $\varphi$  (phase shift control variable), the control of  $V_o$  can be achieved. The reference is slowly varied up to  $V_o^*$ , which can be set as:

$$V_o^* = \frac{V_{DC,1} + V_{DC,2}}{2} \quad (4.30)$$

In Fig. 4.42 the output voltage is represented when a slow reference ramp is applied and finally the rectified average input voltage has been reached. When the output voltage reaches the new steady-state, the voltage balance control is turned on. The balancing is performed in the DABs, adjusting properly the phase shift,  $\varphi_1$  and  $\varphi_2$ .

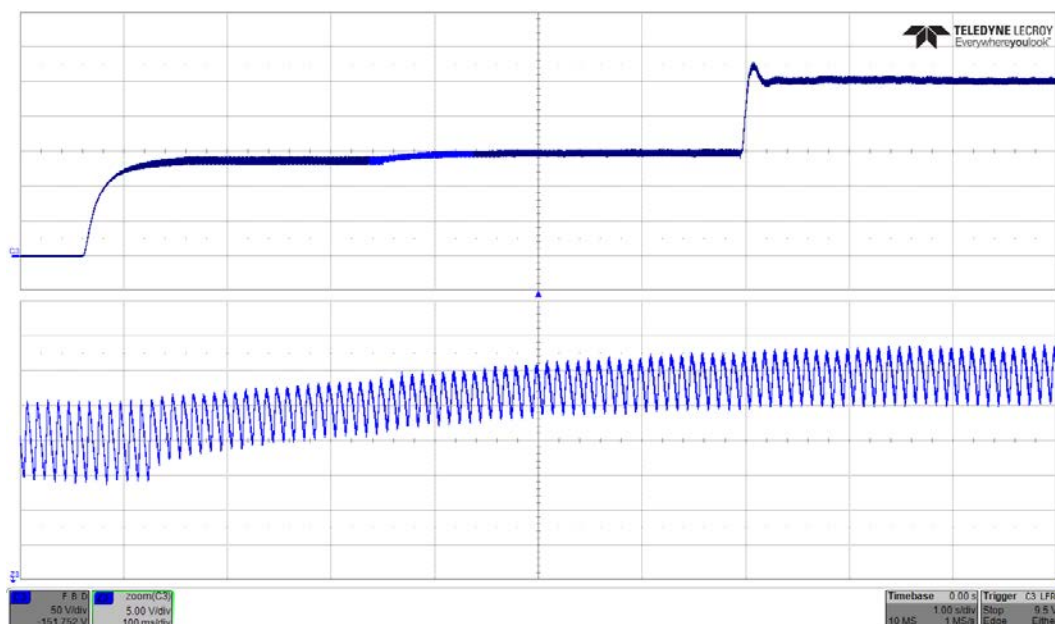


Fig. 4.42: Output voltage response to a slow ramp reference during the soft-start third step.

#### 4.4.4 Soft-Start: Fourth Step

In the fourth step, the following conditions are verified: the DC-link voltages are perfectly balanced by the DAB converters controllers, the output voltages of the DAB converters are also controlled and the output voltage controller (PI controller) is tuned to be around ten times faster than the SSBC MMCC voltage controller.

In a such way the output voltage reference  $V_o^*$  can be set as in the third step and the secondary bridges behave similarly to the primary bridges for each DAB. The balance is verified all the transient and dangerous overvoltage and/or over current are avoided. When the desired DC-link voltage is reached, the output voltage reference is set to its rated value:

$$V_o^* = \bar{V}_o \quad (4.31)$$

The DC-links voltages  $V_{DC,1}$  and  $V_{DC,2}$  during the step variation from the rectified to the desired voltage are represented in Fig. 4.43, together with the grid current. The output voltage  $V_o$  is represented in Fig. 4.44.

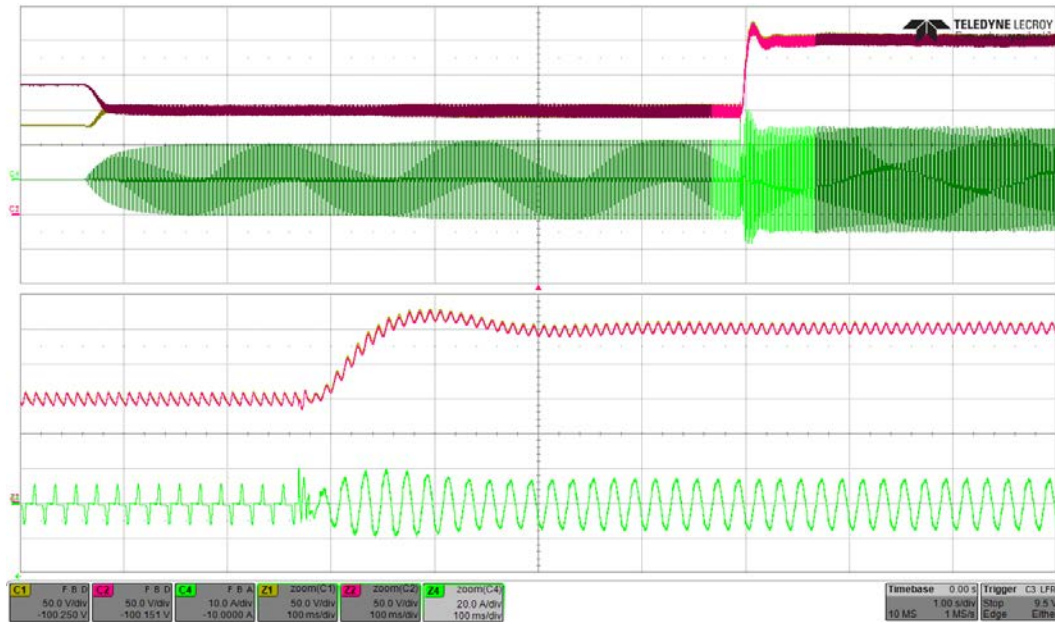


Fig. 4.43: DC-link voltages  $V_{DC,1}$  (yellow),  $V_{DC,2}$  (red) and grid current (green) during the step from passive to active rectifier operation.

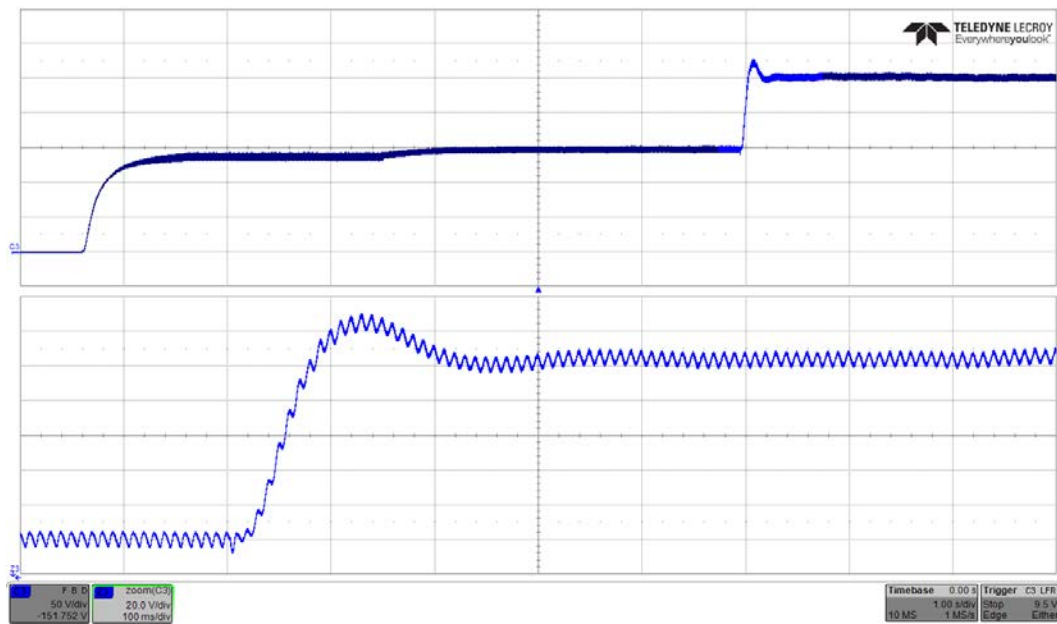


Fig. 4.44: Output voltage  $V_o$  during the step from passive to active rectifier operation.

In Fig. 4.45, the ST DC-link voltages, the output voltage and the grid current are represented during the entire Soft-Start procedure.

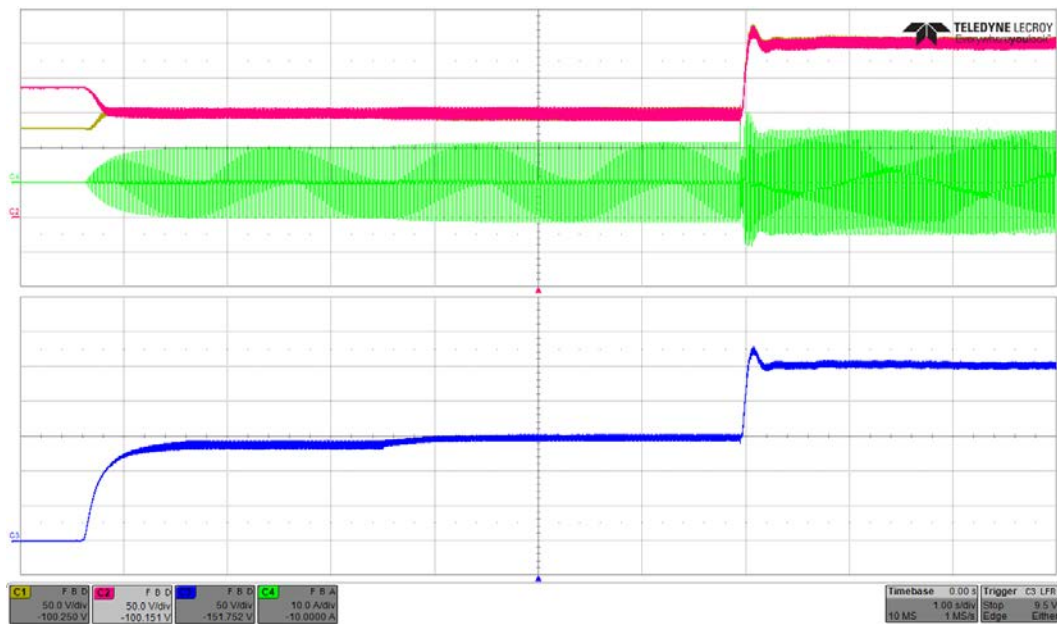


Fig. 4.45: DC-link voltages  $V_{DC,1}$ ,  $V_{DC,2}$ , grid current  $i_g$  and output voltage  $V_o$  during the entire Soft-Start procedure.

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## Conclusion

The rapid growth of renewable energy technologies, such as solar photovoltaic and wind turbines, are changing the nature of transmission, distribution and utilization of electrical energy. Most of the electrical loads-lighting, adjustable speed motors, brushless DC motors, computing and communication equipment are more compatible with DC power. Some distributed renewable energy generator including photovoltaics and fuel cells produce DC voltage. Thus DC power exhibits a great potential compatibility with high-penetration distributed power generation systems.

Trying to foresee the possible future scenarios of the power systems, it can be noticed that DC Smart Grids enable interconnection of different kind of sources requiring different voltage levels due to integration of different renewable sources, loads and energy storage devices. In this scenario the Single-Star-Bridge-Cell Modular Multilevel Cascade Converter and the Dual Active Bridge Converters allow a flexible connection of DC sources and loads with the main AC grid providing advanced control functionalities to the system. The control structure proposed in the thesis guarantees proper operation up to 50% of power imbalance among the different power cells. Besides the combination a Single-star-Bridge-Cell Modular Multilevel Cascade Converter with several Dual Active Bridge Converters extends the possible voltage range operation ensuring galvanic isolation and avoiding faults propagation between the AC and the DC sides.

The proposed power converter topologies have been applied also to other applications: a More Electric Aircraft and a Smart Transformer with the possibility to integrate inside also SiC power devices instead of Si devices in order to increase the power density. This possibility should be further investigated in a future work.

A new voltage balance control has been proposed for the proposed power stage. The peculiarity is that the voltage balance function is in charge of the Dual Active Bridge converters instead of the Modular Multilevel Cascade Converter. The proposed solution allows higher bandwidth than the traditional solution and, as a consequence, it ensures

better dynamic performances. The validity of the designed control method has been proven also in case of start-up procedure and it represents one of the main innovative contributions of the dissertation.

## List of Publications

### *Journal Articles:*

- Á. Molina-García, R. A. Mastromauro, T. García-Sánchez, S. Pugliese, M. Liserre, S. Stasi: “*Reactive Power Flow Control for PV Inverters Voltage Support in LV Distribution Networks*”. IEEE Transactions on Smart Grid, 8(1), 447-456, 2017.

### *National Conference Articles:*

- S. Stasi, F. Cupertino, R. A. Mastromauro, M. C. Poliseno, F. A. Gervasio, S. Pugliese: “*Ambition Power: Design and Construction of Si- and SiC-Based Power Converters Demonstrators for Aircraft, Automotive, Industrial and Photovoltaic Applications*”. 01/2014: chapter 1st Workshop on the State of the Art and Challenges of Research Efforts at POLIBA: pages 287-297; Gangemi Editore, ISBN: 978-88-492-2964-6.
- R. A. Mastromauro, D. Ricchiuto, S. Pugliese, M. Liserre: “*DC SmartGrids: il ruolo del convertitore Cascaded H-Bridge per la realizzazione di un Multibus in DC*”, Convegno Annuale AEIT 2014, Trieste, Settembre 18-19-2014, ISBN: 9788887237252.

### *International Conference Articles:*

- R. A. Mastromauro Rosa, S. Pugliese, S. Stasi: “*An Advanced Active Rectifier based on the Single-Star Bridge Cells Modular Multilevel Cascade Converter for More-Electric-Aircrafts Applications*”. ESARS 2015 – IEEE 3rd International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles, Aachen - Germany; 03/2015.
- R. A. Mastromauro, M. C. Poliseno, S. Pugliese, F. Cupertino, S. Stasi: “*SiC MOSFET Dual Active Bridge Converter for Harsh Environment Applications in a More-Electric-Aircraft*”. ESARS 2015 – IEEE 3rd International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles, Aachen - Germany; 03/2015.
- R. A. Mastromauro, S. Pugliese, D. Ricchiuto, S. Stasi, M. Liserre : “*DC Multibus based on a Single-Star Bridge Cells Modular Multilevel Cascade Converter for DC Smart Grids*”. ICCEP 2015 – IEEE 5th International Conference on Clean Electrical Power (Renewable Energy Resources Impact), Taormina, Italy; 06/2015.

- S. Pugliese, S. Stasi, R. A. Mastromauro: “*Simplified Feedback Linearization Control of a Single-Phase Photovoltaic NPC Converter in Direct-Quadrature Rotating Reference Frame*”. 4th International Conference on Renewable Energy Research and Applications, Palermo - Italy; 11/2015.
- R. A. Mastromauro, S. Pugliese, S. Stasi: “*Universal Operation of a Distributed Power Generation System Based on the Power Converter Control*”. IEEEIC 2016, Florence - Italy; 06/2016.
- S. Pugliese, R. A. Mastromauro, F. A. Gervasio, S. Stasi: “*Performance comparison of simplified feedback linearization control with classical dual loop control for a single-phase grid-connected inverter*”. IECON 2016, Florence - Italy; 10/2016.
- S. Pugliese, R. A. Mastromauro, S. Stasi. “*270V/28V wide bandgap device-based DAB converter for more-electric-aircrafts: Feasibility and optimization*”. Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC), International Conference on. IEEE, Toulouse – France; 11/2016.
- S. Pugliese, M. Andresen, R. Mastromauro, G. Buticchi, S. Stasi, M. Liserre: “*Voltage Balancing of Modular Smart Transformers Based on Dual Active Bridges*”. IEEE ECCE, Energy Conversion Congress and Exposition, Cincinnati, OH – USA, 10/2017.