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Research Article

Design and Optimization of Polarization Splitting and Rotating Devices in Silicon-on-Insulator Technology

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We review polarization splitting and rotating photonic devices based on silicon-on-insulator technology platform, focusing on their performance and design criteria. In addition, we present a theoretical investigation and optimization of some rotator and splitter architectures to be employed for polarization diversity circuits. In this context, fabrication tolerances and their influences on device performance are theoretically estimated by rigorous simulations too.

1. Introduction

In the last few years, silicon-on-insulator (SOI) technology platform has been widely used for the fabrication of integrated photonic devices to be employed for several applications such as high-speed data processing and optical sensing [1–3].

In this context, integrated silicon photonic devices exhibit some unique and considerable advantages with respect to other material systems and technology platforms (e.g., III–V compounds and alloys) suitable for photonic device fabrication. Among all, it is noteworthy to mention that silicon photonic devices are CMOS (complementary metal-oxide semiconductor) compatible with standard microelectronics technology facilities and thus able to large scale integration and low cost fabrication. In addition, the high refractive index contrast (i.e., $\Delta n \approx 2$) between silicon (Si) and its oxide (SiO_2) in C and L bands (i.e., 1530–1625 nm according to ITU standard) allows for fabricating ultracompact silicon photonic devices and circuits characterized by overall footprint dimensions of a few μm $\times$ μm [4]. On the other hand, photonic devices suffer from large transverse electric-transverse magnetic (TE-TM) polarization birefringence because of the high refractive index contrast mentioned above [5, 6]. Consequently, polarization mode dispersion (PMD), polarization dependent loss (PDL), and polarization dependent wavelength (PDλ) represent considerable and not negligible drawbacks that limit device performance and compromise its operation [7]. In addition, the dependence on polarization imposes very strict fabrication tolerances for silicon photonic devices. For example, by considering a photonic filter based on a 10 μm radius ring resonator with 300 nm wide silicon waveguide, the fluctuation of the core width of only 1 nm (i.e., 300 $\pm$ 1 nm) induces a difference of the resonant wavelength between TE mode and TM mode larger than 100 GHz [8]. Therefore, the accuracy improvement of technological processes, such as electron-beam (e-beam) lithography and reactive ion etching (RIE), as well as the design of silicon photonic devices characterized by zero birefringence, represents a suitable approach to minimize the dependence of microphotonic silicon device performance on the polarization of the incoming light [9]. Other solutions have been also proposed, such as the use of high birefringent silicon nitride (Si_3N_4) bent waveguides on SOI platforms [10], the control of SOI waveguide birefringence by inducing stress in cladding layers [11] or in silicon core [12], or the depositing of thin doped top layer onto silicon wafer [13]. However, the subnanometer accuracy and other specific technological

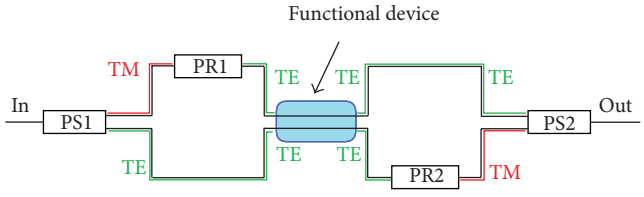


FIGURE 1: Schematic of a polarization diversity photonic circuit [14].

solutions (e.g., the use of stressed or doped layers) are not always suitable for large scale integration and low cost fabrication.

Actually, the polarization diversity scheme is generally adopted as the optimal approach for solving the problem of the polarization dependence affecting high refractive index contrast SOI photonic devices [14–20]. For this purpose, the principle of operation of a polarization diversity circuit can be analyzed according to the schematic proposed in Figure 1.

The configuration sketched in Figure 1 represents basic architecture of a polarization diversity circuit consisting of polarization splitters (PSs) and rotators (PRs) [21–23]. In particular, at the input section the orthogonal polarization components of the input light are split into two different waveguides by using a polarization splitter (i.e., PS1). Consequently, a polarization rotator (i.e., PR1) is employed in one of the waveguides to obtain a 90° rotation. In this way, a single polarization is achieved and the two paths may be operated in parallel with identical structures. In this case, the functional device operates with only TE polarized optical signals. For example, it could be a polarization-sensitive microring resonator employed for optical signal processing such as filtering or add-drop multiplexing. At the output section, a symmetrical configuration consisting of a polarization rotator (i.e., PR2) and one polarization splitter (i.e., PS2) can be implemented in order to combine the two polarizations without any interference. In conclusion, spot-size converters (SSC) can be also employed at both input and output sections for coupling the optical signal from the input fibre to the circuit and vice versa. Finally, by considering the schematic shown in Figure 1, a reciprocal configuration can be designed so that the functional device operates with only TM polarized optical signals.

In Section 2, recent polarization splitting and rotating SOI devices are presented and described as fundamental building blocks of polarization diversity circuits. In particular, main operation principles of such device architectures are discussed in deep, focusing on polarization splitting and conversion performance as well as on design criteria.

Finally, in Section 3 some of the polarization splitters and rotators analyzed in Section 2 are investigated and simulated, including a useful comparison and focusing on the influence of fabrication tolerances on device performance.

2. Polarization Splitting and Rotating Devices in SOI Technology Platform

Nowadays, the capability to control and manipulate the polarization state of optical signals is ensured by the use of polarization mode converters (PMCs). Generally, it is possible to distinguish between two PMC categories: those based on adiabatic mode evolution [24] and those based on mode interference (e.g., mode coupling). In particular, the former are characterized by long device lengths with relaxed fabrication tolerances and wide operative bandwidth. On the contrary, PMCs based on mode interference are very sensitive to operative wavelength and integrated guided-wave geometries, resulting in more severe dimensional tolerances. Moreover, among mode interference PMCs, those ones based on asymmetric periodically load waveguides were some of the first ones that have been introduced and investigated. Recently, Bayat et al. [25] have proposed their application, taking advantage of the interesting properties of photonic crystals on the standard SOI technology platform.

The comparison among different PMCs can be supported by the use of specific parameters such as the polarization extinction ratio (PER) and the polarization conversion efficiency (PCE) defined as follows:

$$\mathrm{PER} = 10\log_{10}\left(\frac{P_c}{P_{nc}}\right)\,[\mathrm{dB}]\,,$$
$$\mathrm{PCE} = \left(\frac{P_c}{P_c + P_{nc}}\right)\cdot 100\,[\%]\,. \tag{1}$$

In (1), P_c is the output power of the optical signal whose polarization has been converted by using a PR, while P_{nc} is the output power of the orthogonal mode (i.e., the mode whose polarization is 90° with respect to the converted signal). In addition, performance of polarization beam splitters and rotators can be also compared in terms of insertion losses (ILs), defined as

$$\mathrm{IL}_i = 10\log\left(\frac{P_i^i}{P_{\mathrm{IN}}^i}\right)\,[\mathrm{dB}]\,,\qquad i = \mathrm{TE},\mathrm{TM}, \tag{2}$$

where P_{IN}^i is the power of the i polarized mode at the PS input port.

The first device considered in this section is a mode-evolution-based PR in SOI technology proposed by Zhang et al. [26]. The photonic waveguide is characterized by a silicon core with refractive index $n_{\mathrm{Si}} = 3.5$ at the operative wavelength $\lambda = 1.55\,\mu$m, surrounded by silicon dioxide ($n_{\mathrm{SiO_2}} = 1.45$ @ $1.55\,\mu$m). The PR sketched in Figure 2 is characterized by an input section consisting in a 400 nm (height) × 200 nm (width) silicon waveguide. In the middle, a transition region is created by tapering the silicon waveguide up to the output section, where the waveguide cross-section is 400 nm (width) × 200 nm (height).

As shown in Figure 2, the optical mode distribution at the input waveguide is quasi-TM polarized. For this purpose, 2D Finite Element Method (FEM) based modal investigation has been carried out for the calculation of the optical mode spatial distributions [27]. Beyond the input section, the optical signal polarization is forced to rotate while the signal is propagating along the transition region, in a highly asymmetrical waveguide. For this purpose, the design of the transition region has to be executed in order that the overall

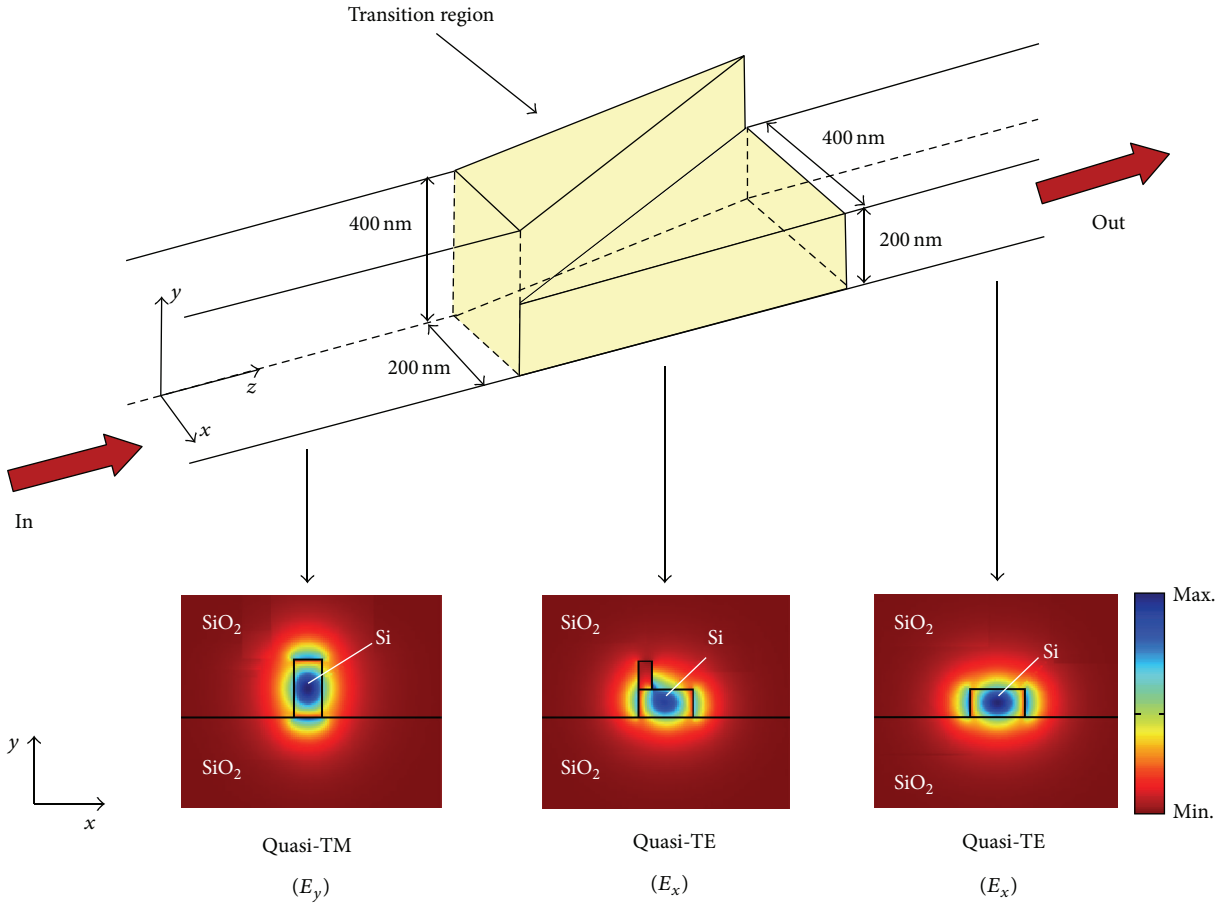


FIGURE 2: Mode-evolution-based polarization rotator in SOI technology with simulations of optical mode spatial distributions in different device cross-sections, in case of TM-TE polarization conversion.

polarization rotation at the end of the transition region is 90°, according to

$$\sum_{n=1}^{N} 2\Delta\varphi_n = 90^\circ, \tag{3}$$

where $\Delta\varphi_n$ is the angle between the propagation direction and the polarization of the incident light at the nth waveguide cross-section along the transition region, assuming N intermediate cross-sections for FEM simulation. At the end of the device, the optical signal is efficiently converted, resulting in a quasi-TE polarized mode distribution concentrated in the output symmetrical silicon waveguide. The device can operate in reverse condition, allowing a polarization rotation from quasi-TE to quasi-TM mode. In fact, the TM mode in the horizontal waveguide also matches with the effective refractive index of TE mode in vertical waveguide. Consequently, launching either quasi-TM or quasi-TE mode at the input section of the PR, polarization rotation effect is performed. It is noteworthy to mention that a rigorous design and an accurate fabrication of the transition region are fundamental requirements in order to obtain low loss and efficient rotation, as well as the effective refractive index matching between propagating modes in the input and output waveguides. For this purpose, Zhang et al. have theoretically and experimentally demonstrated a PER as high as 15 dB in case of TE-TM conversion and IL < 1 dB at the transition region, with a PR characterized by an overall length of 40 μm. The wavelength dependence has been proved to be not significant in the spectral range from 1450 to 1750 nm, reveling less than 2 dB extinction ratio decrease in TM-TE conversion and less than 1 dB in TE-TM conversion. From a technological point of view, the silicon PR based on two-layer silicon waveguide structure has been processed by two-step dry etching, resulting in a complex device fabrication. In fact, the effect of misalignment between the two layers used in the PR fabrication can decrease the rotation performance. In conclusion, the efficient PR proposed in [26] exhibits better performance in case of TE-TM polarization conversion with overall IL of 3 dB and large fabrication tolerances.

A similar PR based on mode evolution in SOI technology has been designed, fabricated, and characterized by Wirth et al. [28]. The device is characterized by an architecture similar to that previously sketched in Figure 2. However, in this case optimized waveguide dimensions are 500 nm (height) × 250 (width) and 500 nm (width) × 250 (height), in input and output sections, respectively. The PR with overall length of 37.5 μm exhibits a PER for TM to TE rotation between 17.8 dB

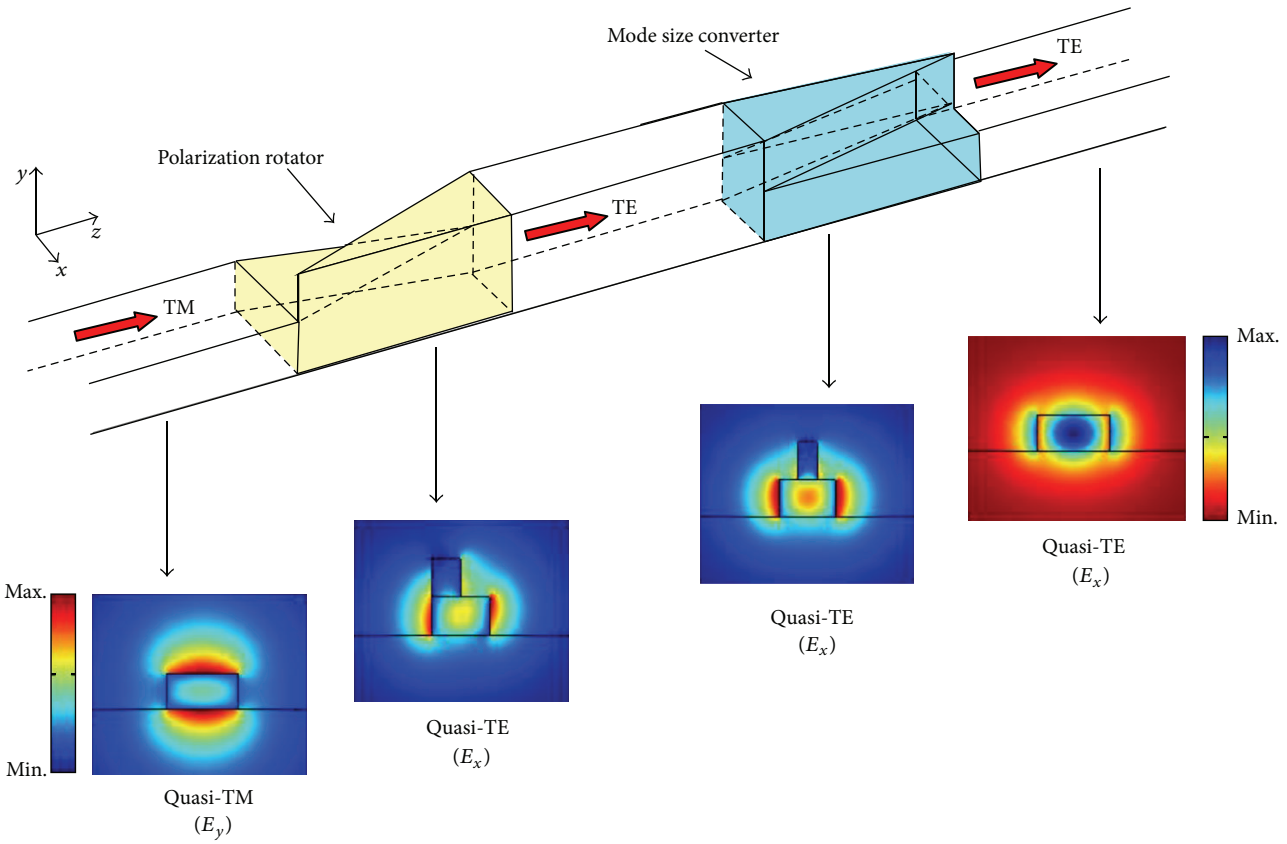


FIGURE 3: Cascade configuration composed of an SOI PR for the TM-TE polarization conversion in abnormal launching condition and a mode size converter in the output section.

and 26 dB in the wavelength range from 1525 nm to 1570 nm, revealing higher performance with respect to the previous PR device.

The main advantage of photonic PRs presented above is the possibility of achieving high polarization rotation efficiency in both normal and abnormal launching conditions. In particular, by considering the PR sketched in Figure 2, the normal launching condition occurs when the input mode is quasi-TM polarized, with this one being the fundamental mode supported by the waveguide. On the contrary, an abnormal condition occurs by launching in input a quasi-TE polarized optical mode. Obviously, this distinction depends on silicon waveguide dimensions and geometry; thus the definition is relevant to the waveguide structure at the PR input section.

In this context, Zhang et al. proposed an SOI mode size converter to be cascaded to the PR previously analyzed, to take advantage of operating at the abnormal launching condition [29]. The mode size converter proposed is characterized by analogous dimensions of the PR sketched in Figure 2 (i.e., input waveguide: 400 nm (height) × 200 nm (width), input waveguide: 400 nm (width) × 200 nm (height). However, the transition region is designed to have symmetric lateral taper and pseudovertical taper shape. In this way, the quasi-TE optical mode spatial distribution gradually converts as the waveguide gradually transforms from a vertical to a horizontal waveguide. For this purpose, 2D-FEM simulations at different device sections are plotted in Figure 3. The length of the transition region of the mode size converter can be at least 5 μm, revealing IL of around 2 dB. By considering longer transition region lengths (i.e., 30 μm) IL still remains stable around 2 dB, revealing quite large fabrication tolerances. Moreover, PERs as high as ~17 dB have been demonstrated experimentally. The overall device constituted by the cascade configuration is shown in Figure 3. In particular, it is characterized by a total length of 3 mm and suffers from high propagation loss ranging from 6.5 to 7.5 dB. For this purpose, authors suggest a silicon thermal oxidation process for reducing the roughness of silicon waveguide sidewalls, as a suitable approach for minimizing total propagation loss. In conclusion, the fabrication process requires two-step etching. Consequently, the effect of misalignment between the two layers used in the PR and mode size converter fabrication can decrease the overall rotation performance.

Zhang et al. investigated and fabricated a SOI PR based on a cascade configuration, similar to that discussed above [33]. The only difference concerns both PR and mode size converter that are based on horizontal slot waveguides instead of conventional silicon channel waveguides. The schematic of the integrated photonic device is shown in Figure 4.

The proposed technological approach, consisting in multilayer deposition and consecutive etching steps, is justified

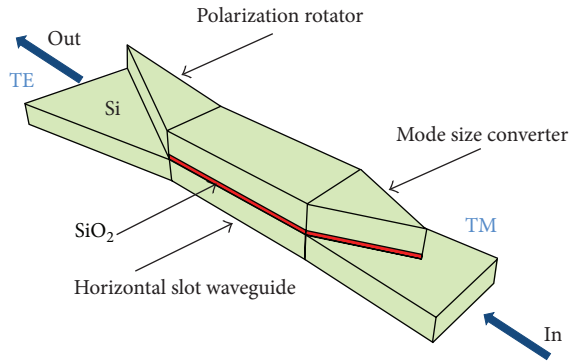


Figure 4: Cascade configuration composed of an SOI PR and a mode size converter, both based on a horizontal slot waveguide.

by high process robustness with respect to the fabrication based on two-step dry etching, as analyzed above. In fact, the possibility of avoiding the partial etching in the silicon channel waveguide allows reducing IL and improving the device performance. In particular, the slot waveguide serves as an etch stop layer for the bulk silicon layer in the last etching process. In this way, the effect of misalignment between multiple layers is minimized, resulting in relaxed fabrication tolerances and better process control. Finally, the fabricated SOI device exhibits propagation loss up to 5.2 and 2.38 dB/cm for quasi-TE and quasi-TM polarized mode, respectively. Moreover, IL for the mode converter as low as 0.5 dB and PERs higher than 14 dB have been achieved for different device lengths, with a flat response in the wavelength region extended from 1530 to 1600 nm in case of TE-TM and TM-TE polarization conversions. The major drawback of this type of devices is represented by the overall length. In fact, by summing the lengths of PR, mode size converter, and intermediate transition region, overall device lengths longer than 1-2 mm occur, resulting in high propagation losses and low device performance.

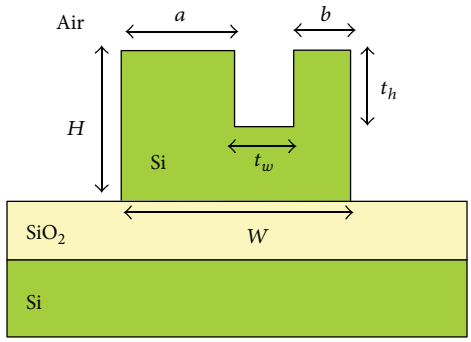
The last PMC based on adiabatic mode evolution analyzed in this section has been proposed by Caspers et al. [34]. In particular, authors theoretically investigated an ultracompact hybrid plasmonic mode evolution PR. The device is supposed to be fabricated on SOI technology platform and consists in standard silicon nanowires as input and output waveguides, characterized by a thickness of 220 nm and a width of 450 nm. In the intermediate section, the silicon waveguide is partially surrounded by a 200 nm thick gold layer separated from the silicon waveguide by a SiO_2 spacing layer. The Si-Au waveguide system has been designed to operate at the operative wavelength $\lambda = 1.55\,\mu$m. In addition, hybrid modes, considered as combinations of Surface Plasmon Polaritons (SPPs) excited at the metal-dielectric interface and conventional dielectric waveguide modes, propagate along the transition region where the polarization rotation occurs. In fact, the Au layer has been supposed to rotate around the silicon waveguide in order to force the polarization conversion. In spite of a complex device fabrication, simulation results reveal the possibility of achieving PER higher than 17 dB and IL of 1.6 dB with an overall device length as short as 4.7 μm. In this context, an ultracompact TE-pass polarizer fabricated on the SOI platform, has been recently demonstrated using a horizontal nanoplasmonic slot waveguide [35]. In particular, the device consists of a channel silicon waveguide surrounded by a 10 nm thick thermal oxide layer. In particular, the SiO_2 slot region is inserted between a copper (Cu) layer and the silicon core characterizing the channel waveguide. The operation principle consists in the fact that only the TE polarized optical mode is concentrated in the two vertical SiO_2 slots, while the TM mode is confined in the top horizontal slot. In this way, by designing a horizontal nanoplasmonic slot waveguide with a width lower than 210 nm, it is possible to achieve the cut-off for the TM mode since it is no more confined. Finally, the optimized device characterized by an overall length lower than 10 μm exhibits a PER higher than 16 dB in an operative bandwidth as wide as 80 nm, with insertion loss of 2.2 dB.

In the following, we analyze a category of SOI polarization rotators based on the principle of waveguide symmetry breaking. For this purpose, Leung et al. have proposed an exhaustive numerical analysis of an asymmetric SOI nanowire waveguide as compact PR [36]. In order to understand the operative principle of such devices, a schematic of the silicon waveguide cross-section is sketched in Figure 5. The principle of waveguide symmetry breaking consists in realizing a trench in the silicon waveguide core by using a single-trench photoresist mask and etching down to the desire depth. In particular, the SOI waveguide proposed here is characterized by an overall width $W = 800$ nm and height $H = 600$ nm. The single trench is 100 nm width (t_w) and 400 nm high (t_h), while the parameters indicated as "a" and "b" in Figure 5 have been set to 600 nm and 100 nm, respectively.

The operation of asymmetric waveguides is based on the excitation of the so-called hybrid modes. In fact, in such device architectures, it is not possible to distinguish between completely TE or TM polarized optical modes, because of the strong waveguide asymmetry. Consequently, the excitation of hybrid modes occurs, and dominant and nondominant optical fields of a selected guided mode can be distinguished. The waveguide cross-section has to be designed in order to maximize the excitation of highly hybrid modes. In particular, the silicon waveguide described previously has been simulated at the operative wavelength $\lambda = 1.55\,\mu$m, and the dominant (H_y-field) and nondominant (H_x-field) optical field spatial distributions are plotted in Figure 5.

The hybrid modes excited into the asymmetric waveguide results to be rotated 45° with respect to the x- and y-axis, resulting in 50% TE and 50% TM polarized orthogonal hybrid modes. As these two polarized modes travel along the single-trench section waveguide, their polarization states will be continuously rotated due to the phase difference between hybrid modes. In particular, at the distance L_π, the polarization state will be fully rotated. The parameter L_π is named half-beat length and it is defined as follows:

$$L_\pi = \frac{\pi}{\Delta\beta}, \tag{4}$$



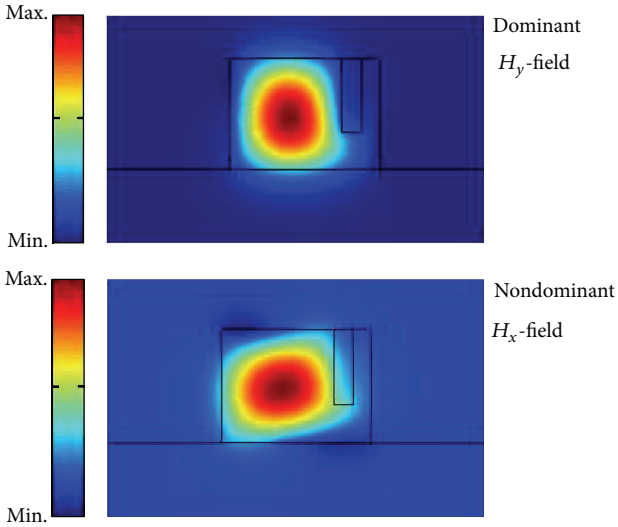


Figure 5: Cross-section of a SOI polarization rotator based on waveguide symmetry breaking. Spatial distributions of the dominant and nondominant hybrid modes.

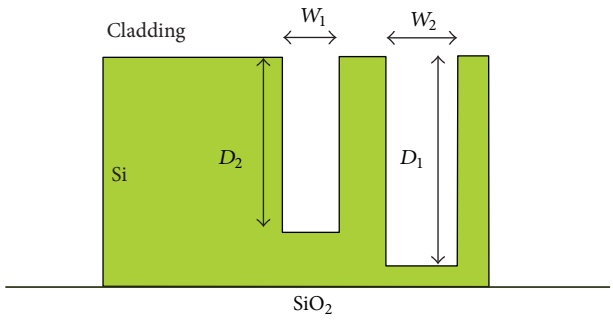


Figure 6: Schematic of the silicon waveguide characterized by a dual-trench asymmetry breaking.

where $\Delta\beta$ is the difference between the propagation constants of the dominant and nondominant optical fields. In this way, the original phase condition between the highly polarized modes will be reversed after propagating a distance $L = L_\pi$, and the polarization state will rotate 90° with respect to the initial one characterizing the optical mode launched into the waveguide. Authors have presented an extensive numerical analysis with the aim of optimizing waveguide geometry

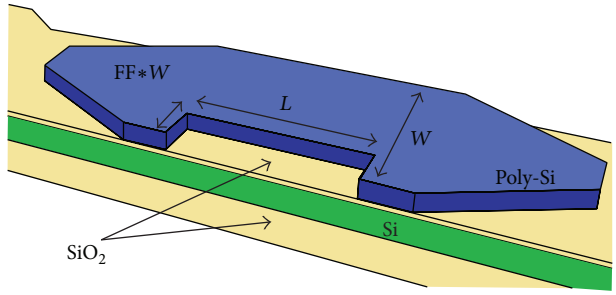


Figure 7: Schematic of a polarization rotator characterized by an asymmetric silicon waveguide.

and device length in order to obtain the best polarization conversion performance. In fact, with an overall device length of $L = 48\,\mu$m, polarization conversion of 99% can be obtained with IL as low as 0.21 dB and polarization crosstalk of about −22.38 dB. Finally, the main advantage of this PR in SOI technology, with respect to those analyzed previously, consists in the simple fabrication process, since only two etch steps are required for the device fabrication.

Velasco et al. have recently proposed an intriguing evolution of the single-trench asymmetric waveguide described above, in order to improve polarization rotation performance and minimize overall device length [30].

In particular, an asymmetric silicon waveguide characterized by two trenches in the silicon core, as sketched in Figure 6, has been designed and fabricated.

The principle of operation of such a device is based on the excitation of orthogonal hybrid modes as analyzed for the previous single-trench SOI PR. Authors have experimentally demonstrated intriguing polarization conversion performance. In fact, a PER = 16 dB, a polarization conversion efficiency up to 97.5% for TE-TM conversion, and a bandwidth as wide as 47 nm have been achieved with a PR device length as short as 10 μm. From a technological point of view, only one etch step is required for the fabrication. In fact, it is possible to take the advantage of the RIE lag effect, that is, the etch depth dependence on the trench width for small feature sizes. In conclusion, a 450 nm wide silicon waveguide has been designed to operate at the operative wavelength $\lambda = 1.5\,\mu$m (see Figure 6). Other geometrical parameters are trench widths equal to $W_1 = 60$ nm and $W_2 = 85$ nm and corresponding etch depths equal to $D_1 = 210$ nm and $D_2 = 230$ nm.

In conclusion, polarization rotators based on asymmetric SOI waveguides have been also proposed in [31, 37]. These devices are not characterized by single- or dual-trench cross-sections. In fact, the asymmetry is obtained by introducing a square geometry defect along the silicon waveguide core, as sketched in Figure 7. The cross-sectional view of the silicon waveguide is equal to that previously proposed in Figure 5, assuming the parameter "b" is set to be equal to 0 nm. In particular, the device is characterized by an amorphous silicon layer of 160 nm deposited onto a 5 nm silicon oxide layer thermally grown on a 200 mm SOI wafer.

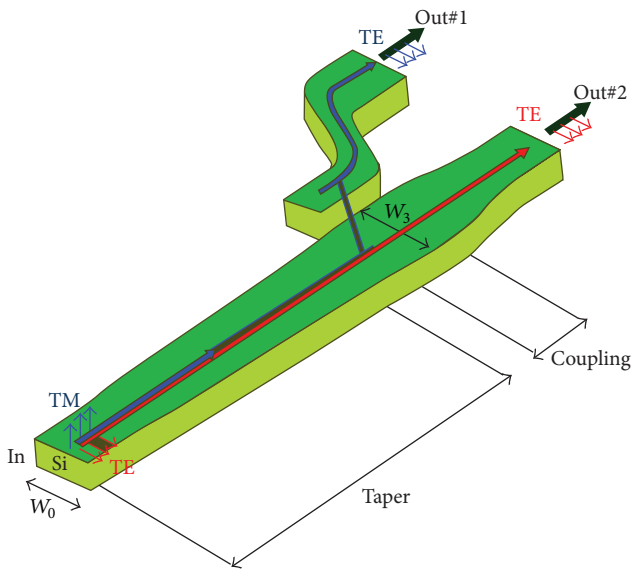


FIGURE 8: An ultracompact polarization splitter rotator based on SOI technology platform.

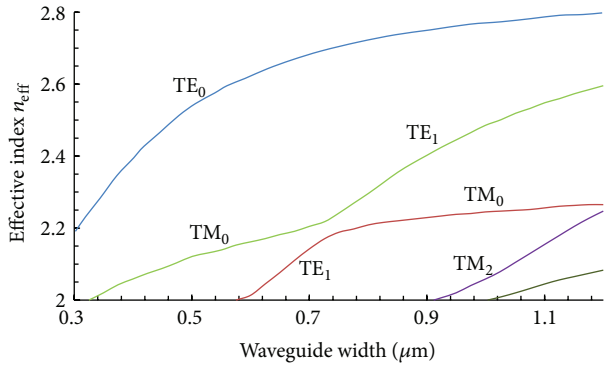


FIGURE 9: The calculated effective indices for the eigenmodes of SOI nanowire covered by Si_3N_4. Silicon waveguide height is set to 220 nm.

According to Figure 7, geometrical parameters selected for the device fabrication are $W = 405$ nm, $L = 7\,\mu$m, and fill factor (FF) equal to 75%. Globally, device performance evidences PCE as high as 89% with a crosstalk of −9,55 dB over a bandwidth as large as 80 nm. The device structure is very robust and fabrication tolerances experimentally analyzed result to be relaxed with respect to those characterizing other PR architectures analyzed in this section. The main drawback of such devices is the 4 etch step process flow used for the fabrication.

Finally, the similar device configuration proposed by Aamer et al. [31] consists in a conventional SOI wire waveguide covered by a 1 μm thick silica cladding. A polarization conversion efficiency above 82.2% over a wavelength range of 30 nm and IL from −1 dB to 2.5 dB have been experimentally demonstrated in a 25 μm long device. In this case, the overall number of etch steps required for the device fabrication is limited to two.

In the following, the class of PMCs based on the principle of mode interference is briefly reviewed. In particular, the first architecture is that proposed by Dai and Bowers [32]. The device consists in an ultracompact polarization splitter rotator realized by combining an adiabatic taper (acting as PR) and an asymmetrical directional coupler (acting as a PS), as sketched in Figure 8.

The principle of operation of such a device can be explained by firstly analyzing the adiabatic taper in the input section. This taper is based on a conventional silicon photonic wire waveguide characterized by a height of 220 nm. The waveguide width gradually changes from the minimum value of $W_0 = 0.54\,\mu$m to the maximum one of $W_3 = 0.9\,\mu$m, corresponding to the width of the asymmetrical directional coupling, as shown in Figure 8. Generally, when the silicon wire waveguide is vertically symmetric (i.e., SiO_2 as bottom and top material cladding), excited modes are purely polarized. This statement is not true when the vertical symmetry is not verified (e.g., air or Si_3N_4 as silicon waveguide cladding material). In fact, when upper-cladding refractive indices are different (i.e., $n_{SiO_2} = 1.445$ and $n_{Si_3N_4} = 2$, at $\lambda = 1.55\,\mu$m), it cannot be possible to distinguish the polarization of some eigenmodes because of the mode hybridization. For this purpose, we show in Figure 9 the effective indices calculated for the silicon waveguide with Si_3N_4 cladding, as a function of different values of waveguide width. From the plot, it is possible to observe that, for a waveguide width around 0.76 μm, the mode conversion between TM fundamental mode and the first higher-order TE mode occurs. In this way, the input and output waveguide cross-sections should be characterized by waveguide width lower and higher than 0.76 μm, respectively, in order to prevent any mode conversion.

In this context, it holds $W_0 = 0.54\,\mu$m and $W_3 = 0.9\,\mu$m respect the condition mentioned above. Moreover, W_0 is small enough to match the single mode condition. On the contrary, the adiabatic taper is characterized by waveguide width ranging from W_0 to W_3, in order to support the mode conversion according to Figure 9.

The output section of the PMC shown in Figure 8 is represented by an asymmetric directional coupler whose arms are identified by a 0.9 μm wide silicon waveguide and a narrow waveguide, with a width of about 0.4 μm. In this way, the first higher-order TE mode, excited along the adiabatic taper, is coupled to the TE fundamental mode of the adjacent narrow waveguide. In summary, the input TM fundamental mode of the waveguide can be converted into the fundamental TE mode at the cross-port of the asymmetrical directional coupler. When the TE fundamental mode is launched in the input waveguide, it does not change its polarization state along the adiabatic taper, according to the curves plotted in Figure 9. Moreover, the TE fundamental mode propagating in the wide waveguide cannot be coupled to the adjacent narrow one in the region of the asymmetrical directional coupler, because of the phase mismatching. Finally, simulation results reveal polarization conversion efficiency as high as 100% with a

device length shorter than 100 μm. In conclusion, only a one-mask process is needed for the device fabrication, combining polarization splitting and rotating into a compact integrated photonic device.

Similar PMC devices have been theoretically investigated and experimentally demonstrated as well, revealing insertion loss as low as −0.6 dB and extinction ratio of 12 dB [21]. Moreover, Ding et al. [38] have designed an ultracompact polarization splitter rotator for the TE-TM polarization conversion. Authors have experimentally demonstrated very large fabrication tolerances by considering the overall SOI device covered by air. In fact, the tolerance of the narrow waveguide width is relaxed to more than 14 nm, conversion efficiency remains stable for tapering lengths varying from 100 μm to 140 μm, and the device results to be less sensitive to the length of the directional coupler.

In the field of investigation of PMCs based on the physical principle of mode interference, it is noteworthy to mention a very efficient TE-TM polarization converter based on two coupled silicon nanowires in SOI technology platform, demonstrated by Liu et al. [39]. In particular the operation principle of such a device is based on the cross-polarization coupling in high-index SOI waveguides. In fact, any cross-coupling between the fundamental TE and TM polarized modes cannot occur across waveguides since they are orthogonal under the assumption that the waveguide profile is symmetrical either horizontally or vertically. However, in the proposed device, the vertical symmetry is broken since the coupled waveguides are covered by air while the buffer layer is silica. In addition, the horizontal symmetry is also broken by placing two parallel asymmetric waveguides characterized by different widths. Consequently, it is possible to design waveguide widths in order to fulfill phase matching conditions between TE and TM modes, resulting in efficient coupling from the TE mode in one waveguide to the TM mode in the other one. In fact, PCE higher than 92% with overall insertion loss lower than −1.6 dB can be achieved in a very compact device characterized by a total length of 44 μm and operating in an operative bandwidth as large as 40 nm. Finally, the proposed device can be easily fabricated by a single etch step and UV lithography.

An ultrashort PS based on the same operation principle described above has been demonstrated by Dai and Bowers by using a bent directional coupler constituted by two SOI waveguides with different core widths [40]. The advantage of using such an architecture consists in achieving a device length shorter than 10 μm and a bandwidth as broad as 200 nm with extinction ratio higher than 10 dB. In addition, fabrication tolerances for the variation of the waveguide width are quite relaxed, being more than ±60 nm.

A further improvement of this type of PS based on coupled waveguides has been proposed by Dai et al. [41]. In particular, a PS based on an asymmetrical S-bent directional coupler has been proposed by considering a strip nanowire coupled to a nanoslot waveguide. The operation principle of such a device is based on the birefringence of the slot waveguide [42]. In fact, the effective index of the TE polarized optical mode propagating in a slot waveguide is generally low (similar to the refractive index of the cladding material), since the optical field is mainly confined in the cover medium (i.e., the low refractive index material, such as air). On the contrary, the effective index of the TM polarized mode is higher than the previous one since the optical spatial distribution is mainly concentrated into the high refractive index material (e.g., silicon). In this way, effective indices of optical modes propagating in silicon slot and strip nanowire waveguides are different especially for the TE polarized one. Consequently, this large phase mismatch prevents power transfer of the TE mode from the channel waveguide input port to the slot waveguide output port. However, the TM mode can evanescently couple into the slot waveguide if both waveguide dimensions are properly designed in order to achieve the best phase matching, resulting in a very efficient polarization splitting. In this context, simulation results evidence the possibility of achieving extinction ratio higher than 10 dB in an operative bandwidth wider than 160 nm, by designing a 6.9 μm long PS.

Analogously, Lin et al. have designed, fabricated, and characterized an ultracompact polarization splitter constituted by a channel silicon waveguide coupled to a silicon slot waveguide [43]. For this purpose, polarization extinction ratios of 21 dB and 17 dB have been achieved for TE and TM polarization, respectively, with a coupling length of 13.6 μm.

Moreover, a compact PS based on two coupled horizontal silicon slot waveguides and characterized by a coupling length of 15 μm has been experimentally demonstrated revealing an extinction ratio higher than 16 dB at the operative wavelength $\lambda = 1.55\,\mu$m [44]. The main drawback of such an architecture consists in a quite complex fabrication. In particular, the proposed PS has been fabricated on an 8-inch Si wafer with a 2 μm thick buried oxide (BOX) layer. The device fabrication consists in an initial multilayer deposition (i.e., 250 nm amorphous Si as the bottom Si layer, followed by 60 nm SiO_2 as the slot, and finally 250 nm amorphous Si as the top Si layer) using plasma enhanced chemical vapor deposition (PECVD). Consequently, waveguide structures can be patterned by using optical lithography and then etched by RIE down to the BOX surface.

Finally, a further evolution of these PS based on slot waveguides has been recently investigated by Wang et al., proposing a novel PS architecture based on a vertical multiple-slotted waveguide coupled to a silicon nanowire [45]. Numerical results exhibit an operative bandwidth as large as 22 nm (ranging from 1.540 μm to 1.562 μm), with the crosstalk lower than −20 dB and overall device length of 20.5 μm.

Actually, the further research frontier of PS architectures based on asymmetric and symmetric bent couplers is represented by the integration of plasmonic waveguides [46, 47]. In particular, in addition to conventional adiabatic mode-evolution and mode-coupling principles already analyzed in this section, the use of metal layers in PS devices and their large birefringence allows the excitation of SPPs by specific polarization light. The advantages of using such devices consist in the possibility of fabricating PS with very short lengths (e.g., 1.1 μm) since SPPs can be confined in very small confinement areas, resulting in an enhanced light-matter interaction and ultrahigh performance as well (e.g., PER > 20 dB

and IL < 1 dB). On the contrary, the fabrication of such devices is not simple and conventional metal depositions are needed for their operation. In addition, fabrication tolerances are not as large as those of other conventional devices analyzed previously, resulting in severe technological process control.

Nowadays, several research efforts are performed in order to design and fabricate ultracompact and ultrahigh performance PMCs (i.e., PR as well as PR), based, for example, on nonlinear tapered slot waveguide [48], multimode interference (MMI) coupler [49] and bend asymmetric slab waveguides [50], towards better performance, more compact devices, and simpler fabrication with more relaxed tolerances.

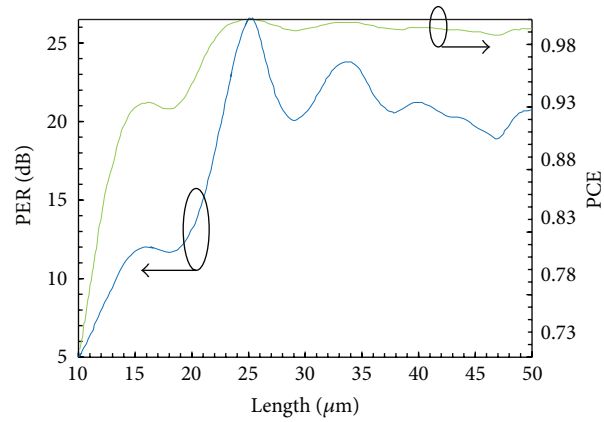


Figure 10: PER and PCE as a function of the overall device length.

3. Design and Optimization of High Performance PMCs

In this section, rigorous theoretical simulations and optimizations of four PMC devices in SOI technology are presented. Moreover, simulation tools based on the eigenmode expansion (EME) and finite difference (FD) methods (i.e., FIMMPROP by Photon Design© [51] and COMSOL Multiphysics© [27]) have been also used to investigate the fabrication tolerances, since they dramatically influence performance and application of polarization splitters and rotators [52]. For this purpose, our investigation procedure consists in considering a multidimensional space defined by all the geometrical parameters characterizing the device to be designed (i.e., length, waveguide width, coupler gap, and filling factor, to name a few). Consequently, the optimization process consists in calculating the unique geometrical configuration that allows achieving the best performance in terms of PER, PCE, and IL as well. In particular, an iterative procedure is implemented, in which several steps are needed, by changing one dimension of the geometrical space, one at one time, and simultaneously fixing all other ones during the same iteration. Finally, small variations around the nominal values of some critical geometrical parameters constituting the optimized multidimensional space will be taken into account for simulating the influence of fabrication tolerance on the overall device performance.

The first architecture considered in our analysis (i.e., Device #1) is a PR based on the principle of the mode evolution, thus operating in the same way as the device shown in Figure 2, previously. In particular, the silicon photonic waveguide is assumed to be realized on a SiO_2 buffer layer and covered by a 2 μm thick top silica cladding. Moreover, input and output waveguides are 500 nm (height) × 250 nm (width) and 500 nm (width) × 250 nm (height), respectively.

In this context, the first optimization process we have investigated consists in calculating the TM-TE polarization conversion performance as a function of increasing values of the overall device length, ranging from 10 μm to 50 μm. Numerical results are plotted in Figure 10 and evidence a precise length value (i.e., $L = 25\,\mu$m) that allows the device to exhibit maximum PER and PCE as high as 26 dB and 99.7%, respectively. However, it is possible to observe in Figure 10 how polarization conversion performance dramatically decreases for device lengths lower than 25 μm. On the contrary, for higher length values, device performance remains quite high, being PCE > 90% and PER > 18 dB. In summary, $L_{\min} = 25\,\mu$m can be considered the minimum suitable length for the design of such a device.

From a technological point of view, the PR considered in this investigation can be fabricated by using a two-step etching process employing standard CMOS facilities, including 193 nm deep UV lithography, inductively coupled plasma reactive ion etching (ICP-RIE), or e-beam lithography for very high resolution patterns. However, the device fabrication may not be so simple because misalignment effects between the employed etching layers can occur, resulting in worst device performance. Consequently, the analysis of fabrication tolerances on PR performance should be taken into account for the design of such devices. For this purpose, we have calculated PER and PCE as a function of different values of the etching depth variation assumed to occur during both the first (i.e., the definition of 250 μm thick layers) and the second etch step (i.e., the definition of 500 μm thick layers), with these ones being very critical design and fabrication processes. Simulation results, which are plotted in Figures 11(a) and 11(b), evidence fabrication tolerances of ±10 nm for the first 250 μm deep etching process. In fact, in the 20 nm wide range centered at the nominal value of 250 μm, PER and PCE are higher than 25 dB and 99.5%, respectively. In Figure 11(b), numerical results related to the second etch step confirm that device performance dramatically decreases only in case of underetching, since the optical mode cannot be efficiently forced to rotate along the transition region. On the contrary, in case of positive etch depth variations around the nominal value of 500 μm, PER and PCE still remain stable and quite high. In summary, even for the second etch step, fabrication tolerances as large as ±10 nm can be taken into account.

In conclusion, device performance has been investigated also as a function of different operative wavelengths in order to define the PR operative bandwidth B_W. Simulation results plotted in Figure 12 evidence a PR bandwidth as wide as

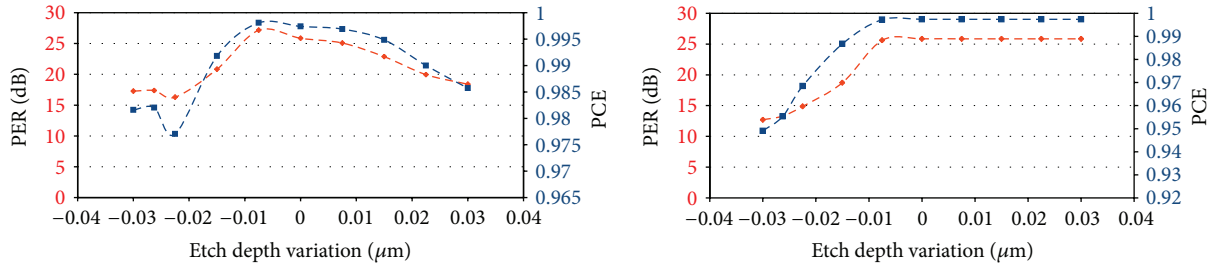


FIGURE 11: PER and PCE of Device #1 calculated as a function of the etch depth variation during the first (a) and second (b) etching processes.

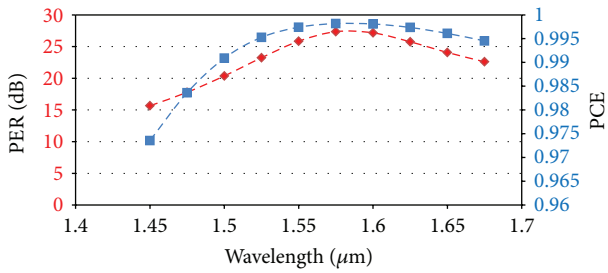


FIGURE 12: PR performance as a function of different operative wavelengths.

100 nm centered at the operative telecom wavelength $\lambda = 1.55\,\mu$m. In fact, in this spectral region PER and PCE are higher than 20 dB and 99%, respectively, revealing ultrahigh performance.

In this context, the bandwidth B_W represents a very crucial parameter in the operation of such devices. In particular, from a physical point of view, by changing the operative wavelength of the optical signal propagating into the device, the optical mode distributions in silicon waveguide cross-sections, as shown in Figures 2, 3, and 5, for example, can change because of the dispersion effects in silicon and its oxide, affecting both the device operation and performance. Consequently, once the device architectures have been optimized, then exploring their operation by sweeping a spectral range around the operative wavelength is needed, in order to ensure high performance in case of single channel operation (i.e., narrow B_W) or multichannel operation as well (i.e., wide B_W).

The second PMC architecture (i.e., Device #2) considered in the theoretical investigation is a PR based on the principle of symmetry breaking for the hybrid mode excitation. The silicon device is characterized by a dual-trench architecture, as that shown in Figure 6. In particular, the top and cross-sectional views of the PMC are shown in Figure 13.

The device proposed here is assumed to be fabricated on standard SOI technology platform (i.e., SOI wafer with 260 nm thick silicon layer on top of 2 μm thick BOX) by using only one etch step process and employing the RIE lag effect for realizing the dual-trench architecture. Moreover, an e-beam lithography can be employed in this case, since the space between the inner and outer trenches can be as narrow as ~30 nm, thus imposing a high resolution pattern definition.

The device has been designed in order to operate at the wavelength $\lambda = 1.55\,\mu$m and to efficiently convert the input TM polarized optical mode to TE polarized one at the output section. In Figure 13, all the geometrical parameters characterizing the overall silicon waveguide cross-section have been indicated with the only exceptions of the parameter L (i.e., the length of the device without including the input and output tapered regions) and S (i.e., the space between the inner and outer trenches), since they have been selected in order to optimize the device performance. In fact, S represents a critical design parameter because it can affect the widths of both the inner and outer trenches. For this purpose, a tolerance within the range of ±6 nm centered around the design optimized value (i.e., 34 nm) is taken into account for real device fabrication.

In the optimization procedure, we have analyzed PR performance as a function of several geometrical parameters such as S and L as well as the inner and outer trench widths, initially set to 60 nm and 90 nm, respectively. All the numerical and simulation results are plotted in Figures 14(a)–14(d). In particular, as demonstrated in Figure 14(b), best device performance can be achieved by considering the width $S = 33$ nm. In fact, PER of about 34 dB and ideal PCE as high as 99.9% can be achieved. Fabrication tolerances of ±2 nm are required to ensure PER higher than 20 dB and PCE higher than 95%. PR performance has been also simulated as a function of different values of the conversion length L as plotted in Figure 14(a). In particular, simulations have been carried out by considering all geometrical parameters fixed with the width set to $S = 33$ nm, since the conversion length L is demonstrated to be not influenced by the variations of S. Moreover, numerical results confirm the conversion length $L = 5\,\mu$m as the optimal one, since it is possible to obtain the highest PCE and PER. Finally, very relaxed fabrication tolerances as large as ±500 nm can be considered for the device length in order to assure high polarization conversion performance (i.e., PER > 25 dB and PCE > 85%).

The optimization procedure of the PR silicon device based on dual-trench asymmetry waveguide consists in estimating the influence of trench widths and heights on device performance too. In the previous section we have already discussed the RIE lag effect usually employed for fabricating different trenches onto the same waveguide, by using a single

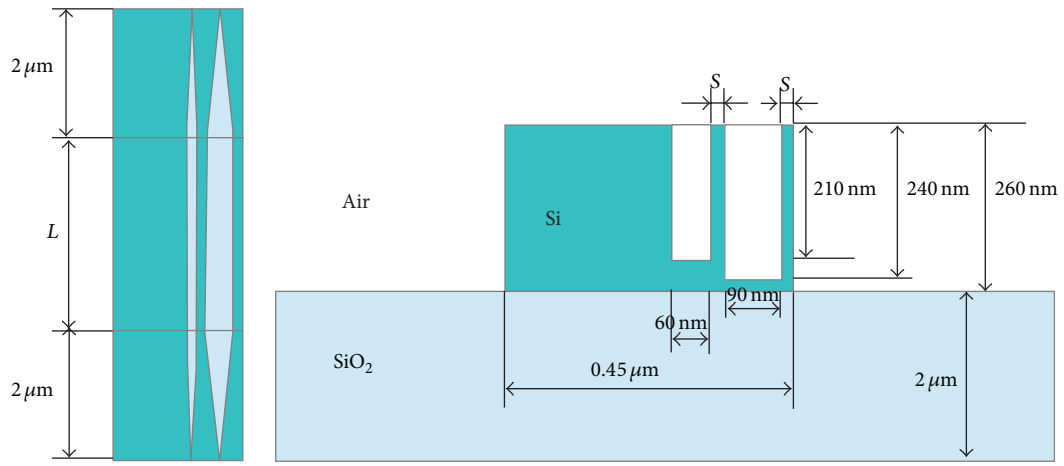


FIGURE 13: Top (left) and cross-sectional (right) views of the double-trench SOI PR.

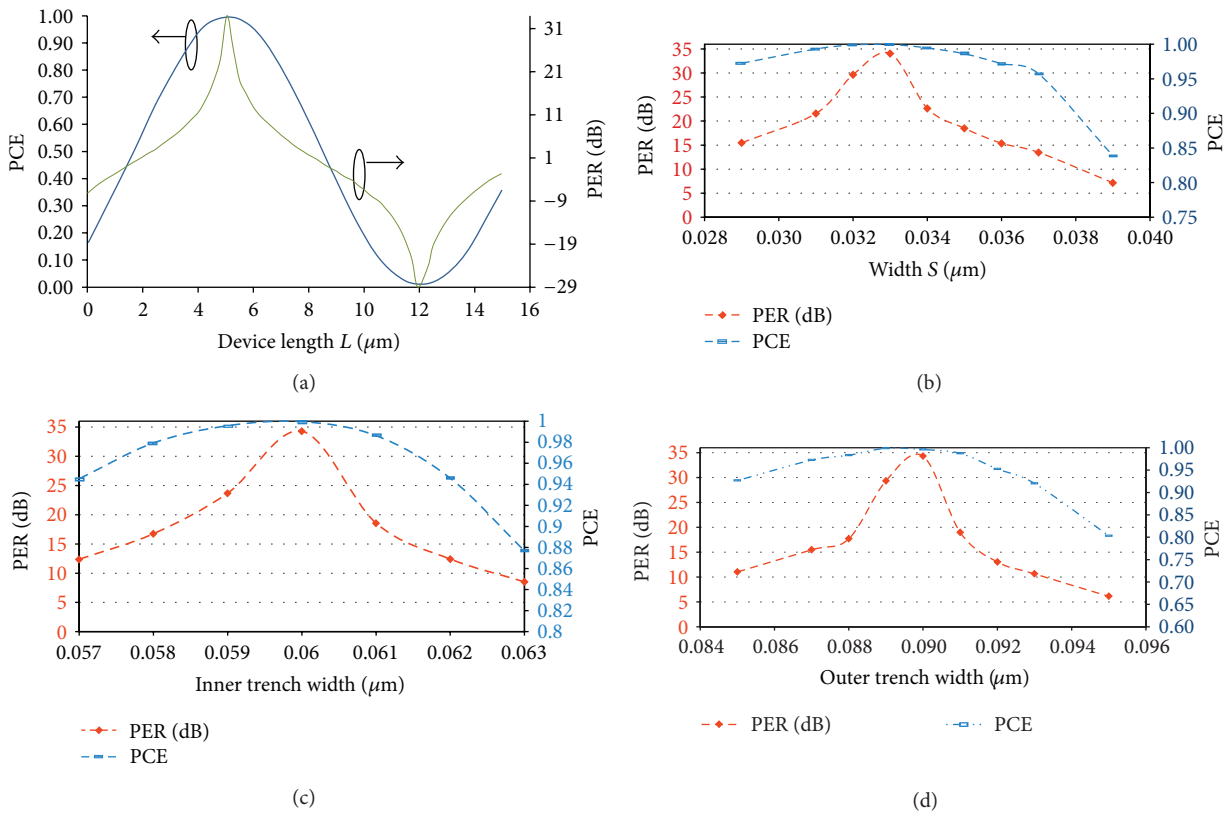


FIGURE 14: Polarization conversion performance as a function of the conversion length L (a), parameter S (b), different inner (c) and outer trench widths (d).

etch step. In this context, we keep the ratio between width and height of a single-trench constant considering, at the same time, that this approximation is valid only for very small variations of both trench width and height. Numerical results plotted in Figures 14(c) and 14(d) suggest optimal inner and outer trench widths equal to 60 nm and 90 nm, respectively. The etch depth is 210 nm in case of the inner trench and 240 nm for the outer one, with an overall waveguide height of 260 nm.

Ideal device performance can be theoretically achieved with the geometrical dimensions mentioned above and the optimum conversion length of about 5 μm, as previously demonstrated. Furthermore, fabrication tolerances for both the inner and outer trench widths are not so large. In fact, a

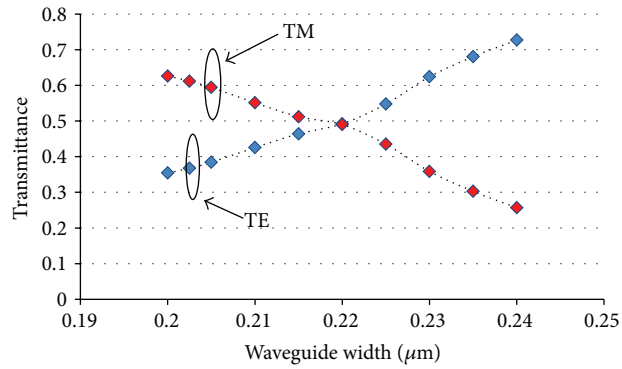


FIGURE 15: Transmittance of orthogonal hybrid modes supported by the silicon waveguide as a function of different widths W.

variation of ±3 nm can produce a dramatic decrease of PER and PCE, being lower than 20 dB and 85%, respectively.

In conclusion, the bandwidth of the PR device proposed centered at $\lambda = 1.55\ \mu$m is as wide as 50 nm, ensuring in this spectral range PER > 17 dB and PCE > 98%.

The third device configuration (i.e., Device #3) considered in this theoretical investigation is that proposed in [31] and previously sketched in Figure 7. In particular, a silicon channel waveguide surrounded by silica is assumed to be fabricated on a SOI wafer with 220 nm thick silicon layer on top of 2 μm thick BOX layer and modified into an asymmetric waveguide by etching a square profile of the right external side. In this case, 193 nm deep UV as well as e-beam lithography and ICP-RIE etching can be employed for device fabrication. In addition, chemical vapor deposition (CVD) can be employed for silicon photonic waveguide passivation as well. The waveguide is 220 nm high, while the width of the waveguide can be set in order to maximize the excitation of orthogonal hybrid modes. Finally, the etched square profile is 70 nm deep, while its width is proportional to the waveguide width W by a filling factor indicated as FF.

In this case, the first step of the design procedure consists in calculating the optimum waveguide width for the hybrid mode excitation, with this one being a fundamental requirement for the device operation. For this purpose, the transmittance of the fundamental orthogonal modes supported by the waveguide is plotted in Figure 15 as a function of different values of W. As a result of our calculations, the best waveguide width is $W = 220$ nm, resulting in a trench width of 113 nm with a filling factor FF = 25%. Once defined the geometrical dimensions of the waveguide cross-section, it is possible to analyze the influence of fabrication tolerances and device length on polarization conversion performance.

For this purpose, a TM-TE polarization conversion has been considered and all the results are plotted in Figures 16(a)–16(c).

In particular, the optimum length value results to be $L = 29\ \mu$m where an ideal PCE = 100% and a PER > 50 dB can be achieved (Figure 16(a)). Moreover, fabrication tolerances for the parameter L are as large as ~±3 μm around the optimum value. In fact, device performance still remains acceptable in this range, with PER being always higher than 16 dB.

Device performance has been also analyzed as a function of the filling factor and the etch depth characterizing the single trench on the right side of the silicon waveguide. Numerical results are plotted in Figures 16(b) and 16(c). In particular, the optimum FF is confirmed to be 25%, where PCE and PER are the highest (i.e., PER > 45 dB and PCE > 99%). In addition, variations of ±3% around the optimum FF value do not affect the device performance at all.

The etch depth of the single trench of 70 nm is the best design solution for maximizing both PER and PCE. In addition, a variation of the etch depth within the range ±5 nm centered at 70 nm can be tolerated without significantly degrading the polarization conversion performance. Finally, the last graph shown in Figure 17 evidences an overall PR bandwidth as large as 20 nm, centered at operative wavelength $\lambda = 1.55\ \mu$m. In this spectral range, PER and PCE are higher than 17.5 dB and 98.3%, respectively.

The last PMC configuration (i.e., Device #4) analyzed in this section is a compact polarization splitter rotator as that investigated in [32], assumed to be fabricated in SOI technology platform by e-beam lithography and ICP-RIE etching processes. In Figure 18, a schematic of the proposed device is sketched with all geometrical dimensions labeled. The PS has been designed to execute a TM-TE polarization conversion at the operative wavelength $\lambda = 1.55\ \mu$m.

In particular, the overall architecture is assumed to be covered by a Si_3N_4 cladding in order to assure an asymmetric vertical refractive index distribution for increasing the mode hybridization. For this purpose, it is possible to refer to Figure 9, where calculated effective indices for the eigenmodes supported by the 220 nm high silicon waveguide are plotted as a function of different waveguide widths. In particular, the adiabatic taper has been divided by three sections in order to optimize the design procedure and ensure the TM_0-TE_1 polarization conversion along the tapered region, according to the modal evolution plotted in Figure 9.

The design of the asymmetric directional coupler represents a crucial step for the correct device operation. In fact, the TE higher-order mode propagating along the tapered waveguide cannot be coupled to the adjacent narrow waveguide because of the phase mismatching. Consequently, only the TE_0 fundamental mode will be coupled to the narrow waveguide and guided to the device output. On the contrary, the TE_1 higher-order mode will propagate straight on the input waveguide, without influencing the optical mode split on the adjacent arm. In this context, device performance has been investigated as a function of different coupler gaps and lengths L, by initially considering all other geometrical dimensions to be fixed as indicated in Figure 18.

In Figures 19(a) and 19(b), device performance (i.e., PER and PCE) has been sketched as a function of different coupler gaps. In particular, the best value for the gap is $g = 0.15\ \mu$m, where PER of 12.5 dB and PCE as high as 95% can be theoretically achieved. It is noteworthy to mention that, for gap values lower than 0.15 μm and higher than 0.25 μm, PS performance dramatically decreases since the coupling coefficient becomes too small. Consequently, the power coupled to the S-bend, in this weak coupling condition, is too low, resulting in compromised polarization conversion efficiency. Moreover,

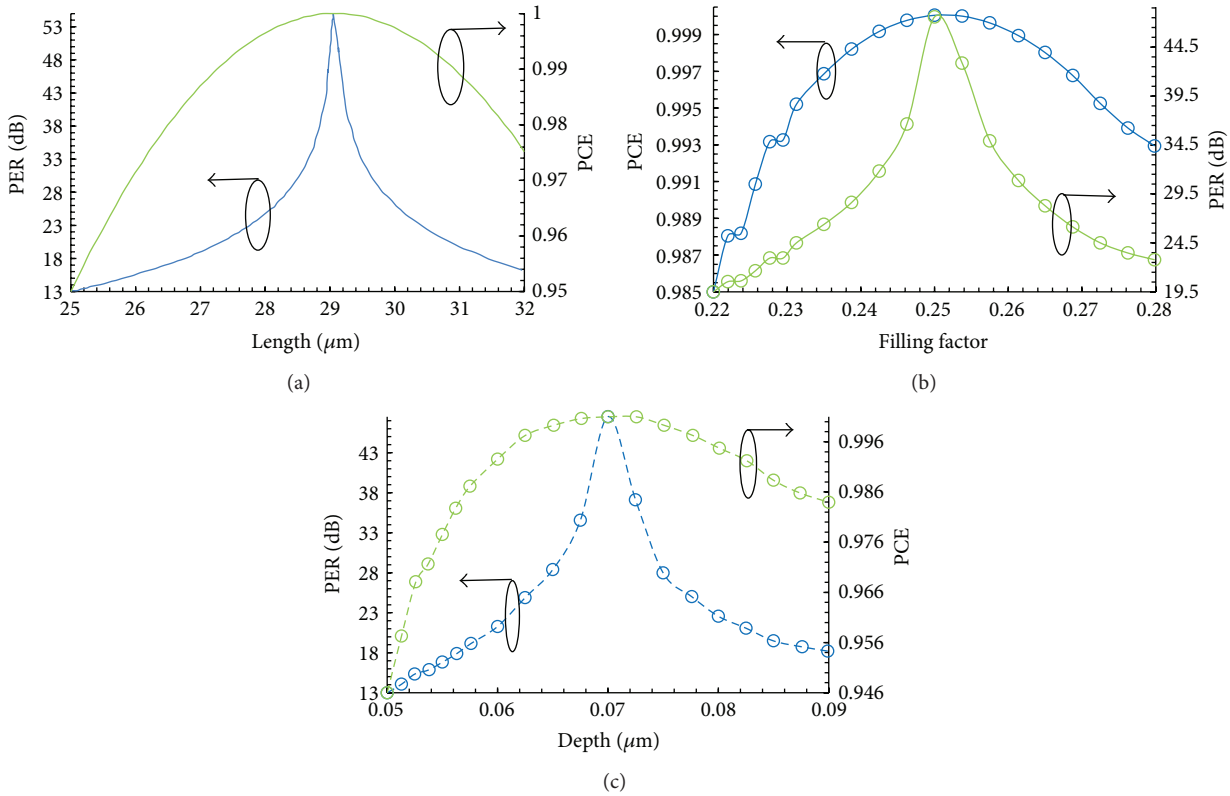


FIGURE 16: PER and PCE as a function of different PR lengths (a), filling factors FF (b), and trench depth values (c).

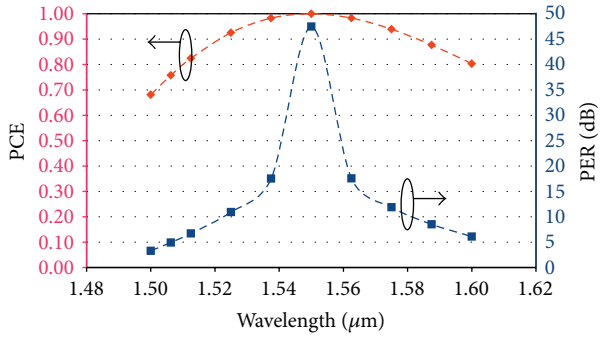


FIGURE 17: PR polarization conversion performance as a function of different operative wavelengths.

PER decreases by 3 dB with a gap variation of 25 nm, revealing more severe fabrication tolerances with respect to other PS configurations, as analyzed previously.

Once the optimum coupler gap $g = 0.15\,\mu$m has been defined, device performance is calculated as a function of different coupling lengths, with the aim of maximizing the polarization splitting. In Figure 19(b), is it possible to observe that the variations of PER and PCE results to be periodic as a function of the parameter L, as it was expected by the coupled mode theory (CMT). In fact, the plot has been zoomed only in the first period being the initial condition $L = 0\,\mu$m. Furthermore, the performance peak is achieved approximately at the half of the fundamental coupling length (i.e., $L \approx 17\,\mu$m), resulting $L \approx 7\,\mu$m, at which PER $\approx$ 17 dB and PCE $\approx$ 98% can be theoretically achieved. This trend is justified because all the power can be coupled from the adiabatic taper to the S-bend at $L \approx 7\,\mu$m, maximizing the TM-TE polarization conversion. Finally, fabrication tolerances result to be as large as $\pm 2\,\mu$m.

In summary, the optimized asymmetric directional coupler is characterized by a coupler gap $g = 0.15\,\mu$m and a coupling length $L = 7\,\mu$m. Consequently, the last geometrical dimension to be investigated is the waveguide shift represented by the parameter S, as shown in Figure 18. For this purpose, numerical results evidence the optimum value for $S = 1.2\,\mu$m, achieving PER as high as 39 dB and PCE higher than 99.98%, with fabrication tolerances of ± 400 nm, ranging from $0.7\,\mu$m to $1.5\,\mu$m. In conclusion, the overall device bandwidth has been calculated as wide as ~170 nm centered at the operative wavelength $\lambda = 1.54\,\mu$m, allowing a multichannel device operation. Finally, extinction ratio between optical powers monitored at the output ports of the device has been estimated as about 15 dB at $\lambda = 1.55\,\mu$m, revealing very high performance.

This section is concluded by presenting a useful comparative analysis of PMC devices designed and optimized in this work. For this purpose, all photonic devices indicated with the name "Device #n" (with $n = 1, 2, 3, 4$) are listed, and their performance (i.e., PER and PCE), operative bandwidths, overall lengths and number of etch processes required for their fabrication are appropriately summarized.

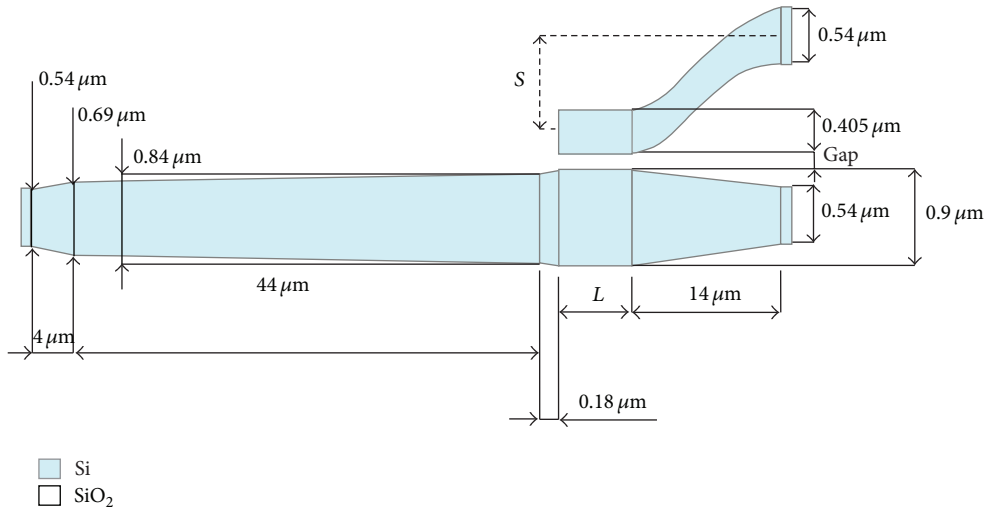


Figure 18: Schematic of the compact polarization splitter rotator in SOI technology platform.

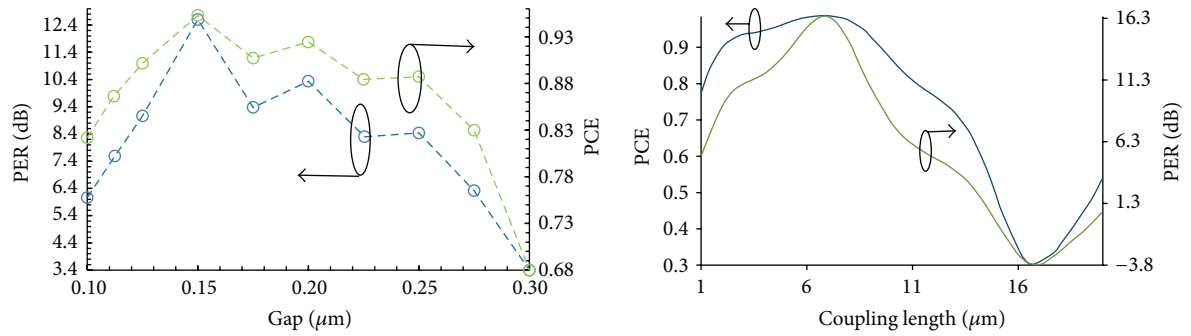


Figure 19: PMC performance as a function of different coupler gaps (a) and coupling lengths (b).

Table 1: Comparison among different PMC architectures.

Device	Performance	B_W	L	Etch step
[26]	PER = 15 dB	300 nm	40 μm	2
Device #1	PER = 26 dB PCE = 99.7%	100 nm	25 μm	
[30]	PER = 16 dB PCE = 97.5%	47 nm	10 μm	1
Device #2	PER > 17 dB PCE > 98%	50 nm	5 μm	
[31]	PCE = 82.2%	30 nm	25 μm	2
Device #3	PER > 17.5 dB PCE = 98.3%	20 nm	29 μm	
[32]	PCE ≃100%	70 nm	100 μm	1
Device #4	PER = 39 dB PCE ≃100%	170 nm	75 μm	

Furthermore, in Table 1 each device is also compared to experimental and theoretical results of corresponding device architectures as presented and discussed in Section 2.

Numerical results demonstrate that, although all optimized devices can exhibit very intriguing performance, Device #4 is that characterized by best PER and PCE, as it is confirmed also by experimental measurements in [32]. In particular, its PER = 39 dB is approximately the double of PER parameters exhibited by all the other optimized devices as listed. In addition, this type of architecture can be fabricated with a single etch step process and e-beam lithography but it reveals, at the same time, severe tolerance of eventual coupler gap fabrication errors, as it has been demonstrated previously. However, the whole analysis suggests a trade-off among device performance, dimensions, and their bandwidth and fabrication complexity. In fact, it is possible to observe in Table 1 that the length of Device #4 is the longest one (i.e., $L = 75$ μm) among all the other configurations.

Globally, optimized PMC devices can achieve better polarization conversion performance with respect to analogous not-optimized devices proposed in the literature. In particular, small overall device lengths (i.e., L) and very wide operative bandwidths (i.e., B_W) confirm these PMC devices as an intriguing solution for the integration of ultracompact polarization rotator and splitter in photonic

integrated circuits characterized by small footprints of a few μm $\times$ μm. In addition, all devices considered in this paper are CMOS compatible with standard microelectronics technology facilities, resulting very suitable for low cost fabrication and large scale integration.

4. Conclusion

In this paper we have firstly reviewed some of the fundamental PMC architectures designed and fabricated in SOI technology platform. In particular, several device configurations proposed as polarization splitter, rotator, and mode size converter, as well as combinations of them into the same integrated photonic circuit, have been taken into account. Then, polarization conversion performance, design criteria, fabrication tolerances as well as insertion losses, overall bandwidths, and fabrication processes have been considered for a comparative analysis.

In Section 2, we have presented the design and optimization of four PMC architectures described in Section 1. In particular, the influence of fabrication tolerances on device performance has been theoretically investigated. For this purpose, rigorous simulations based on the eigenmode expansion (EME) and finite difference (FD) methods have been executed. Simulation results reveal very high polarization conversion performance (e.g., PER > 20 dB and PCE > 90%), operative bandwidths as wide as 100 nm, and ultracompact PMC characterized by lengths as small as 5 μm. Furthermore, a useful comparison between our results and experimental and theoretical ones published in the literature confirms the validity of the design and optimization procedures implemented in this work, as well as the possibility of improving PMC performance by further device optimizations. Actually, main PMC specifications are essentially oriented to simple fabrication processes, relaxed fabrication tolerances, and wide operative bandwidth for a suitable device operation in standard C and L communication bands. Recently, PMC applications have been also extended to the unexplored and intriguing midinfrared wavelength region, confirming the fundamental role that such devices play in integrated photonics [53, 54].

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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