Selecting and designing the front-end amplifier for high-gain photomultiplier detectors with optimal timing performance

Selecting and Designing the Front-end Amplifier for High-gain Photomultiplier Detectors with Optimal Timing Performance

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Abstract

High-gain photomultiplier detectors are employed in an increasing number of applications in different fields to evaluate with great accuracy the occurrence time of light flashes composed by few or even single photons. Examples of these application fields are medical imaging, astroparticle and high energy physics, laser spectroscopy and LIDAR. To fulfill a good single photon timing accuracy, in the range of few hundreds of picoseconds, not only detectors with intrinsic excellent timing resolution (photomultiplier tubes, microchannel plated detectors, silicon photo multipliers, etc.) must be used, but the very first front-end amplifier (FEA) stage, used to read-out the detector, must also be carefully chosen and designed.

We compare here three commonly used solutions for the FEA, from the point of view of the best achievable timing resolution: the charge sensitive amplifier (CSA), the voltage amplifier (VA) and the current buffer (CB). The results show that the CSA solution is limited in terms of frequency response by the usually large equivalent capacitance of the detector and that, surprisingly, the presence of the parasitic inductance *L*, due to interconnection detector-FEA, has a noise shaping effect which favourably affects the timing accuracy of the CB over the VA configuration. To support this study, simulations of simple implementations of the compared FEA solutions have been performed, under the same conditions.

Moreover, with reference to a given detector and to a particular value of *L*, we show how the best timing accuracy of the CB is obtained by selecting an appropriate combination of input resistance and bandwidth of the FEA.

Keywords: Timing accuracy; high-gain photomultiplier detectors; front-end electronics..

1. Timing accuracy: different front-end solutions

In single-photon applications of high-gain photomultipliers [1-4], when a Leading Edge Discriminator (LED) is used as time pick-off, it is well known that the total jitter in time measurements can be evaluated by means of the ratio between the rms electronic noise, σ_{no}, and the slope of the FEA output pulse at a given threshold V_{TH} [5]:

$$\sigma_t = \frac{\sigma_{no}}{\left.\frac{dV_{OUT}}{dt}\right|_{V_{OUT}=V_{TH}}} \quad (1)$$

Fig. 1 shows, schematically, the three common solutions adopted in the literature as FEA for high-gain photomultiplier detectors. For the CSA (Fig. 1a), if *GBW* and e_n^2 are, respectively, the gain-bandwidth product and the equivalent input power spectral density of the voltage amplifier, we can easily derive the following expressions of maximum slope (in t=0) of the output signal and of the rms output noise, σ_{no}:

$$\left.\frac{dV_{OUT}}{dt}\right|_{MAX} \cong \frac{Q_{eff}}{C_{eq}+C_F} GBW;\ \sigma_{no} \cong \frac{e_n}{2}\sqrt{\left(1+\frac{C_{eq}}{C_F}\right) GBW}, \quad (2)$$

By substituting the expressions (2) in (1), the minimum jitter achievable by the CSA solution is:

$$\sigma_t \cong \frac{e_n(C_{eq}+C_F)}{2Q_{eff}}\sqrt{\left(1+\frac{C_{eq}}{C_F}\right)\frac{1}{GBW}} \quad (3)$$

From (3) we can observe that the timing accuracy of the CSA FEA is strongly limited by the usually large value of the detector equivalent capacitance C_{eq}, especially in the SiPM case; thus the following analysis can be restricted to the other two remaining approaches, VA and CB. Fig. 2 shows two basic CMOS implementations of the two FEA. The circuits share the same input transistor, biased at the same operating point (I_D = 1 mA) and the same bandwidth. In Fig. 2, *L* represents the parasitic inductance due to the interconnections between detector and FEA [6-7].

Without considering *L*, we can obtain an approximate expression for the jitter, which applies to both configurations:

$$\sigma_t \cong \frac{i_{n1}C_{eq}}{2g_{m1}Q_{eff}}\sqrt{\frac{1}{BW}} = \frac{e_{n1}C_{eq}}{2Q_{eff}}\sqrt{\frac{1}{BW}}, \quad (5)$$

where e_{n1} is the gate-referred equivalent noise of the input transistor M_1, and *BW* is the amplifier bandwidth ($\approx 1/R_L C_L$).

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Figure 1 (spans over the 2 columns)

Figure 2 (spans over the 2 columns)

For the CB, the main noise contributions come from the power spectral density of the noise drain currents of the input MOSFET M_1, and of the transistor which provides I_{BIAS}. The former is effective only at high frequencies, because of the zero introduced by the equivalent capacitance of the detector C_{eq}, whereas the latter is shunted to ground at high frequencies by the same capacitance. Since the noise contribution of the bias transistor can be minimized by using a low-g_m current mirror, we can neglect it and assume, conservatively, that the total output current noise of M_1 is effective on the full frequency spectrum. This worst-case assumption allows to easily derive the time jitter given in (5).

2. Effect of the parasitic inductance on the timing accuracy: simulation results and conclusions

Table I reports the simulations results of the VA and CB configurations, taking into account L. The slope of the leading edge of the output pulse worsens for increasing values of L in both circuits, due to a new time constant, L/R_{in} which arises at the FEA input, thus limiting the slope of the input current [7]. Concerning noise, the effects of the parasitic inductance are different for the two configurations; while the output noise of the VA is only slightly affected by L, the output noise of the CB decreases for increasing value of L, due to a noise shaping effect. In fact, at high frequencies, L decouples C_{eq} from the source of M_1, reducing the contribution of i_{n1} to the output noise.

As a conclusion, from Table I it is evident that the CB approach exhibits better timing performance as compared to the VA, when the effect of the inductance due to the detector/FEA interconnection is considered.

Figure 3

Finally, referring to a CB FEA, Fig. 3 shows the simulation results of a study on the behavior of the timing accuracy as a function of the FE design parameters R_{in} and BW for the Hamamatsu H8500 PMT. It appears that the design criteria of increasing BW and reducing R_{in} as much as possible, as suggested from (5), does not represent the best possible design choice when considering the parasitic inductance L; on the contrary, for a given detector and interconnection inductance L, an optimal pair (R_{in}, BW) can be found, which correspond to a minimum of the overall timing accuracy σ_t.

Table I. VA vs CB: main performance parameters for different values of L.

L [nH]	σ_{n0}(VA) [μV]	σ_{n0}(CB) [μV]	dV_{OUT}/dt (VA) [V/s]	dV_{OUT}/dt (CB) [V/s]	σ_t(VA) [ps]	σ_t(CB) [ps]
10	4.52	3.41	8.68×10^4	9.01×10^4	52.0	37.8
20	4.82	3.15	6.21×10^4	6.38×10^4	77.5	49.4
40	5.10	2.87	4.18×10^4	4.26×10^4	122.1	67.3
60	5.24	2.71	3.22×10^4	3.26×10^4	162.8	83.2
80	5.32	2.61	2.63×10^4	2.66×10^4	201.9	97.9
100	5.37	2.54	2.25×10^4	2.27×10^4	239.0	111.8

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FIGURE CAPTIONS

Figure 1. High-gain photodetector (simplified model) coupled to a (a) Charge Sensitive Amplifier (CSA); (b) Voltage Amplifier (VA); (c) Current Buffer (CB).

Figure 2. Simple CMOS implementations of the (a) VA and (b) CB, used in the simulations to evaluate the time jitter.

Figure 3. CB: timing accuracy vs bandwidth for different values of R_{in} and L = 10 nH (Hamamatsu H8500 PMT).

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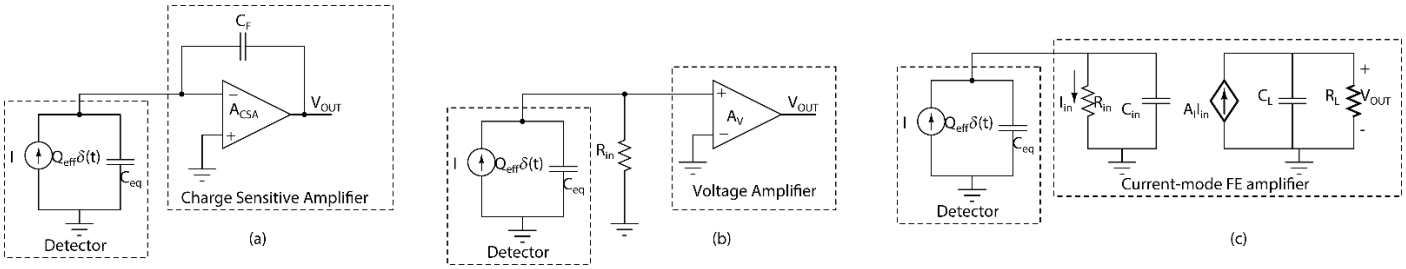
1 **Figure 1 (2 columns)**



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1 **Fugure 2 (2 columns)**

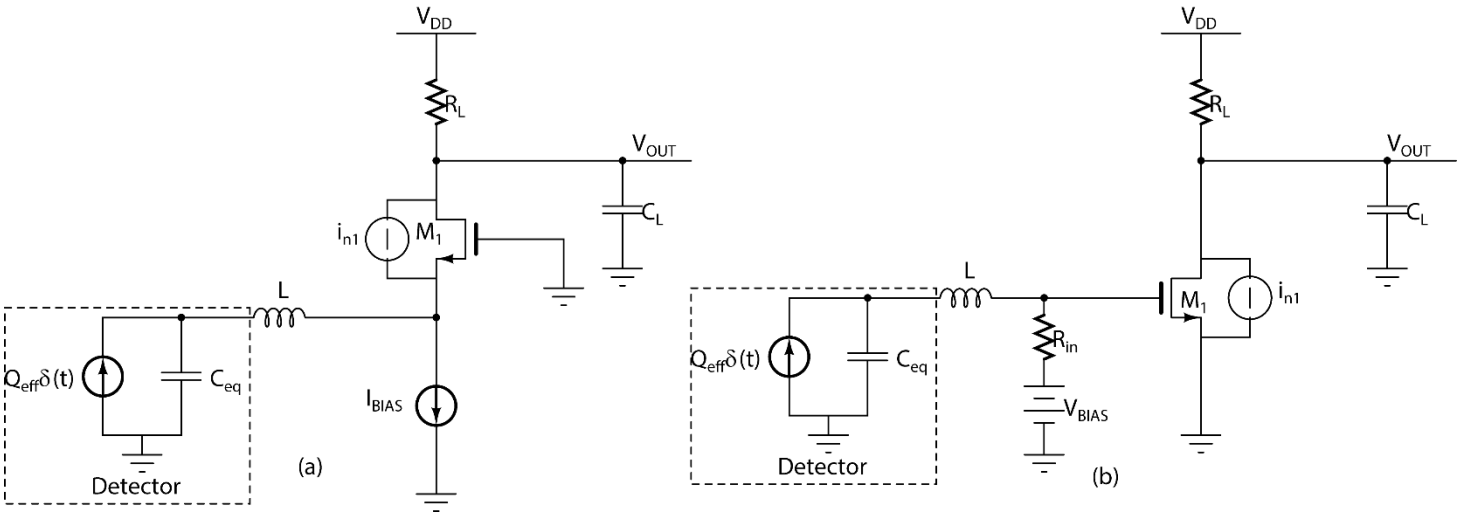

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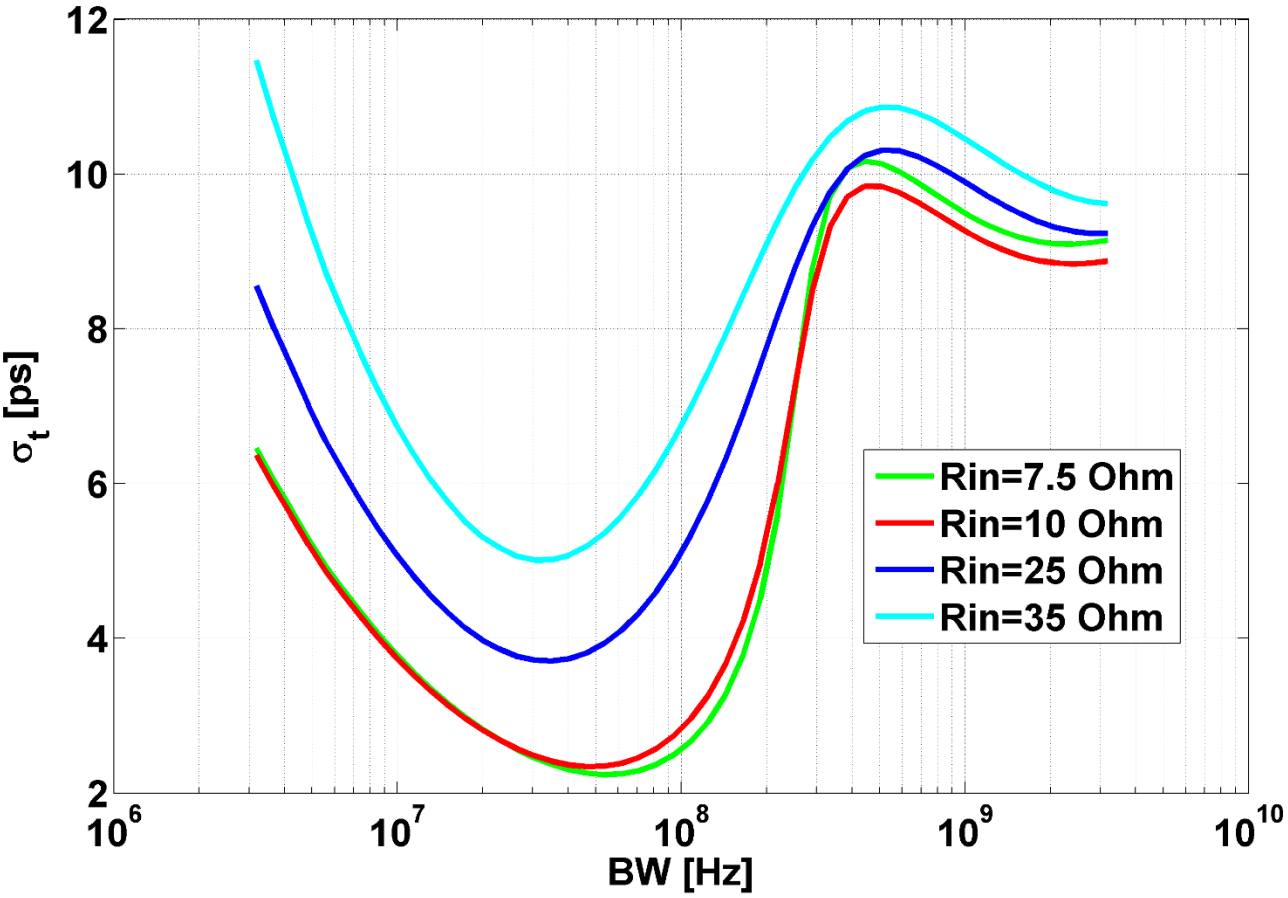
Figure 3 (colour; 1 column)



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