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Experimental test and characterization of BASIC64, a new mixed-signal front-end ASIC for SiPM detectors

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Abstract

BASIC64 is a new multichannel front-end ASIC for Silicon photomultiplier detectors used in PET systems. The preamplifier input resistance is ~50 Ω. It is low enough not to further affect the slope of incoming current pulses, already plagued by the presence of stray series inductance. For each channel, the signals generated by the detector follow two parallel processing paths, respectively for timing and energy measurements. The timing accuracy and linearity results from experimental test and characterization are presented and confirm that BASIC64 is suitable for PET applications.

Keywords: SiPM, front-end electronics, readout ASIC

1. Introduction

In the framework of the INSIDE (INnovative Solutions for Dosimetry in hadrontherapy) project, a multichannel front-end ASIC, BASIC64, has been developed in a standard 0.35 μm CMOS technology for interfacing both p-on-n and n-on-p SiPM detectors used in the PET systems [1]. The self-triggering ASIC hosts 64 current-mode front-end channels; each of them can generate a trigger signal whenever a valid event is recognized and provides the associated energy information out of a built-in 8 bit ADC [2]. The channel architecture is based on a very simple open-loop current buffer, i.e. a CG configuration. This solution removes any possible stability issue, which may stem from encompassing in a negative feedback loop large values of the detector terminal capacitance [3]. Both a current-mode approach and a leading-edge discrimination methodology help to preserve the favourable timing performance of the SiPM and meet the demanding application requirements in terms of input dynamic range. The input impedance is scaled down to 50 Ω and no further effort is made at reducing it to extremely lower values, considering that the parasitic inductance itself is dominant in the mechanism of slowing down the SiPM current pulses [4]. For each channel, the incoming signals run into two different paths, for timing and energy measurements. The energy "slow" path includes an integrator and a peak detector; an analog voltage proportional to the peak of the integrated charge is produced before being digitalized by the on-chip ADC. The digital logic macro integrated in the ASIC manages autonomously the readout procedure, which can be carried out in sparse or serial mode. Furthermore it controls the ADC and the data transfer via a LVDS link and resets the ASIC after the completion of the readout procedure.

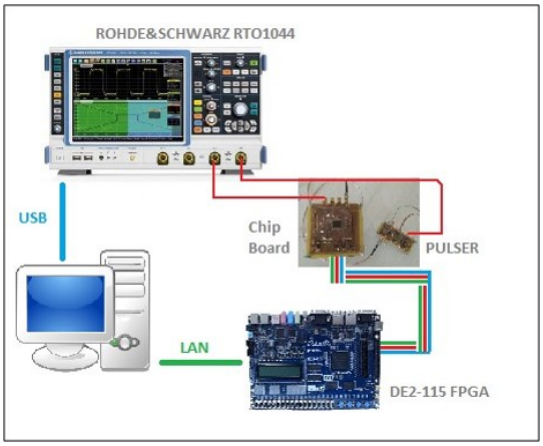

Figure 1: Measurement setup.

2. Measurement setup

The experimental test setup (Figure 1) includes a prototype test board for the front-end ASIC, a fast step voltage generator board (PULSER) for charge injection and a digital oscilloscope for signals visualization and data acquisition. Configuration, power and control signals are dispatched using a FPGA board and two DC power supplies (not shown in the figure) that complete the setup. The PULSER reproduces the effect of charge injection from the SiPM with 1000 pF series capacitor, enabling to adjust injected charge in the range from 16 pC to 576 pC with the resolution of a 16 bit DAC.

3. Test and characterization

Firstly, a DC electrical functionality test has been performed to measure quiescent currents and voltages throughout the chip

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Table 1: The relevant parameters of the BASIC64. The measurement have been carried out at room temperature and the results refer to the channel 15 of the ASIC.

Parameters	Measured Value
Timig jitter (1 σ)	40 ps
Gain	3 mV/pC
Maximum NLE	1.5 %
Noise (FWHM)	580 fC

reference test points at different configuration settings and the outcomes exhibited good matching with simulations. For two over 64 channels both timing and charge gain have been measured and evaluated. As far as timing measurements are concerned, an FPGA time controlled input signal of given amplitude has been sent to the ASIC for a defined number of cycles and the trigger out signal recorded. The distribution of the time difference between the time stamps of the two signals has been plotted and fitted. The results, in Figure 2, have shown the possibility to reach a remarkable average timing accuracy of 40 ps RMS down to very low input charge levels under careful setting of the timing discriminator threshold, even though strictly dependent on ambient temperature. Regarding charge measurements, the input signal has been swept and injected charge varied from 32 pC to 576 pC in 3.2 pC steps (~20 photoelectron in SiPM). Analog output voltage has been sampled and data fitting with a linear regression technique has allowed gain and integral non-linearity error to be retrieved. Digitized data carrying input charge information are also available out of the onboard 8 bit ADC and fit in with the corresponding analog output voltage measures. The transfer function of the output voltage vs. input charge (Figure 3) exhibits a maximum absolute non-linearity error of 1.5 % up to 576 pC (~3600 photoelectrons), in good agreement with simulations. The parameters of the main blocks composing the analog signal processing chain (common gate input buffer, discriminators, shaper, peak detector, programmable gain amplifier and ADC), have been evaluated so far, exhibiting 3 mV/pC gain. Lastly, noise measurements have been carried out by keeping the timing discriminator threshold constant while sweeping the input signal. For each threshold value, 1000 signal samples have been collected and the number of valid events (chip triggering) has been counted. The derivative of the resulting S-Curve, in Figure 4, has allowed us to plot the noise distribution, whose dispersion around the mean divided by gain expressed in mV/fC has led us to calculate an input referred noise of 580 fC. The measured relevant parameters of the presented ASIC are summarized in Table 1.

4. Conclusion

The ASIC performance is compliant with PET application requirements. Even though timing jitter related to weak input signals is not at the cutting edge of timing performance, it still marks a good result considering that the ASIC has not been designed to meet the specification of Single Photon Timing Resolution (SPTR) applications. Gain linearity is acceptable over the whole input range required for resolving the 511 keV peak.

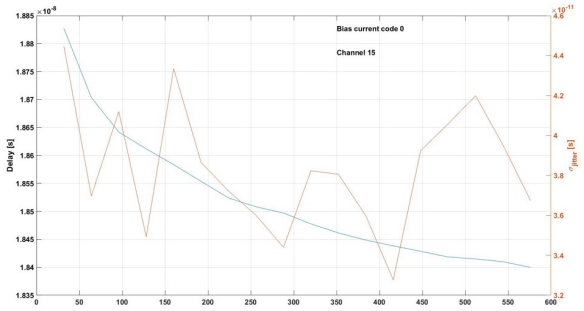

Figure 2: Gain and Non-Linearity Error vs. Input Charge.

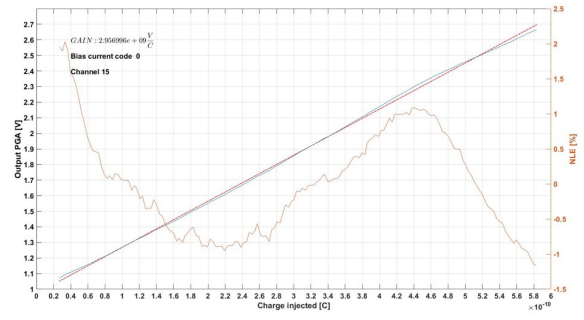

Figure 3: Jitter and Delay vs. Input Charge.

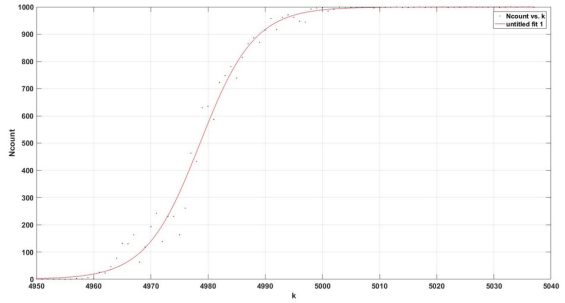

Figure 4: S-Shape Curve vs. Input Charge @ fixed threshold.

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