A Novel Non-Volatile Optoelectronic Memory: The Photon-Triggered FGMOS

Martino De Carlo

***Abstract*— A novel non-volatile opto-electronic memory at a wavelength of 850 nm is presented. The memorization principle exploits the same concept of floating-gate metal-oxide-semiconductor (FGMOS) memories, i.e. the trapping of charges in a floating gate. The basic memory cell of the Photon-Triggered FGMOS (PTFGMOS) is realized through the physical combination of a FGMOS and a silicon waveguided structure; each photon absorbed by silicon generates an electron-hole pair. The high voltage applied to the control gate of the FGMOS attracts the generated free electrons towards the floating gate, trapping them (tunnel effect) even after the control gate voltage is lowered. Hence, the electrons trapped in the floating gate affect the threshold voltage of the MOSFET, thus making the memory easily readable electrically. The device provides a useful way to directly store the information from the optical to the electrical domain. The footprint of the designed PTFGMOS single cell is 5 μm × 2 μm.**

***Index Terms*— Optoelectronic memory, floating gate, non-volatile, storage, MOSFET, FGMOS.**

I. Introduction

THE recent achievements in the area of integrated optical memories and the increasing adoption of optical interconnects in the Datacom and Computercom Industries explain the growing interest for information storage directly from the optical domain, with fast access and storage time, high density and increased bandwidth [1]. Specifically, non-volatile memories enable the possibility of retaining stored information even after the power is switched off. The interest for non-volatile optical memories has been further pushed forward thanks to the growing attention to neural networks and their photonic implementation with neuromorphic circuits [2], [3], [4]. Some solutions to realize non-volatile optical memories make use of phase-change materials (PCMs) [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15]. There are also some different recent approaches proposed to achieve non-volatile memorization of light, using organic materials [16], [17], [18], for high-density and low-power storage. Different solutions make use of magnetic materials [19], [20]. In [21], an electrically programmable optical non-volatile memory has been experimentally proved, showing the idea a floating gate metal-oxide-semiconductor (FGMOS) to modulate the optical phase in a silicon ring resonator.

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In this work, a novel device is shown and simulated to realize an optoelectronic memory working at a wavelength of 850 nm, the Photon-Triggered Floating Gate Metal-Oxide-Semiconductor (PTFGMOS). The device can store the optical information as electrons trapped in a floating gate. The memory is fully CMOS compatible; it makes use of silicon and silicon nitride.

II. The Photon-Triggered FGMOS

The idea presented in this work is based on the concept of the FGMOS. FGMOSs (widely used in flash memories) are peculiar MOSFETs able to permanently trap charges in a floating gate, thus modifying the threshold voltage of the MOSFET, realizing a non-volatile memory [22]. In this work, the concept of an FGMOS is combined with an optical waveguide; when high voltage is applied to the gate and no current flows between source and drain (they are both configured as high impedance), an optical absorbing medium (silicon) efficiently converts the guided photons at 850 nm to an electron-hole pair. Thanks to the high voltage applied to the control gate, the photogenerated electrons are attracted next to the boundary with the top insulator (SiO_2) and some of them get trapped (stored information) into the floating gate (due to the tunnel effect). The presence of a negative charge in the floating gate influences the threshold voltage of the MOSFET, making the memorized information easily readable, as in FGMOSs. Since the presence of photons triggers the generation of electrons that get trapped in the floating gate, the device will be called Photon-Triggered FGMOS (PTFGMOS). The device is supposed to be placed inside a complex photonic integrated circuit (including low-loss waveguides), so silicon nitride (Si_3N_4) has been chosen to realize the waveguides that are end-fire coupled to the PTFGMOS to minimize the footprint of the memory cell. The device, shown in Fig. 1a, comprises the PTFGMOS cell (cross section in Fig. 1c) and a low-loss silicon nitride waveguide (cross section in Fig. 1b). Finite Elements Method (FEM) and optical propagation simulations have been performed to simulate the device.

III. Device Modeling

A. Semiconductor Analysis

For the semiconductor (silicon) 2D simulations, the Drift-Diffusion model [23], described by differential equations (1.a-1.e), has been solved through a general-purpose FEM solver:

$$\boldsymbol{J}_n = eD_n \nabla n + n\mu_n \nabla E_c - enD_n \nabla \ln(N_c) \quad (1.a)$$

$$\boldsymbol{J}_p = -eD_p \nabla p + p\mu_p \nabla E_v + epD_p \nabla \ln(N_v) \quad (1.b)$$

$$\frac{\partial n}{\partial t} = G_n - R_n + \frac{1}{e} \nabla \cdot \boldsymbol{J}_n \quad (1.c)$$

$$\frac{\partial p}{\partial t} = G_p - R_p - \frac{1}{e} \nabla \cdot \boldsymbol{J}_p \quad (1.d)$$

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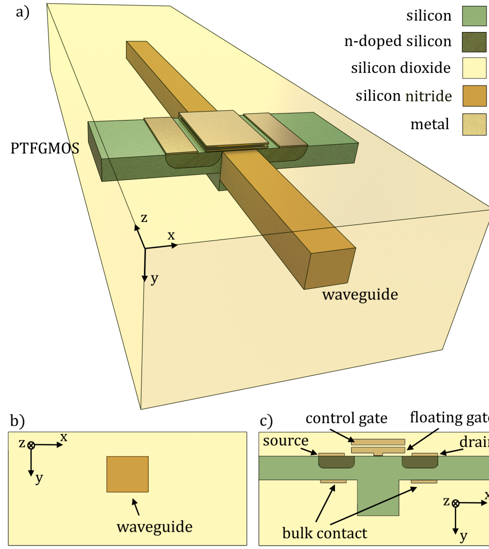

Fig. 1. (a) Rendering of a PTFGMOS cell fed by a Si_3N_4 waveguide. (b) Si_3N_4 waveguide cross section. (c) PTFGMOS cross section.

$$\nabla \cdot \boldsymbol{E} = \frac{\rho}{\varepsilon} \tag{1.e}$$

where $n(p)$ is the carrier concentration of electrons (holes), e is the charge of the electron, $\boldsymbol{J_n}$ ($\boldsymbol{J_p}$) the current densities of electrons (holes), D_n (D_p) is the constant diffusion coefficient for electrons (holes) and μ_n (μ_p) is the mobility (assumed to be constant) of electrons (holes); G_n (R_n) and G_p (R_p) are the rates of electrons and holes generation (recombination), respectively; E_c (E_v) is the conduction (valence) band energy; $\boldsymbol{E}$ is the electric field; N_c and N_v represent the effective density of states in conduction and valence band, respectively. Finally, ε is the permittivity and ρ is the charge density.

The main effect realizing the trapping of carriers in the floating gate is the tunnel effect. The tunnel barrier boundary condition between the semiconductor region and the oxide has been modeled using the following equations [22]:

$$\boldsymbol{n} \cdot \boldsymbol{J}_n = +A^n_{FN} E^2_{ins} e^{-\frac{B^n_{FN}}{E_{ins}}} \tag{2}$$

$$\boldsymbol{n} \cdot \boldsymbol{J}_p = 0 \tag{3}$$

with $\boldsymbol{n}$ the normal vector to the surface at the boundary; A^n_{FN} and B^n_{FN} are the Fowler-Nordheim coefficients [22]; E_{ins} is the normal component of the electric field in the insulating layer. The optical transitions in the semiconductor are modelled with generation rates for electrons ($G_{n,abs}$) and holes ($G_{p,abs}$) [24]:

$$G_{n,abs} = G_{p,abs} = \alpha \Phi = \frac{\alpha S}{\hbar \omega} \tag{4}$$

where α is the power absorption coefficient, Φ is the photon flux, ω is the angular frequency of incident photons, S is the Poynting vector (along the optical propagation direction, z), and $\hbar$ is the reduced Plank constant.

Drain, source and bulk contacts have been simulated to be ohmic. The gate has been simulated to have a contact work function of 4 eV.

IV. Numerical Simulations

For the 2D semiconductor simulations, an out-of-plane thickness of $W = 5\ \mu$m has been used. The doping concentration in the source and drain regions is 10^{18} cm^{-3}. The doping concentration in the lightly p-doped substrate is 10^{16} cm^{-3}. The source and drain regions are 600 nm × 200 nm and are separated by 800 nm. The thickness (d_t) of the SiO_2 layer separating the floating gate and the silicon in the tunneling region is 8 nm, that is assumed to be a conservative value for repeatability and endurance [25]. The width (w_t) of the tunneling interface, that should be designed as a trade-off between endurance and speed (a larger tunneling region usually involves higher capacitance and slower writing time), has been chosen to be 280 nm (Fig. 2). The distance between the control gate and the floating gate is 15 nm (sufficiently high to avoid a second tunneling effect). For the simulations, a structured full-quad mesh composed by rectangular elements (2 nm × 0.4 nm) has been used at the interface region between the semiconductor and the top oxide. In details, an 800 nm × 10 nm fine-meshed layer in the semiconductor and a 280 nm × 8 nm fine-meshed layer in the oxide tunneling region were defined. Elsewhere, an unstructured triangular mesh limited by a maximum size of 40 nm has been adopted, except for the boundaries of the source and drain regions and of the control and floating gates, where the maximum mesh size has been limited to 10 nm.

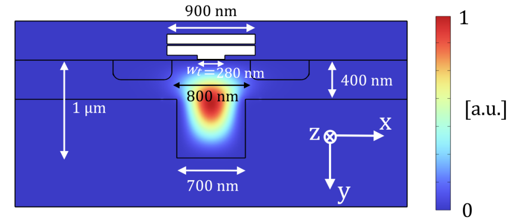

Fig. 2. Poynting vector along z in the PTFGMOS, arbitrary units.

A. Optical Simulations

The cross section of the PTFGMOS consists of a 400-nm-high silicon slab, and an additional 700 × 600 nm^2 silicon region buried in SiO_2. Refractive indices of 3.65, 2.021 and 1.4525 have been used for silicon, silicon nitride and silicon dioxide, respectively, and an extinction coefficient $k_{Si} = 0.004$ (from which the power absorption coefficient, α, can be derived as $\alpha = 4\pi k_{Si}\ /\lambda$, with λ the optical wavelength) for silicon [26]. The real part of the effective refractive index of the PTFGMOS has been calculated to be 3.590, for $\lambda = 850$ nm. The normalized Poynting vector along the propagation direction of the optical mode is shown in Fig. 2. The insertion loss at the end-fire coupling between the silicon nitride waveguide (Fig. 1b) mode (having effective refractive index equal to 1.886) and the PTFGMOS (Fig. 1c) one has been evaluated with optical simulations (EigenMode Expansion, EME, [27] simulations with Perfectly Matched Layer boundary conditions at the edges of the simulation region) to be around 1 dB. By combining optical and semiconductor simulations (with Eq. (4)) in the PTFGMOS region, it has been possible to simulate the writing, the reading, and the erasing operations.

B. Hysteresis in the PTFGMOS

The photogenerated electrons get trapped in the floating gate in a non-volatile way, thanks to the high voltage applied to the control gate. The non-volatility of the memory has been checked by verifying the presence of hysteresis when applying a sinusoidal voltage (with three different frequencies) to the control gate of the PTFGMOS cell (in the presence of

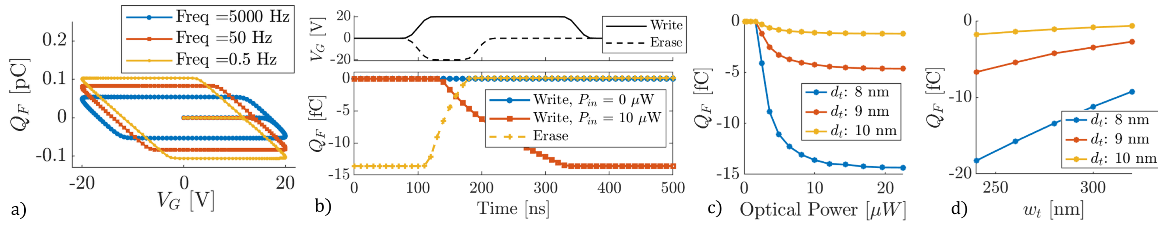

Fig. 3. (a) Hysteresis in the PTFGMOS, for a sinusoidal input at the gate voltage (drain and source in high impedance). (b) V_G and Q_F vs time during writing (with optical power of 0 μW and 10 μW) and erasing operations. (c) Q_F after writing as a function of the input optical power for three values of the tunnel thickness (d_t). (d) Q_F as a function of the width (w_t) of the tunnelling region, for three values of the tunnel thickness (d_t).

10 μW of input light in TE mode), while keeping the drain and source contacts as high impedance (Fig. 3a). For positive gate voltages, $A^n_{FN} = 1.23 \cdot 10^{-6}$A/V^2 and $B^n_{FN} = 237$ MV/cm have been used, whereas for negative gate voltages, $A^n_{FN} = 1.82 \cdot 10^{-7}$A/V^2 and $B^n_{FN} = 188$ MV/cm [22].

C. Writing, Reading and Erasing

The writing operation has been simulated (Fig. 3b). An analysis in the time domain has been performed, by considering a voltage pulse applied to the control gate (V_G) with a peak value of 20 V both in the absence and in the presence of light (10 μW in the fundamental TE mode). The control gate pulse consists of 200 ns with a high state voltage of 20 V, with additional 50 ns transition zone at the start and 50 ns transition zone at the end of the pulse. In the presence of light, the photogenerated electrons get trapped in the floating gate, leading to a value of trapped charge $Q_F = -13.6$ fC. In the absence of light, the change in the trapped charge in the floating gate is negligible when the gate pulse is applied. This represents the effectiveness of the writing operation. In fact, the trapped charges in the two cases (presence and absence of input light of 10 μW) are distinguishable after the control gate pulse finishes. The charge trapped in the floating gate is much lower than in the cases shown in Fig. 3a, because of the fast writing time, compared to the slow (sinusoidal) inputs in Fig. 3a. Fig. 3c shows the dependence of the charge Q_F as a function of the input optical power (with the same writing gate pulse used in simulations in Fig. 3b), for three values of the tunnel thickness (d_t), around the chosen value of 8 nm. It is evident that for input power higher than 10 μW, the stored charge can be considered approximately constant. Fig. 3d shows the trapped charge (after the same writing gate pulse used in simulations in Fig. 3b) as a function of the width, w_t, of the tunnelling interface, for three values of the tunnel thickness (d_t).

To erase a written PTFGMOS cell, high reversed voltage is applied to the control gate, with source, drain and base contacts grounded. A voltage pulse of -20 V (with a duration of 194 ns, with additional 50 ns at the start transition zone and 50 ns at the end transition zone) has been applied to the control gate, to force the erasing operation in the memory (Fig. 3b).

The reading operation is based on the change in the threshold voltage of the PTFGMOS in the presence of trapped electrons in the floating gate. As it can be seen from Fig. 4a, the threshold voltage (V_{T1}) in case of $Q_F = -13.6$ fC is higher than the threshold voltage (V_{T0}) corresponding to zero trapped charge. By applying a control gate voltage of $V_R = 1.25$ V, a current of 40 μA can be obtained in case of written memory, for $V_{DS} = 100$ mV, whereas negligible current is obtained in no charge condition. Since the device can be implemented in an electronic circuit, a proposal for its electrical symbol is shown in Fig. 4b.

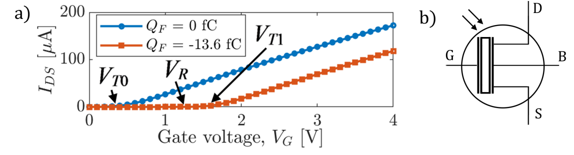

Fig. 4. (a) Reading. I_{DS} vs V_G, for the two values of Q_F ($V_{DS} = 0.1$V). (b) Proposal for an electrical symbol for the PTFGMOS.

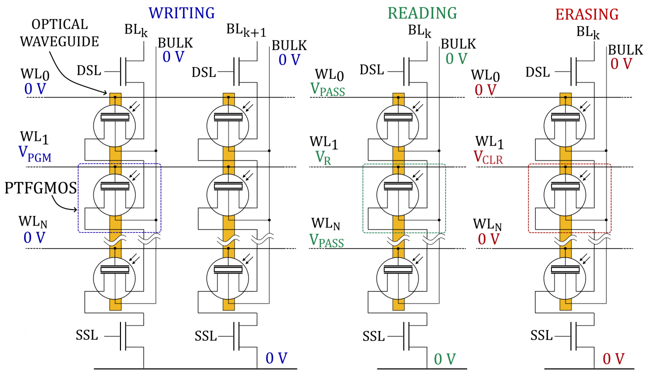

Fig. 5. PTFGMOS NAND array (writing, reading and erasing).

V. PTFGMOS Array

Fig. 5 shows a schematic for the writing, reading and erasing processes in a PTFGMOS array. For the writing operation, the wordline (WL_1 in Fig. 5) is set at $V_{PGM} = 20$ V. Simultaneously, the presence of light in the waveguide crossing all the PTFGMOSs in the same bitline (BL_k), enables the identification of the single cell to be written (Fig. 5). It should be noticed that the wordline (WL) contacts, connected to the control gates, are arranged to be perpendicular to the direction of the waveguide, as shown in Fig. 5. Since each PTFGMOS cell absorbs around 25% of optical power, ten WLs would require an input power of 180 μW (to ensure at least 10 μW reaching the last PTFGMOS on the same BL). During the reading operation, the drain selection line (DSL) and the source selection line (SSL) voltages are set to make the corresponding transistors work as pass transistors, as it happens in classical NAND flash memories, and the gate voltage of the PTFGMOS to be read (WL_1 in Fig. 5) is set to $V_R = 1.25$ V, whereas the other WLs are set to a voltage V_{PASS} higher than both V_{T0} and V_{T1} Finally, during the erasing process, an entire WL is erased with $V_{CLR} = -20$ V and bulk set to 0 V.

VI. Conclusion

A Photon-Triggered Floating Gate Metal-Oxide-Semiconductor (PTFGMOS) has been presented as a non-volatile optoelectronic memory. It could pave the way to new low-cost applications, including neuromorphic photonics.

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