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ELECTRICAL AND INFORMATION ENGINEERING

Ph.D. Program

SSD: ING/IND-32 - CONVERTERS, ELECTRICAL MACHINES AND DRIVES

Final Dissertation

Advanced Control and Modulation Strategies for High-Performance Multilevel Power Converters

---

by

Lara Bruno

Supervisor:

Prof. Vito Giuseppe Monopoli

Coordinator of Ph.D Program:

Prof. Mario Carpentieri

XXXVIII Cycle - November 1st, 2022 - October 31st, 2025

Politecnico di Bari

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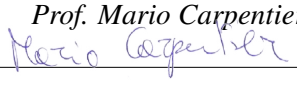
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XXXVIII Cycle - November 1st, 2022 - October 31st, 2025

Abstract (eng)

This thesis reports the outcomes of three years of doctoral research undertaken during the XXXVIII cycle of the PhD Program in Electrical and Information Engineering at the Polytechnic University of Bari. Conducted at the Power Electronics Laboratory of the same institution, the work investigates and develops advanced modulation strategies for multilevel power converters, with the primary aim of improving efficiency, reliability, and grid harmonic performance in both drive and grid-connected applications. As part of this work, a six-month research stay has been undertaken at Eidgenössische Technische Hochschule (ETH), Zurich, Switzerland.

Beginning with an in-depth analysis of conventional Pulse Width Modulation techniques for multilevel converters, particularly the Cascaded H-Bridge topology, the work develops optimized phase-shift Pulse Width Modulation methods to minimize harmonic distortion while maintaining low switching losses. Analytical derivations are complemented by extensive experimental validation carried out on the dedicated setups of the Power Electronics Laboratory at the Polytechnic University of Bari, which also reveal the inherent limitations of conventional PWM, especially its inability to independently control pulses within each control period. Building on these findings, the research introduces a novel Pulse Position Modulation scheme that generates gate signals as a sum of individually timed pulses optimized for specific harmonic objectives, thereby increasing the modulation degrees of freedom and enabling more precise harmonic cancellation with reduced

switching losses and fast dynamic performance. The proposed method is first validated on a full-bridge converter and then applied to two-level inverters to suppress common-mode voltage, reduce leakage currents, and enhance the operational lifetime of photovoltaic panels and motor bearings. Pulse Position Modulation is subsequently extended to multilevel Cascaded H-Bridge converters to mitigate harmonics under unbalanced conditions, with experimental results on laboratory prototypes demonstrating superior performance compared to traditional modulation strategies. The thesis further proposes an innovative interleaved Cascaded H-Bridge topology designed to increase voltage levels while reducing the number of semiconductor devices, supported by a dedicated modulation strategy whose experimental validation confirms improvements in scalability, harmonic performance, and overall efficiency. Finally, an enhanced modulation and control approach is applied to the Flying Capacitor Buck Converter, leveraging the flying capacitor as an energy buffer for active damping and improved DC system stability. This last contribution, developed during a six-month visiting period at ETH Zurich, shows how advanced modulation and control strategies can reduce the need for input filters and additional damping circuits, thereby consolidating the role of innovative control strategies in optimizing converter performance.

This thesis ultimately demonstrates that advanced and experimentally validated modulation strategies are not simply auxiliary control tools but constitute the core enabling technology that drives the evolution of high-performance, reliable and sustainable next-generation power converters.

Abstract (it)

Questo lavoro di tesi illustra i risultati di tre anni di ricerca svolta durante il XXXVIII ciclo del Dottorato di Ricerca in Ingegneria Elettrica e dell'Informazione presso il Politecnico di Bari. Condotta presso il Laboratorio di Convertitori Elettronici di Potenza dello stesso Ateneo, la ricerca si è concentrata sull'analisi e lo sviluppo di strategie di modulazione avanzate per convertitori elettronici di potenza multilivello, con l'obiettivo di migliorarne l'efficienza, l'affidabilità e la qualità armonica dei segnali in uscita, sia nelle applicazioni legate agli azionamenti elettrici sia in quelle connesse alla rete elettrica. Durante questo percorso è stato inoltre svolto un periodo di ricerca di sei mesi presso l'Eidgenössische Technische Hochschule (ETH) di Zurigo, in Svizzera.

Partendo da un'analisi approfondita delle tecniche convenzionali di Pulse Width Modulation per convertitori multilivello, in particolare per la topologia Cascaded H-Bridge, la tesi sviluppa metodi innovativi a sfasamento ottimizzato, volti a ridurre la distorsione armonica in rete mantenendo contenute le perdite di commutazione. Le deduzioni teoriche sono supportate da un'ampia validazione sperimentale condotta sui banchi prova dedicati del Laboratorio di Convertitori Elettronici di Potenza del Politecnico di Bari, che evidenziano anche i limiti intrinseci delle tecniche convenzionali, in particolare l'impossibilità di controllare in modo indipendente gli impulsi all'interno di ciascun periodo di controllo. Sulla base di queste osservazioni, la tesi introduce una tecnica innovativa, denominata Pulse Position Modulation, capace di generare i segnali di controllo come somma di impulsi temporalmente definiti, la

cui posizione viene ottimizzata per ogni periodo di controllo per perseguire specifici obiettivi armonici. Questa soluzione aumenta i gradi di libertà della modulazione, consentendo una più precisa cancellazione armonica, riducendo le perdite di commutazione e migliorando le prestazioni dinamiche. Il metodo è inizialmente validato su un convertitore full-bridge e successivamente applicato a un inverter a due livelli, con l'obiettivo di sopprimere la tensione di modo comune, ridurre le correnti di dispersione e prolungare dunque la vita utile dei pannelli fotovoltaici o dei cuscinetti dei motori, a seconda dell'applicazione. La Pulse Position Modulation viene poi estesa ai convertitori multilivello Cascaded H-Bridge per mitigare le armoniche in condizioni sbilanciate, accompagnata da risultati sperimentali sul setup del Laboratorio di Convertitori Elettronici di Potenza, che ne confermano la superiorità rispetto alle strategie tradizionali. La tesi propone inoltre una topologia innovativa di Cascaded H-Bridge *interleaved*, progettata per aumentare i livelli di tensione riducendo il numero di dispositivi semiconduttori, supportata da una strategia di modulazione dedicata la cui validazione sperimentale dimostra significativi miglioramenti in termini di scalabilità, prestazioni armoniche ed efficienza complessiva. Infine, una strategia di modulazione e di controllo avanzata è applicata al Flying Capacitor Buck Converter, sfruttando il condensatore del convertitore come buffer energetico per fare *active damping* e per il miglioramento della stabilità dei sistemi in corrente continua. Questa attività, sviluppata durante il periodo di ricerca presso l'ETH di Zurigo, dimostra come le tecniche di modulazione e di controllo avanzate possano ridurre la necessità di filtri di ingresso e circuiti di smorzamento aggiuntivi, consolidando l'importanza di strategie di modulazione innovative per ottimizzare le prestazioni dei convertitori di potenza.

Dunque, la tesi dimostra come le strategie di modulazione avanzate, validate sperimentalmente, costituiscano il fulcro tecnologico per lo sviluppo dei convertitori di potenza di nuova generazione, elevandone efficienza, affidabilità e sostenibilità.

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Chapter 1

Introduction

The global energy scenario is experiencing a great transformation. The growing dependence on fossil fuels, together with the continuous increase of their cost, has accelerated the need for significant economic and human investments in the development of alternative energy sources that are both sustainable and cost-effective. For decades, renewable energy technologies have been at the center of research efforts, and their integration into the electrical grid has been made possible through the design and evolution of different families of power electronic converters.

In modern transmission and distribution systems, high-power electronic solutions are essential not only to ensure the reliable delivery of energy but also to guarantee power quality. Consequently, power electronic converters are required to achieve these tasks with high levels of efficiency. The continuous rise in global energy demand has stimulated the emergence of new converter topologies and the advancement of semiconductor technologies capable of handling higher voltage and current levels. The race to develop next-generation devices has led to components that can withstand up to approximately 6.5 kV and 2.5 kA. However, a strong competition still exists between conventional high-power converter topologies based on high-voltage semiconductors and innovative multilevel architectures relying on mature medium-voltage devices.

In this context, multilevel converters have emerged as an attractive solution for medium- and high-power applications. They enable the achievement of high power ratings while exploiting reliable and commercially mature semiconductor technology. Compared with traditional two-level converters, multilevel converters offer significant advantages, particularly in terms of output waveform quality and nominal power capability. For example, as the number of voltage levels increases, the total harmonic distortion (THD) of the output waveform is reduced, leading to improved performance.

These advantages have made multilevel converters a highly active research field worldwide. Current investigations focus not only on developing novel converter topologies but also on enhancing their performance through advanced control and optimization techniques. Research topics include simplification of control schemes, optimization algorithms to minimize THD, DC-link voltage balancing, current ripple mitigation, harmonic elimination through pre-calculated switching functions, compliance with increasingly stringent grid codes, and hybrid architectures that combine features of different topologies.

1.1 Motivation and goal of the thesis

The motivation of this PhD thesis stems from the pivotal role of modulation techniques in the operation of multilevel converters, as they directly influence efficiency, reliability and the quality of the output waveforms. Power losses and harmonic performance are intrinsically linked to the strategy adopted for generating the gating signals of semiconductor devices, which makes modulation one of the most significant and enduring research topics in power electronics. Each new multilevel topology is therefore accompanied by dedicated modulation schemes, specifically designed to reduce switching and conduction losses while maximizing harmonic performance. Beyond the intrinsic performance of the converters themselves, ad-

vanced modulation techniques also play a decisive role in limiting the harmonic distortions injected into the grid, thereby enhancing system stability and ensuring compliance with increasingly stringent regulatory requirements. Although many of these methods can be regarded as refinements or extensions of techniques originally conceived for two-level converters, their relevance becomes even more critical in the context of multilevel architectures, where the higher degree of complexity demands more sophisticated and tailored solutions. Within this framework, the investigation and advancement of modulation strategies for multilevel converters constitute the central motivation and primary objective of the present doctoral research.

Building upon this general motivation, the research begins with an in-depth analysis of conventional Pulse Width Modulation (PWM) techniques for application to multilevel converters, with particular emphasis on the Cascaded H-Bridge (CHB) topology, in order to meet specific harmonic objectives, namely the mitigation and cancellation of grid harmonics. To this end, optimization procedures are applied to conventional phase-shifted PWM strategies to introduce targeted harmonic components capable of cancelling undesirable distortions within the electrical grid, thereby enabling the converter to operate as an active grid harmonic compensator. The innovative methods developed in this work focus on the determination of optimized carrier phase-shift angles for multilevel converters, with the dual aim of achieving prescribed harmonic cancellations and reducing switching losses, thereby extending the operational lifetime of the converter.

A detailed investigation of PWM techniques, however, reveals inherent limitations in their harmonic performance. A close examination of the PWM signal generation process shows that each individual pulse is constrained to a fixed position within its control period, as it results from the comparison between a carrier and a modulating signal. Consequently, any phase shift applied to the signal affects all pulses uniformly, making it impossible to control each pulse individually. Building on this observation, the present thesis introduces a completely novel modulation

approach for power converters, which directly synthesizes the control signal as a sum of individual pulses defined within each control period. The position of each pulse is determined through dedicated optimization procedures aimed at achieving prescribed harmonic objectives. This strategy introduces a significantly higher number of degrees of freedom, enabling more precise harmonic cancellation while simultaneously simplifying the implementation of the modulation technique.

The modulation technique developed during this PhD program, referred to as Pulse Position Modulation (PPM), is initially validated on a simple full-bridge module configuration to demonstrate its capability to simultaneously enhance harmonic performance and dynamic response. Subsequently, the potential of PPM is exploited to minimize common-mode voltage in a conventional inverter configuration, with the objective of reducing leakage currents circulating through photovoltaic panels or motor bearings, thereby addressing both grid-connected and drive applications. After establishing the advantages of PPM in conventional converter topologies, the method is extended to a multilevel CHB configuration to eliminate undesired harmonics arising under unbalanced operating conditions, such as non-uniform solar irradiance, differing battery states of charge, or the application of active thermal control methods. The effectiveness of PPM across these three configurations is demonstrated in this thesis through experimental tests carried out on the dedicated setups at the Polytechnic University of Bari, evidencing its marked superiority over traditional modulation strategies reported in the literature. In this way, the development of PPM opens a new direction in the field of modulation techniques, introducing an entirely original paradigm for converter control.

Building upon the extensive investigation of the conventional CHB converter and its modulation, the research then explores an alternative topology to further demonstrate the crucial role of dedicated modulation schemes. Traditional CHB configurations typically employ high-current power switches, which considerably increase system costs and limit their suitability for low-voltage, high-power ap-

plications. To address these constraints, this thesis introduces an enhanced CHB topology based on interleaved full-bridge submodules. By interleaving multiple submodules within each cell, the proposed configuration allows the use of smaller and lower-cost switching devices, while markedly improving the converter's scalability with respect to output current. For this innovative architecture, a dedicated modulation strategy has also been developed to fully exploit the benefits of the interleaved structure. The effectiveness of the proposed topology and its modulation approach is substantiated by experimental results, which will be presented and discussed throughout this thesis.

Finally, the last part of this thesis focuses on the development and analysis of an innovative, dedicated control strategy, accompanied by a specific modulation approach, for a different class of multilevel converter: the Flying Capacitor Buck Converter (FCBC). This approach is specifically designed to exploit the inherent capability of the flying capacitor to act as an energy buffer, thereby enabling active damping and enhancing the stability of DC systems while reducing the need for input filters and eliminating additional damping circuits. This line of research has been carried out during a visiting period at the Eidgenössische Technische Hochschule (ETH) in Zurich, Switzerland. The results obtained once again highlight the pivotal role of control and modulation techniques in achieving targeted performance objectives and unlocking the full potential of advanced converter topologies.

1.2 Structure of the thesis

The thesis has been organized as follows.

- Chapter 2 addresses multilevel power converters, with particular emphasis on the CHB configuration, presenting the modulation and control techniques

reported in the literature. It also includes experimental waveforms obtained from a three-phase closed-loop scheme developed during the PhD program at the Polytechnic University of Bari.

- Chapter 3 presents two novel optimized phase-shift PWM strategies designed to mitigate harmonic pollution in the electrical grid while simultaneously minimizing switching losses. The discussion is supported by a rigorous analytical treatment and validated through experimental evidence.

- Chapter 4 provides a comprehensive description of the proposed PPM technique. It opens with a rigorous mathematical formulation of a generic PPM gating signal and its distinctive features, followed by an experimental validation on a full-bridge topology to demonstrate the method's effectiveness. Then, the application of the PPM strategy to reduce common-mode voltage in a conventional three-phase two-level inverter is explored. A comprehensive mathematical formulation is developed, and experimental results demonstrate that PPM effectively limits leakage currents, thereby extending the operational lifetime of photovoltaic panels and motor bearings.

- Chapter 5 presents the experimental validation of the proposed PPM strategy applied to CHB converters. The chapter aims to demonstrate the capability of the PPM technique to enhance the harmonic quality of CHB output waveforms, particularly under unbalanced operating conditions. After recalling the simulation-based comparison with conventional PS-PWM and optimized VPS-PWM schemes, the same analysis is extended to the experimental setup. The results confirm PPM effectiveness and practical feasibility in multilevel converter applications.

- Chapter 6 introduces a novel CHB topology based on the interleaving of full-bridge submodules, designed to increase the number of voltage levels and im-

prove harmonic quality while using fewer semiconductor devices. Following an analytical derivation of the associated modulation technique, experimental results confirm the effectiveness of the proposed configuration.

- Chapter 7 presents the results obtained during the visiting period at ETH, focusing on an innovative active damping method that leverages the energy-buffering capability of the flying capacitor in a FCBC. The approach is thoroughly validated through detailed simulation results.

- Finally, the conclusions of the thesis are drawn in the final chapter.

1.3 List of scientific publications

1.3.1 Journals

1. L. Bruno, R. Mandrioli, M. Ricco and V. G. Monopoli, "A Novel Interleaved Full-Bridge Submodule Architecture for High-Performance Cascaded H-Bridge Converters," in IEEE Transactions on Industrial Electronics (submitted).

2. L. Bruno and V. G. Monopoli, "An Innovative Strategy for Common-Mode Voltage Reduction in Three-Phase Voltage-Source Inverters Based on Pulse Position Modulation," in IEEE Transactions on Industrial Electronics, doi: 10.1109/TIE.2025.3579093.

3. L. Bruno and V. G. Monopoli, "A New Synthesis Technique of Control Signals for Power Converters Based on Pulse Position Modulation," in IEEE Access, vol. 12, pp. 188625-188636, 2024, doi: 10.1109/ACCESS.2024.3516193.

4. L. Bruno, D. D'Amato, R. Leuzzi and V. G. Monopoli, "Analysis of Electrical Aging Effects on AC High Frequency Motor Based on Exchange Market

Algorithm Model Parameter Identification," in IEEE Access, vol. 12, pp. 32753-32761, 2024, doi: 10.1109/ACCESS.2024.3371861.

5. A. M. Alcaide et al., "Extremely Low Frequency PS-PWM Based Technique for Cascaded H-Bridge Converters With Grid Voltage Compensation Capability," in IEEE Transactions on Industrial Electronics, vol. 71, no. 4, pp. 3242-3252, April 2024, doi: 10.1109/TIE.2023.3274870.

6. V. G. Monopoli et al., "A Hybrid Modulation Technique for Operating Medium-Voltage High-Power CHB Converters Under Grid Voltage Disturbances," in IEEE Transactions on Industrial Electronics, vol. 71, no. 1, pp. 462-472, Jan. 2024, doi: 10.1109/TIE.2023.3241246.

1.3.2 Conferences proceedings

1. L. Bruno, R. Mandrioli, M. Ricco and V. G. Monopoli, "Cascaded H-Bridge Based on Interleaved Full-Bridge Submodules," *IECON 2025 - 51st Annual Conference of the IEEE Industrial Electronics Society, Madrid, Spain, 2025*.

2. M. Jeong, L. Bruno and J. Biela, "Transient Power Decoupling of 3-level Flying Capacitor Buck Converter: Removing Negative Input-resistance for Extended Frequency Range," *10th IEEE Workshop on the Electronic Grid (eGrid 2025), Glasgow, Scotland, 2025*.

3. L. Bruno, R. Leuzzi and V. G. Monopoli, "Efficiency and Harmonic Quality Improvement in a Cascaded H-Bridge Converter Through an Innovative Carrier Signal," *2023 IEEE Energy Conversion Congress and Exposition (ECCE)*, Nashville, TN, USA, 2023, pp. 3466–3473, doi: 10.1109/ECCE53617.2023.10362440.

Chapter 2

Multilevel Power Converters

The increasing demand for power converters capable of interfacing with medium-voltage (MV) grids and supplying MV loads has fostered significant advancements in both converter topologies and semiconductor technologies suitable for such voltage levels. Within this context, two predominant design approaches have emerged. The first relies on conventional converter topologies implemented with high-voltage semiconductor devices, while the second is based on modular multilevel architectures employing low- or medium-voltage devices. In general, multilevel converters are defined as DC–AC conversion systems able to synthesize more than three discrete voltage levels at the output terminals [1–3].

Among the various advantages of the multilevel topology, there is the ability to guarantee automatic voltage sharing among power semiconductor devices, eliminating the need for series connections. In addition, multilevel waveforms are characterized by significant harmonic distortion reduction for a given switching frequency, thereby improving power quality and system efficiency. The smaller voltage steps typical of multilevel waveforms also contribute to electromagnetic interference (EMI) reduction, which decreases filtering requirements and insulation stress. Furthermore, multilevel topologies properly generate lower common-mode voltages, effectively reducing electrical stress on motor bearings in electric drive

systems and leakage currents in photovoltaic panels, and enhancing overall system reliability.

During the PhD research, a thorough investigation of the Cascaded H-Bridge (CHB) topology has been conducted, focusing on the development and implementation of techniques aimed at enhancing efficiency and improving the harmonic quality of output waveforms under conditions of external disturbances and unbalanced operation. Therefore, after investigating the most important multilevel topologies, this chapter begins with an overview of the CHB converter structure, followed by a review of the main modulation techniques discussed in the literature. The analysis then focuses on output current control strategies, with particular emphasis on the discrete controller implemented for a three-phase grid-connected CHB converter. This controller has been experimentally validated through laboratory testing. The chapter concludes with the presentation and analysis of the corresponding experimental results.

2.1 Review of multilevel topologies

Over the years, various multilevel converter topologies have been proposed, but only a limited number have achieved industrial attention. The most known are the Neutral-Point Clamped (NPC), Active NPC (ANPC), Flying Capacitor (FC), and Nested NPC (NNPC) converters, which typically operate in the 2.3-4.16 kV range. Even if they are effective in certain applications, these topologies require significant modifications to increase voltage levels, making them less attractive for high-power systems due to cost and reliability issues [4–8].

To overcome these limitations, cascaded converter topologies, also known as multi-cell converters, have been introduced, such as the CHB and Cascaded NPC (CNPC), which are built from modular low-power submodules with isolated DC sources [9, 10]. These converters offer scalability, fault-tolerant operation, and are

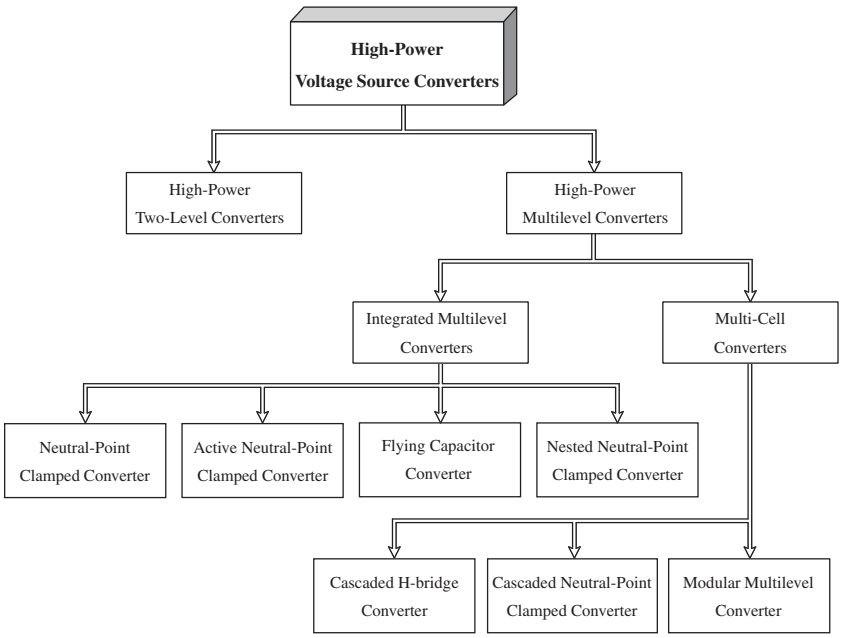


Figure 2.1: Classification of voltage source converters [13].

suitable for voltages up to 13.8 kV. However, they require bulky and costly transformers to supply isolated voltages.

Another relevant topology is the Modular Multilevel Converter (MMC), which also employs a modular structure with cascaded submodules but does not rely on isolated DC sources [11, 12]. This design choice eliminates the need for transformers and supports high-voltage operation, making MMCs suitable for a broad range of applications. Then, CHB, CNPC, and MMC offer distinct advantages and limitations depending on system requirements, application context, and design priorities. The most important developments in voltage source converters are shown in Fig. 2.1, with a particular focus on multilevel converters.

2.2 Cascaded H-Bridge converter

As previously stated, the CHB converter represents a highly promising solution for various high- and medium-voltage applications, including medium-voltage drives, high-voltage direct current (HVDC) transmission systems, the integration of re-

newable energy sources into the grid, and power quality improvement systems such as STATCOMs. Its advantageous features include full modularity using low- or medium-voltage power semiconductor devices, fault-tolerant operation due to module redundancy, and ease of maintenance. These benefits are a direct consequence of its design, based on the power electronics building block approach, achieved through the series connection of multiple power modules.

2.2.1 Structure and topology

The generalized circuit configuration of a three-phase CHB in shown in Fig. 2.2. The CHB converter consists of a series connection of H-bridge power cells, where each cell is made up of a single-phase, 3-level H-bridge inverter and an isolated DC voltage source. This series arrangement of H-bridge modules naturally increases both the output voltage and the overall power rating of the converter. The topology enables the generation of waveforms with a greater number of voltage levels, thereby reducing harmonic distortion. Furthermore, this structure allows the converter to achieve medium or high voltage levels while utilizing only standard low-voltage technology components. The phase voltage is obtained by summing the voltages produced by each submodule, meaning that the voltage levels are directly influenced by the number of modules connected in series, as described by the following equation:

$$N_{levels} = 2N + 1 \tag{2.1}$$

where N is the number of modules connected in series per phase and N_{levels} is the number of output voltage levels.

Examining the individual submodule (such as the first submodule of phase A), it can be described as a fundamental DC/AC power conversion circuit, typically comprising low-voltage IGBT devices and a DC-link capacitor. As previously men-

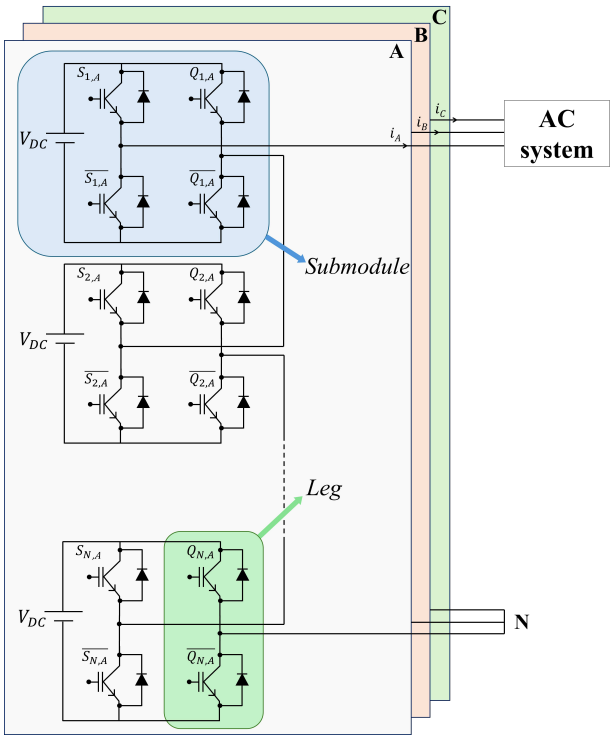


Figure 2.2: Configuration of Cascaded H-Bridge.

Table 2.1: Switching states of H-bridge submodule

State	$S_{1,A}$	$\overline{Q_{1,A}}$	$v_{HB,1,A}$
1	1	1	V_{DC}
2	1	0	0
3	0	1	0
4	0	0	$-V_{DC}$

tioned, the full-bridge configuration, commonly known as the H-bridge converter, is widely used in CHB converters. The circuit diagram of the first H-bridge submodule of phase A is illustrated in Fig. 2.3. It consists of two half-bridge legs ($S_{1,A}$, $\overline{S_{1,A}}$ and $Q_{1,A}$, $\overline{Q_{1,A}}$), each paired with a DC-link capacitor and its own independent DC voltage source. Each leg includes two IGBT devices, accompanied by antiparallel diodes, and they operate in a complementary manner. All possible combination of switching states for $S_{1,A}$ and $\overline{Q_{1,A}}$ are shown in Table 3.1, which generate three voltage levels, "0", "V_{DC}" and "$-V_{DC}$".

Fig. 2.3 also illustrates the AC output voltage of the H-bridge submodule, which

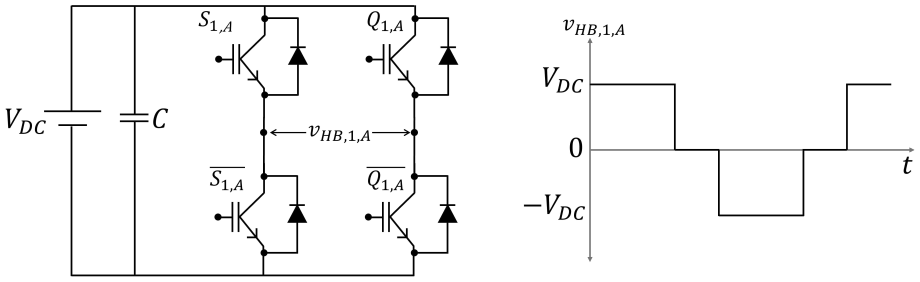


Figure 2.3: Full-bridge submodule and output voltage waveform.

is synthesized according to the following equation:

$$v_{HB,1,A} = (S_{1,A}\overline{Q_{1,A}} - Q_{1,A}\overline{S_{1,A}})V_{DC} \tag{2.2}$$

Thus, the key advantages of the CHB configuration can be summarized as follows:

- Its modular design allows for easy scalability in both voltage and power ratings.
- It is capable of generating output voltage and current waveforms that exhibit reduced dv/dt and minimal ripple, typically resulting in a very low total harmonic distortion (THD).
- It enables the generation of output voltage waveforms with a high number of voltage levels, facilitating operation of the H-bridge submodules at significantly low switching frequencies.

2.2.2 Modulation techniques

Modulation techniques are essential for regulating the AC output voltage of power converters, enabling it to track the reference value determined by the control system. This desired AC output voltage is achieved by adjusting the duty cycle of the switching devices, with the modulation technique playing a critical role in

this process. Furthermore, modulation schemes are designed to address additional control objectives, including voltage balancing, minimization of power losses, reduction of common-mode voltage, and suppression of current ripple, among others. Among the most common modulation techniques, carrier-based methods are the most widely used due to their practical implementation. In the case of two-level power converters, carrier-based modulation involves comparing the modulating signal with a single triangular (or sawtooth) carrier signal to generate the gating signals for the converter's switching devices. This carrier modulation approach can be extended to multilevel converters, where multiple triangular carrier signals are compared with a phase modulating signal to produce the gating signals. This technique is commonly referred to as a multi-carrier modulation scheme. Depending on the arrangement of the carriers, multi-carrier modulation schemes can be classified into phase-shift pulse width modulation (PS-PWM) and level-shift pulse width modulation (LS-PWM). In PS-PWM, the triangular carrier signals, each with the same magnitude, are arranged horizontally. In contrast, in LS-PWM, the triangular carrier signals with identical magnitudes are vertically aligned. Further classification of LS-PWM is based on the phase relationship between adjacent carriers, leading to three distinct schemes: phase-disposition (PD-PWM), phase-opposition-disposition (POD-PWM), and alternate phase-opposition-disposition (APOD-PWM). These modulation schemes fall within the high switching frequency category ($f_{sw} > 2000\,\text{Hz}$) and are commonly used to control multilevel power converters due to their straightforward implementation and ease of extension to systems with a higher number of voltage levels. However, they are associated with higher switching losses when compared to modulation schemes that operate at lower or fundamental switching frequencies [14–18].

The sampled average modulation (SAM) and space vector modulation (SVM) schemes are categorized as low switching frequency modulation techniques ($100\,\text{Hz} < f_{sw} < 2000\,\text{Hz}$). The SAM approach directly controls the phase voltages of a CHB,

implicitly generating the line-to-line voltages. In contrast, the SVM method directly controls the line-to-line voltages of a CHB, with the phase voltages being generated implicitly. The SAM technique is easily extendable to CHBs with any number of submodules without requiring modifications to the implementation algorithm. However, the SVM approach becomes more challenging to implement as the number of submodules in a CHB increases [19, 20]

Fundamental switching frequency modulation schemes are widely used in high-power converters like CHBs, due to their ability to minimize switching losses by operating the power converters at the fundamental frequency. Selective harmonic elimination/mitigation (SHE/SHM) schemes fall within this category. SHE/SHM schemes provide high-quality output waveforms and precise control over output voltage harmonics, while keeping the device switching frequency low in comparison to other modulation techniques. The implementation of the SHE/SHM scheme primarily involves offline calculation of switching angles and solving non-linear equations. However, as the number of voltage levels increases, the number of switching angles grows significantly, making it increasingly difficult to solve for such a large set of switching angles [21, 22].

The detailed performance of a selection of these modulation techniques applied to CHB converter is presented in the following subsections.

a. Phase-Shift Pulse Width Modulation

The modulation scheme involving the horizontal arrangement of identical triangular carrier signals is referred to as PS-PWM. In PS-PWM, all triangular carriers share the same frequency and peak-to-peak amplitude, but exhibit a phase shift between adjacent signals. This strategy requires one triangular carrier for each submodule of the CHB, resulting in N carrier signals. These N carriers are arranged with a phase shift ϕ_c, as illustrated in Fig. 2.4, where a simplified scheme with only three carrier

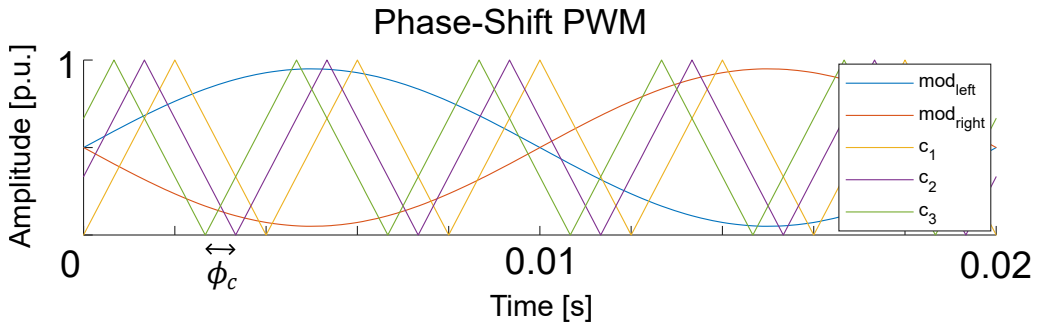


Figure 2.4: The Phase-Shift PWM strategy.

signals is shown. The phase shift ϕ_c between the carrier signals is determined by the following equation:

$$\phi_c = \frac{2\pi}{N} \tag{2.3}$$

As previously mentioned, each CHB submodule consists of two half-bridge legs that form the H-bridge. Consequently, two 50 Hz sinusoidal modulating signals, in phase opposition, are required, one for each leg, as depicted in Fig. 2.4. By comparing the modulating signals with the carrier signals, the driving signals required for the CHB devices are determined.

PS-PWM is particularly appealing due to its simplicity of implementation. Additionally, it ensures that the semiconductor stress and the power handled by each submodule are evenly distributed, preventing any device from aging prematurely compared to the others.

b. Level-Shift Pulse Width Modulation

In LS-PWM, the triangular carrier signals, which have identical peak-to-peak magnitude and frequency, are vertically aligned within the linear modulation region. However, this modulation scheme is less preferred due to its tendency to cause an uneven distribution of power loss across the submodules and devices. Depending on the phase relationship between adjacent carriers, LS-PWM can be further cate-

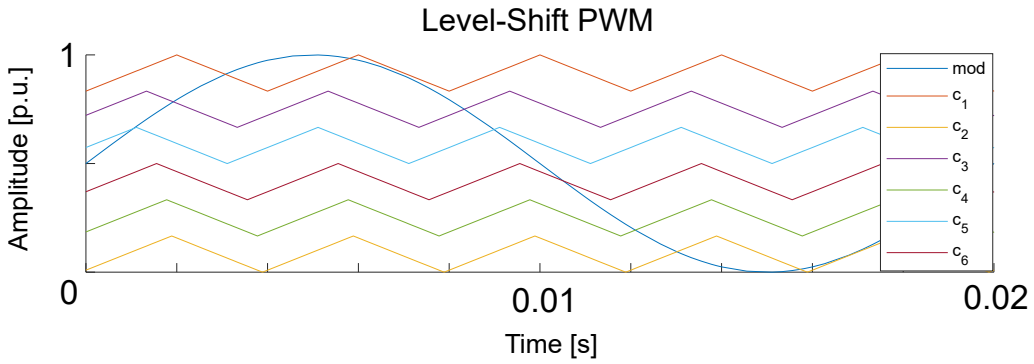


Figure 2.5: The Level-Shift PWM strategy.

gorized into three variations:

- PD-PWM, where the triangular carrier signals are vertically arranged in-phase with each other, as shown in Fig. 2.5, where a simplified scheme applied to a 3-cells CHB is shown.
- POD-PWM, where the triangular carrier signals above the sinusoidal reference zero are in-phase, while those below the sinusoidal reference zero are in phase opposition.
- APOD-PWM, where all the triangular carriers are alternately arranged in phase opposition.

To control a CHB with N cells, $2N$ carrier signals are needed, one for each top switch of the converter. Among these, the PD-PWM strategy is widely preferred, as it produces an output voltage with the lowest THD.

c. Selective Harmonic Elimination/Mitigation

SHE/SHM methods are modulation schemes specifically designed for high-power converters to meet the grid standards with very reduced power loss, in fact they operate at the fundamental frequency and are designed to control the amplitude of the desired harmonics. The fundamental component is determined through the first equation, while the remaining equations are used to either set the amplitude

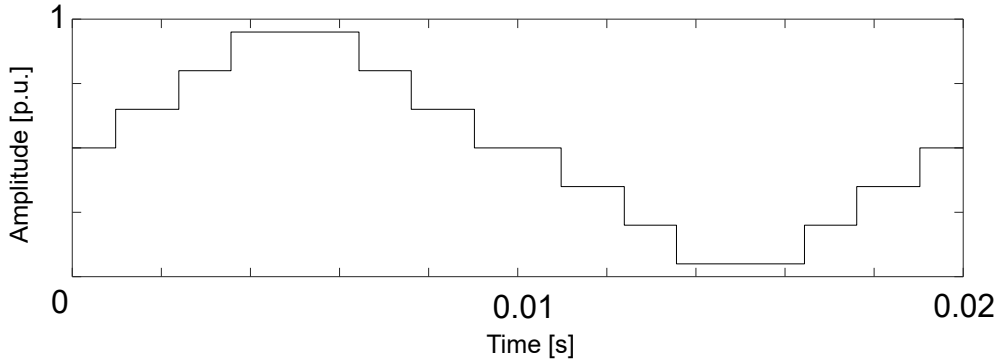


Figure 2.6: SHE/SHM-based CHB output voltage.

of undesired harmonics to zero (in the case of SHE) or minimize the overall harmonic content (in the case of SHM). Consequently, a system of equations is established, with each equation depending on the switching angles (α_i), which are the unknown values to be solved. The output voltage and current quality highly depend on the number of switching angles that are considered in the calculation of a preprogrammed switching pattern. The switching angles set should be obtained offline and the computational cost depends on the number of considered switching angles (i.e., on the number of harmonics to be eliminated/mitigated). The SHE/SHM methods are stiff since the preprogrammed solution should be updated each fundamental period. A typical SHE/SHM-based CHB output voltage waveform is shown in Fig. 2.6.

2.2.3 Output current control techniques

Ensuring the stable and efficient operation of the CHB converter requires precise regulation of the phase current, which is therefore treated as a primary control objective. By accurately following the current reference signal in both steady-state and transient regimes, it contributes to minimize phase and amplitude deviations, thus improving the converter's performance and efficiency.

Current control strategies in power electronics are generally divided into two main categories: nonlinear and linear methods. Among these, linear techniques are

the most commonly employed across industrial applications and academic research, mainly due to their well-understood behavior and implementation simplicity. These methods regulate the switching signals, typically generated by a modulation strategy, and include controllers based on Proportional-Integral (PI) and Proportional-Resonant (PR) schemes. While PI controllers operate in the synchronous reference frame d-q, PR controllers are designed for the rotary coordinates α-β [23]. Although linear control approaches are attractive due to their reduced implementation complexity, they often exhibit limitations in dynamic performance, particularly when dealing with nonlinear system behaviors. For this reason, nonlinear control methods have been introduced to enhance the system's response and stability under varying operating conditions. These techniques include, among others, Model Predictive Control (MPC), fuzzy logic, state feedback, and hysteresis control. Many of the control solutions developed for conventional two-level converter systems are applicable to multilevel topologies, such as the CHB. In particular, this chapter focuses on the regulation of the phase currents in a three-phase grid-connected CHB configuration. Therefore, the control strategy adopted here employs a PR controller, which is particularly well suited for the objectives of this work.

a. Proportional resonant controller

While PI controllers are prevalent in industrial applications, they are inherently unsuitable for the direct control of sinusoidal signals. Since this chapter focuses on the control of a three-phase CHB, a PR controller operating in the stationary α-β reference frame is implemented. This approach not only addresses the challenges of three-phase control but also provides a unified framework adaptable to both single-phase and three-phase CHB topologies. Several approaches have been proposed in the literature for regulating phase voltage and current using resonant controllers [24, 25]. These studies extend the ideal transfer function of the resonant

regulator by incorporating the crossover frequency ω_c and a phase compensation term δ. As a result, three distinct forms of the resonant regulator can be defined: the ideal version, the real version, and the phase compensation (trigonometric) version.

1. Ideal PR controller The ideal resonant controller possesses a single degree of freedom, and its tuning is based on the gain parameter k_i. This controller is theoretically designed to provide infinite gain at the target frequency, which, in the context of output current control, corresponds to the fundamental angular frequency ω_o. Despite the straightforward implementation, the ideal resonant controller exhibits slow transient behavior and is highly susceptible to noise disturbances. The mathematical formulation of its transfer function is presented in (2.4), while Fig. 2.7 illustrates the corresponding Bode plot, highlighting the frequency response characteristics of the ideal PR controller.

$$G_{r_{Ideal}}(s) = \frac{k_i s}{s^2 + \omega_o^2} \tag{2.4}$$

2. Real PR controller To enable the practical implementation of a digital PR controller, it is common to introduce an additional parameter into the transfer function defined in (2.7). This parameter, known as the crossover frequency ω_c, corresponds to the frequency at which the open-loop system's Bode magnitude plot intersects the 0 dB line (i.e., unit gain). The crossover frequency plays a fundamental role in evaluating both the stability and dynamic characteristics of the control system. From a control perspective, ω_c is directly associated with the system's bandwidth, which is defined as the frequency range within which the closed-loop response remains within 3 dB of its steady-state value. As such, it also serves as a quantitative indicator of the system's responsiveness. Introducing ω_c into the transfer function effectively mitigates the infinite gain produced by the ideal PR controller at the resonant frequency, thus yielding a more selective and damped frequency response.

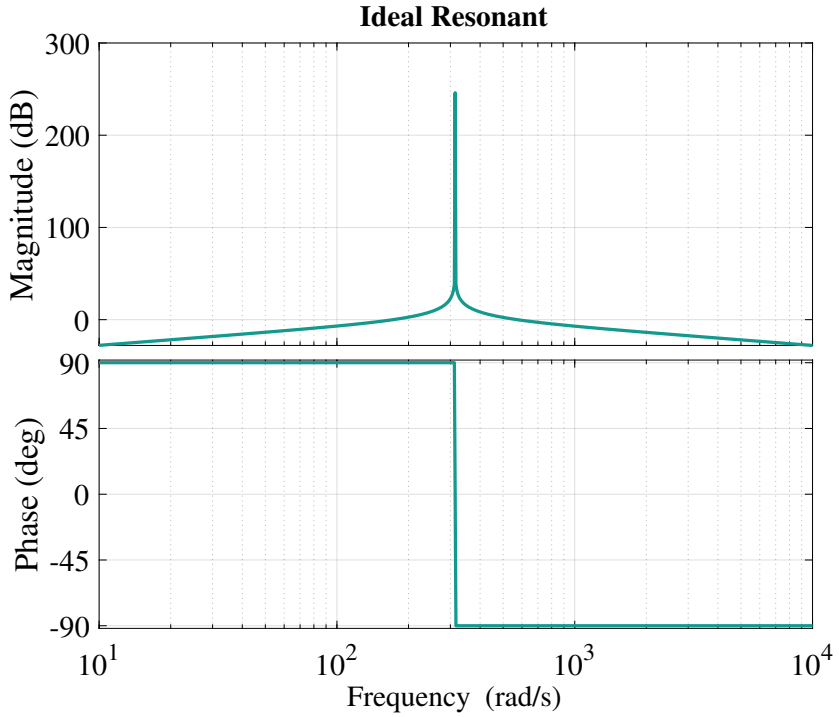


Figure 2.7: Bode diagram of ideal PR controller.

This adjustment not only reduces the computational burden required to implement the control law, but also enhances robustness by decreasing the controller's sensitivity to high-frequency noise. However, in certain scenarios, this trade-off may lead to a noticeable tracking error. The modified transfer function, which reflects these improvements, results in what is referred to as the real PR controller, as shown in (2.5). The frequency response of this version is depicted in the Bode diagram shown in Fig. 2.8.

$$G_{r_{Real}}(s) = 2k_i\omega_c \frac{s + \omega_c}{s^2 + 2\omega_c s + \omega_o^2} \tag{2.5}$$

3. Real PR controller with phase compensation (trigonometric) In recent developments, the trigonometric resonant controller, also known as the phase - compensated PR regulator [25, 26], has gained considerable attention. This advanced variant of the PR controller is specifically designed to offer three independent de-

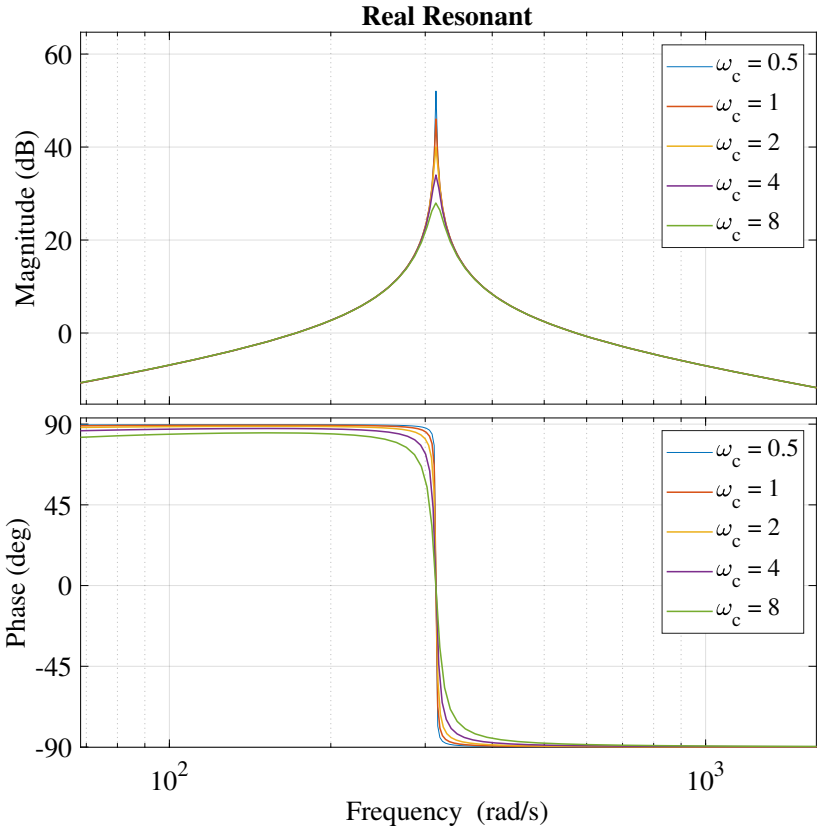


Figure 2.8: Bode diagram of real PR controller response by varying crossover frequency ω_c.

grees of freedom, enabling separate tuning of the gain k_i, the crossover frequency ω_c, and the phase compensation angle δ. The formulation of this controller, presented in (2.6), is particularly well suited for grid-connected systems where the power supply may exhibit significant distortion or where the connected loads are highly sensitive to voltage fluctuations. Due to its enhanced flexibility and robustness, the trigonometric PR regulator is often preferred in such demanding operating conditions. The Bode diagram illustrating the frequency response of this controller is provided in Fig. 2.9.

$$G_{r_{Real}}(s) = 2k_i\omega_c \frac{s\cos\delta + \omega_c - \omega_o \sin\delta}{s^2 + 2\omega_c s + \omega_o^2} \tag{2.6}$$

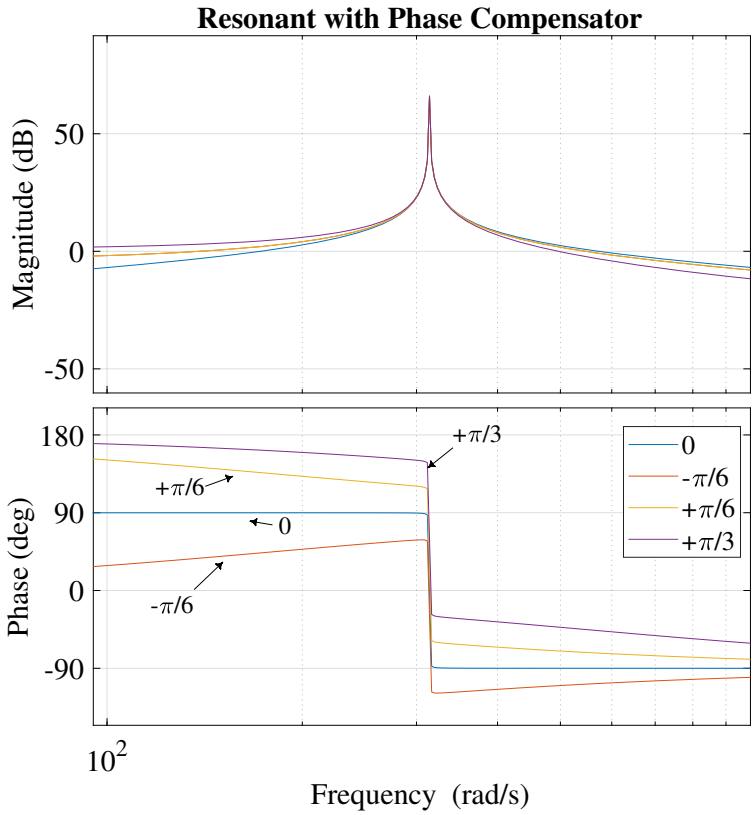


Figure 2.9: Bode diagram of PR trigonometric controller response by varying phase angle δ.

b. Discrete PR controller

In this chapter, output current regulation is achieved through a PR controller incorporating phase compensation. By setting the phase angle $\delta = 0$, the controller structure simplifies to the real PR version, characterized by two degrees of freedom. To enable practical implementation on digital platforms such as microcontrollers or FPGAs, it is necessary to convert the continuous-time transfer function presented in (2.9) into its discrete-time counterpart. Among the various discretization techniques available, this work adopts the Tustin (bilinear) transformation method [27].

The design of a discrete controller assumes that its behavior approximates that of an equivalent continuous-time controller, particularly in terms of preserving the key features of the frequency response, most notably, the crossover frequency ω_c. The Tustin transformation ensures a one-to-one mapping between the stability re-

gions of the continuous and discrete domains. However, this mapping comes at the cost of compressing the entire continuous frequency spectrum into the finite range $[0, \pi]$ in the discrete domain. As a result, the non-linear nature of the transformation introduces discrepancies in the correspondence between the continuous and discrete resonance frequencies and phase characteristics. To mitigate this issue, a pre-warping technique is applied around the target resonant frequency, ensuring more accurate frequency-domain matching. In the following, the step-by-step procedure for applying the Tustin method with pre-warping to discretize the PR controller is described.

Given:

$$s = \frac{2(z-1)}{T(z+1)} \tag{2.7}$$

where T denotes the sampling period of the control system, and given the pre-warping frequency, defined according to the resonant frequency ω_o:

$$\omega_{pw} = \frac{2}{T} tan(\frac{\omega_o T}{2}) \tag{2.8}$$

the modified Tustin transform with pre-warping frequency becomes:

$$s = \frac{\omega_o}{\omega_{pw}} \frac{2(z-1)}{T(z+1)} = \frac{\omega_o}{tan(\frac{\omega_o T}{2})} \frac{z-1}{z+1} \tag{2.9}$$

After selecting the desired discretization method, the next step involves formulating the general discrete-time transfer function as follows:

$$G_r(z) = \frac{k_1 + k_2 z^{-1} + k_3 z^{-2}}{1 + y_1 z^{-1} + y_2 z^{-2}}. \tag{2.10}$$

Following the discretization of (2.9) through the substitution defined in (2.9), a new parameter $k_T = \frac{\omega_o}{\tan\left(\frac{\omega_o T}{2}\right)}$ is introduced to simplify the resulting expressions. With this definition, Equation (2.10) can be rewritten as:

$$G_r(z) = \frac{2k_i\omega_c\left(k_T\frac{(z-1)}{(z+1)}\cos\delta + \omega_c - \omega_o\sin\delta\right)}{\left(k_T\frac{(z-1)}{(z+1)}\right)^2 + 2\omega_c\left(k_T\frac{(z-1)}{(z+1)}\right) + \omega_o^2} \tag{2.11}$$

which can be simplified by distinguishing the numerator $Num(z)$ and the denominator $Den(z)$:

$$Num(z) = z^2a_1 + za_2 + a_3 \tag{2.12}$$

$$Den(z) = z^2b_1 + zb_2 + b_3 \tag{2.13}$$

where:

$$\begin{aligned}
a_1 &= 2k_i\omega_c k_T\cos\delta + 2k_i\omega_c^2 - 2k_i\omega_c\omega_o\sin\delta \\
a_2 &= 4k_i\omega_c^2 - 4k_i\omega_c\omega_o\sin\delta \\
a_3 &= 2k_i\omega_c^2 - 2k_i\omega_c\omega_o\sin\delta - 2k_i\omega_c k_T\cos\delta \\
b_1 &= k_T^2 + 2\omega_c k_T + \omega_c^2 + \omega_o^2 \\
b_2 &= 2\omega_c^2 - 2k_T^2 + 2\omega_o^2 \\
b_3 &= k_T^2 - 2\omega_c k_T + \omega_c^2 + \omega_o^2
\end{aligned} \tag{2.14}$$

Having now derived the expressions for both the numerator and the denominator, the coefficients k_1, k_2, k_3, y_1, and y_2 can be determined as follows:

$$\begin{aligned}
k_1 &= \frac{a_1}{b_1} \\
k_2 &= \frac{a_2}{b_1} \\
k_3 &= \frac{a_3}{b_1} \\
y_1 &= \frac{b_2}{b_1} \\
y_2 &= \frac{b_3}{b_1}
\end{aligned} \tag{2.15}$$

The detailed expressions for the five controller parameters are presented in (2.16). The numerical values provided in this section correspond precisely to those used in the implementation of the non-ideal PR controller.

$$
\begin{aligned}
k_1 &= \frac{2k_i\omega_c k_T \cos\delta + 2k_i\omega_c^2 - 2k_i\omega_c\omega_0 \sin\delta}{k_T^2 - 2\omega_c k_T + \omega_c^2 + \omega_0^2} \\
k_2 &= \frac{4k_i\omega_c^2 - 4k_i\omega_c\omega_0 \sin\delta}{k_T^2 - 2\omega_c k_T + \omega_c^2 + \omega_0^2} \\
k_3 &= \frac{2k_i\omega_c^2 - 2k_i\omega_c\omega_0 \sin\delta - 2k_i\omega_c k_T \cos\delta}{k_T^2 - 2\omega_c k_T + \omega_c^2 + \omega_0^2} \\
y_1 &= \frac{2\omega_c^2 - 2k_T^2 + 2\omega_0^2}{k_T^2 - 2\omega_c k_T + \omega_c^2 + \omega_0^2} \\
y_2 &= \frac{k_T^2 + 2\omega_c k_T + \omega_c^2 + \omega_0^2}{k_T^2 - 2\omega_c k_T + \omega_c^2 + \omega_0^2}
\end{aligned}
\tag{2.16}
$$

2.3 Implementation and testing of a control strategy on a grid-connected three-phase CHB converter

The controller developed in the previous section has been employed to regulate the three-phase output currents of a grid-connected CHB converter. The primary objective is to ensure that the CHB injects currents into the grid that are in phase with the corresponding grid voltages and have an amplitude consistent with the desired level of active power injection. This control strategy has been implemented on the experimental setup of a three-phase, three-cell CHB converter, which has been entirely designed, developed, and tested as part of the PhD research activities.

2.3.1 Experimental setup

This paragraph describes the experimental setup developed, assembled, and tested entirely during the PhD research activity, and used for the validation of the CHB current control. The setup is located at the Power Electronics Laboratory of the Polytechnic University of Bari and consists of a scaled prototype of a three-phase CHB converter connected to the grid. The experimental tests have been conducted using three cells, each with a voltage of 120 V.

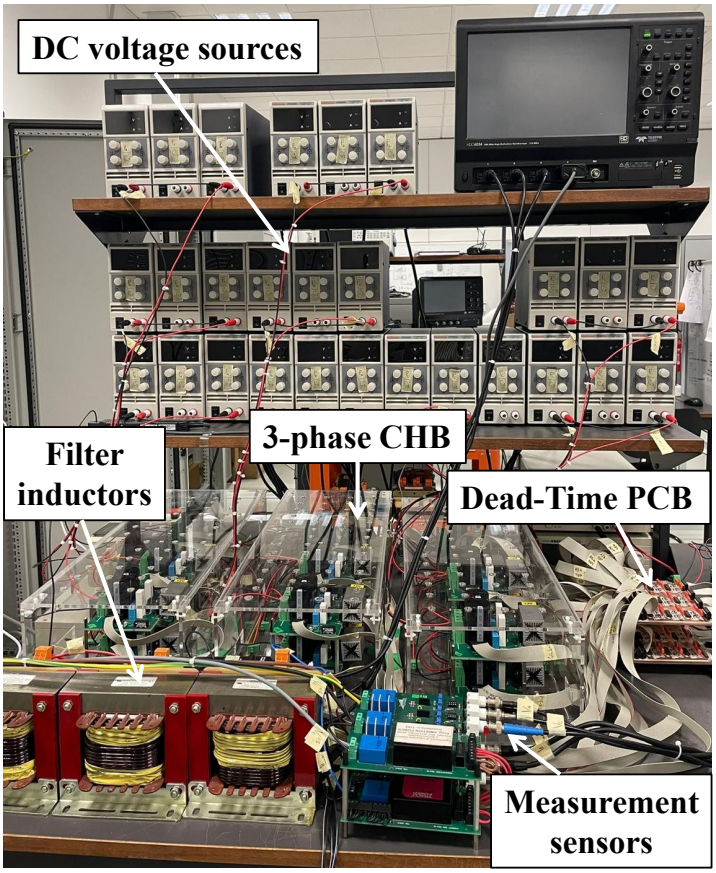


Figure 2.10: Picture of the experimental setup of the CHB.

Fig. 2.10 shows the complete test bench, which includes the three-phase grid-connected CHB inverter, three filter inductors, a dead-time generation PCB, and a set of voltage and current sensors. The design, implementation, and control of this grid-connected CHB converter prototype have constituted a core part of the experimental research carried out throughout the PhD program.

The converter consists of three series-connected cells per phase, specifically designed for this application. Each submodule features a DC-link capacitor of 1000 μF. The complete set of parameters used during testing is summarized in Table 2.2, while the internal structure of a single leg constituting a CHB cell is illustrated in Fig. 2.11.

The PWM modulation and control algorithms are implemented on the PED-Board (Power Electronics and Drives-Board), a control platform equipped with a

Table 2.2: Setup parameters

Parameter	Symbol	Value
Number of cells per phase	N	3
DC Voltage	V_{DC} [V]	120
Cell capacitor	C [μ]	1000
Filter inductance	L [mH]	6
Switching frequency	f_c [kHz]	1
Fundamental frequency	f_o [Hz]	50

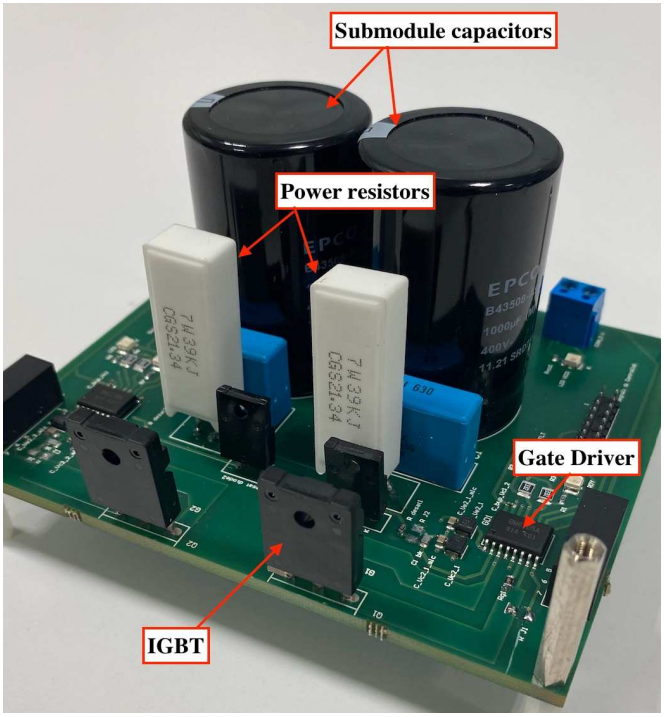


Figure 2.11: Single leg of a CHB cell.

Field Programmable Gate Array (FPGA). The FPGA is programmed using National Instruments' LabVIEW FPGA environment, which allows for the development of control logic through an intuitive block diagram interface, offering a more accessible alternative to traditional VHDL-based programming. To enable the driving of all submodules in the CHB, a custom dead-time generation board with a fixed delay of 1 μs has been developed in the Power Electronics Laboratory at the Polytechnic University of Bari, as illustrated in Fig. 2.12. This additional board is necessary due to the limited number of PWM outputs available on the main control board, which are insufficient to directly manage all the submodules. The dead-time board

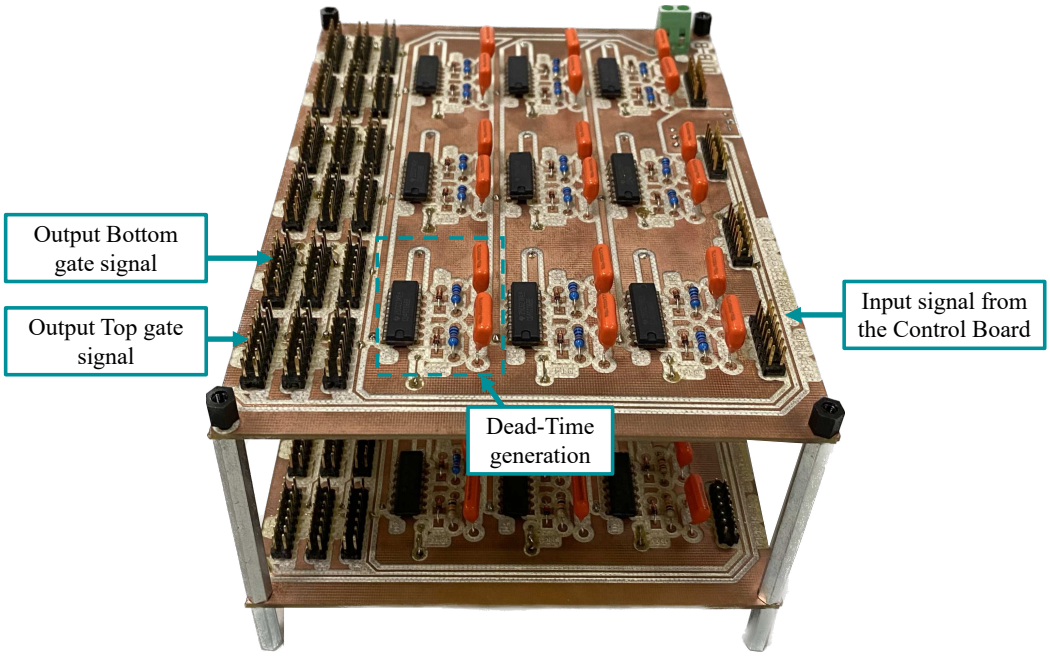


Figure 2.12: Dead-Time generation board.

acquires the control signals of the upper switches of each submodule, generating the complementary signals for the lower switches, and inserting the required dead time via an analog circuit based on integrator stages. This approach allows the control board to generate signals only for the upper switches of each cell, effectively reducing by half the number of gate signals that need to be generate.

Fig. 2.13 shows the measurement board used for acquiring voltage and current waveforms. This board is primarily responsible for conditioning the analog signals so it falls within the acceptable input ranges of the ADCs, typically spanning either (–5 V to +5 V) or (0 V to +5 V). For signal acquisition, LEM transducers have been selected in place of the optocouplers commonly used in similar applications. This decision is mainly justified by the superior linearity performance of LEM sensors, which is maintained for both alternating (AC) and direct (DC) currents. Two specific models have been chosen for the experimental setup: the LV 25-P SP5, used for high-voltage measurements, and the LA 25-NP, suited for current measurements. The selection of these components ensures accurate signal acquisition and reliable

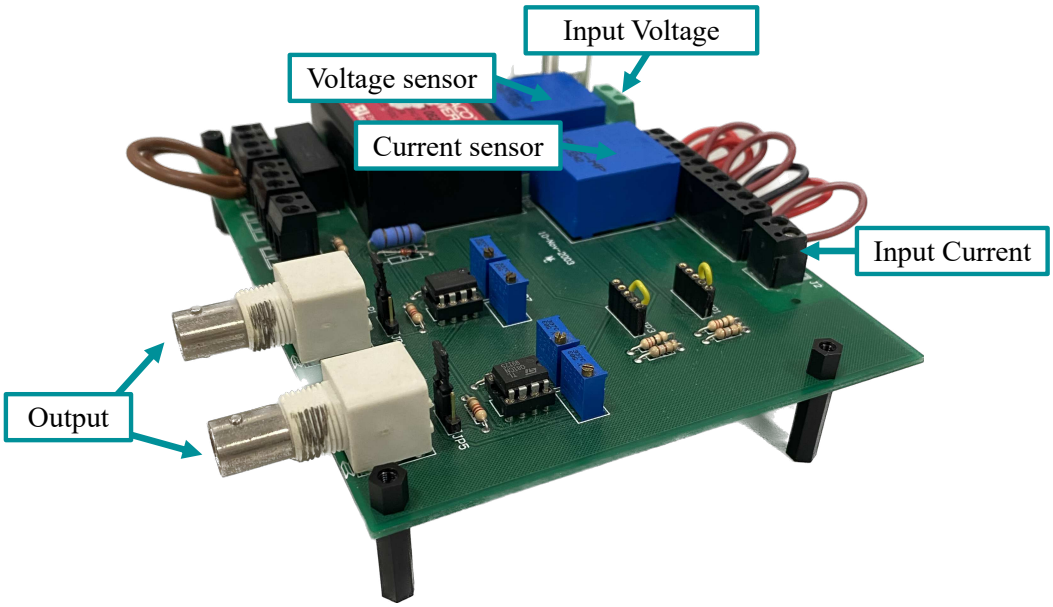


Figure 2.13: Voltage and current measurement board.

adaptation to the voltage and current levels typical of three-phase power conversion systems.

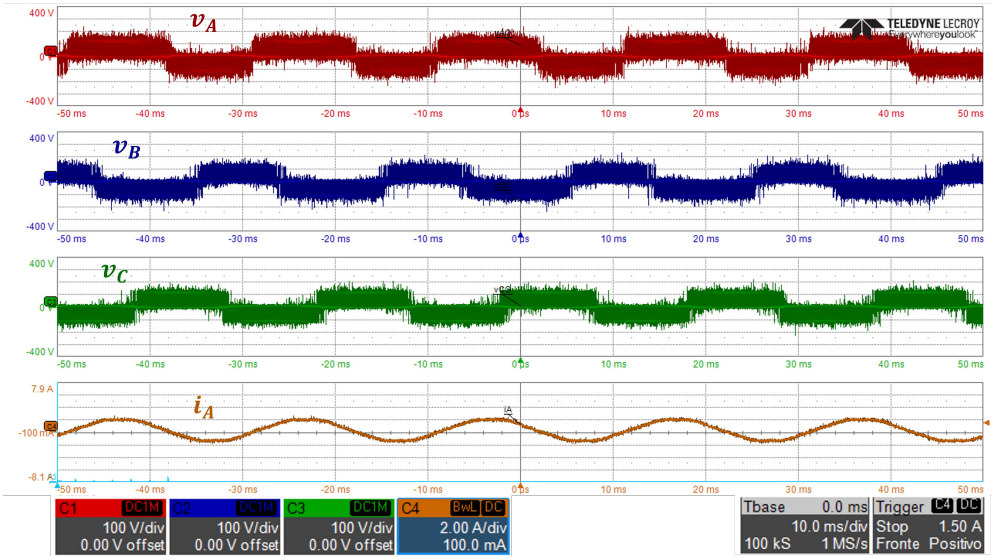
2.3.2 Implemented control strategy

As previously discussed, the main objective of this chapter is to implement a control strategy capable of ensuring synchronization with the main grid while regulating the active power injection through a current control loop. The adopted control system is based on a PR regulator, which, as highlighted in the previous paragraph, is particularly well-suited for grid-connected applications operating in the stationary α-β reference frame. The system relies on the measurement of both phase currents and grid voltages using dedicated sensors. The measured phase currents are transformed into the α-β frame to be regulated by the PR controllers. Simultaneously, the grid voltages are processed by a Phase-Locked Loop (PLL) algorithm, which extracts the instantaneous phase angle of the grid. The PLL operates by transforming the measured three-phase grid voltages into the *dq* rotating reference frame aligned

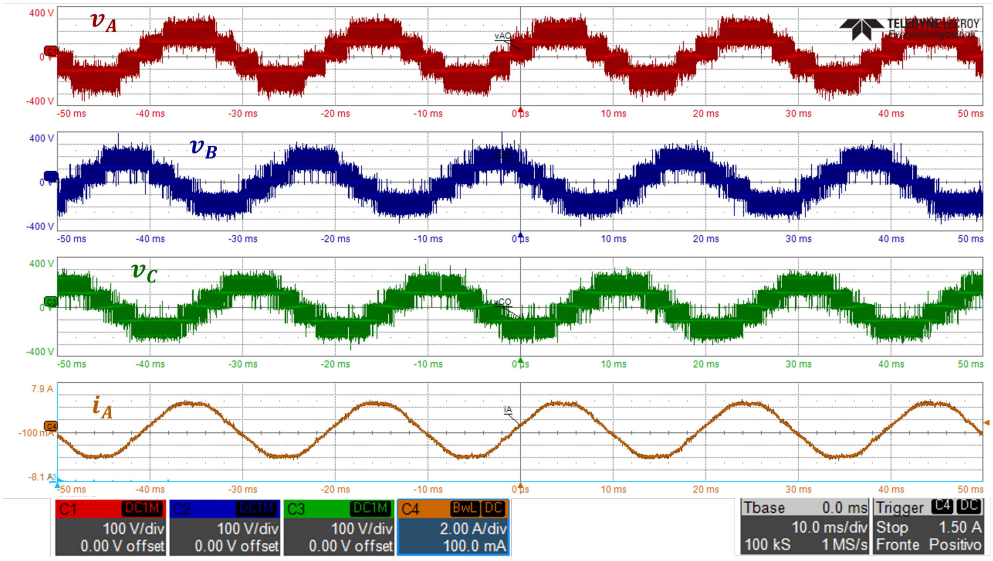
with the estimated grid voltage vector. The q-axis component of the voltage is then regulated to zero through a PI controller, ensuring that the d-axis remains aligned with the grid voltage vector. The output of the PI controller corresponds to the estimated grid angular frequency, which is integrated to obtain the instantaneous phase angle. This information is then used to generate current references that are perfectly in phase with the grid voltages, enabling the injection of purely active power into the grid. Regarding the modulation technique, a conventional PS-PWM scheme has been applied to the three-phase CHB converter. This method involves comparing the appropriately phase-shifted carrier signals ($0°, 60°, 120°$) with the sinusoidal modulation signals generated by the designed control system in order to obtain the desired current amplitude.

2.3.3 Test of the 3-phase CHB setup

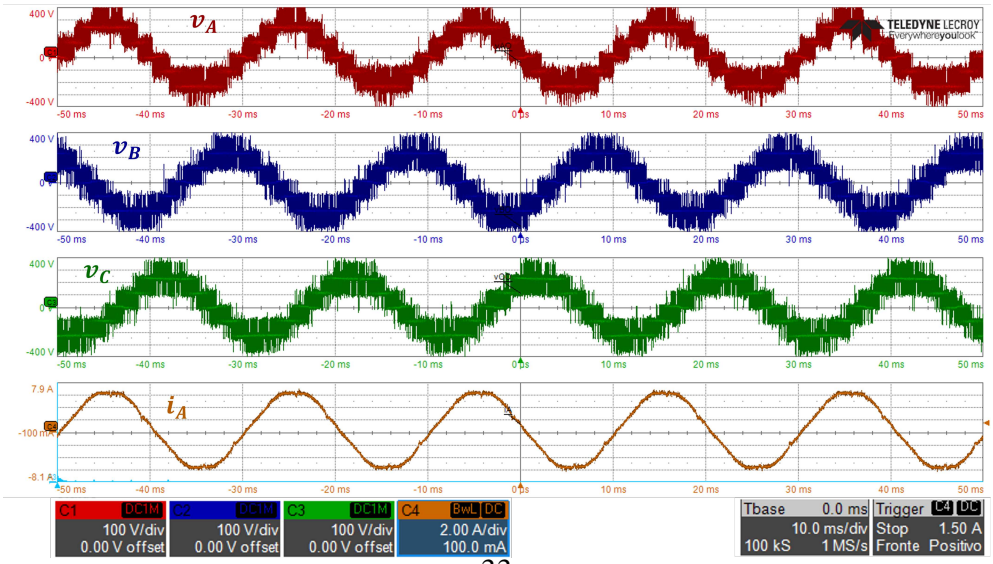
This paragraph presents the experimental results obtained to validate the operation of the grid-connected CHB inverter. Output current control has been implemented using PR regulators, along with a PLL to ensure synchronization with the main grid. This configuration enables the injection of active power only. In particular, the amplitude of the current reference has been gradually raised, and the corresponding results are presented in Fig. 2.14. This figure illustrates the three-phase output voltages and the phase A current for current reference amplitudes of 2 A (Fig. 2.14a), 4 A (Fig. 2.14b), and 6 A (Fig. 2.14c). In all cases, the measured current closely matches the reference amplitude, validating the effectiveness of the current control strategy. Furthermore, an increase in the number of voltage levels can be observed as the current amplitude increases. This behavior is attributed to the corresponding rise in the modulation index generated by the controller, which results in finer voltage steps. As expected, for high modulation index, seven voltage levels ($2N + 1$) are observed, corresponding to the series connection of 3 cells per phase.



(a)



(b)



(c)

Figure 2.14: Three-phase CHB output voltage waveforms and phase A current for current reference values of (a) 2 A, (b) 4 A, and (c) 6 A.

Chapter 3

Modulation Techniques for Cascaded H-Bridge Under Grid Voltage Disturbances

In grid-connected applications, the injected current into the power grid must meet the minimum requirements outlined in the relevant grid codes and standards [28]. This is particularly important when the grid itself exhibits undesired distortions, which are often observed, especially in low-order harmonics. If no corrective action is taken, these grid-induced distortions will be present in the current injected by the converter [29]. To ensure compliance with power quality standards, it is crucial to address this issue during the design of control and modulation techniques for grid-tied converters connected to the point of common coupling (PCC).

Fig. 3.1 provides a mathematical representation of this phenomenon. As an example, Fig. 3.2 illustrates an undesirable third-harmonic distortion in the power grid, represented in blue. However, by appropriately adjusting the voltage generated by the power converter, it is possible to compensate for this harmonic distortion, as shown in red in the same figure. This process highlights the importance of effective modulation and control strategies to maintain grid stability and adhere to power

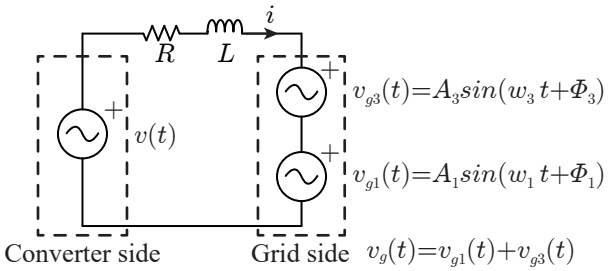


Figure 3.1: Equivalent circuit of the single-phase CHB connected to a grid with a non-negligible third-harmonic distortion.

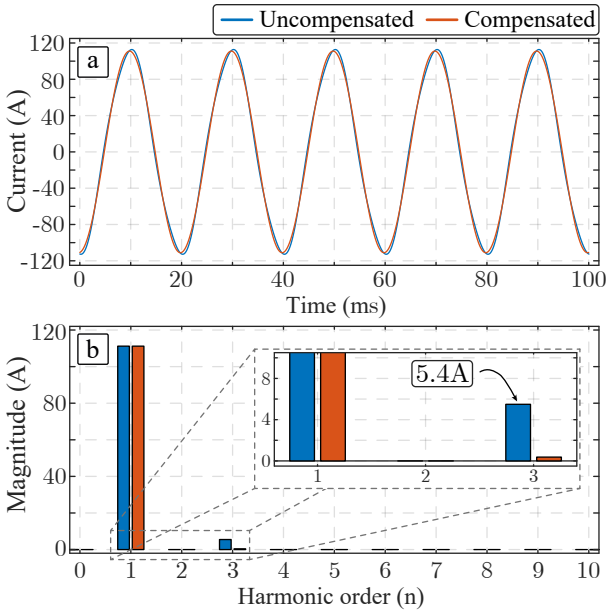


Figure 3.2: (a) Injected currents in the presence of grid voltage disturbance. (b) Harmonic spectra.

quality standards.

This chapter introduces two innovative strategies for mitigating grid disturbances using a CHB converter while concurrently minimizing switching losses. The first approach employs a hybrid modulation technique that integrates block switching (BS) with a unipolar PWM scheme. The second method operates the CHB converter at a low-frequency PWM mode, adjusting the phase shift of the carriers to meet specific harmonic performance criteria. These techniques are implemented on a single-phase, three-cell CHB topology, as illustrated in Fig. 3.3. Before presenting the proposed methods, a comprehensive harmonic analysis of the CHB output

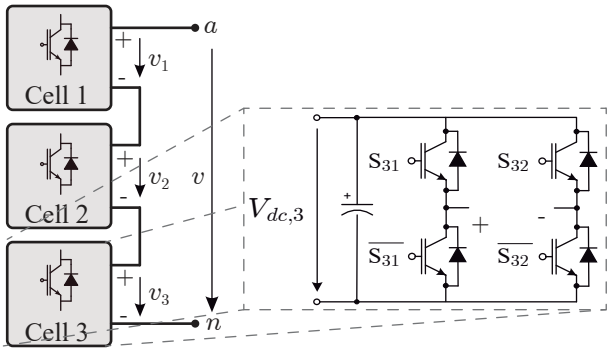


Figure 3.3: Three-cell single-phase multilevel CHB converter.

waveforms is conducted, including a discussion on variable phase-shift modulation techniques and their impact on waveform quality.

3.1 Mathematical description of the output voltage of the CHB converter

The CHB converter is typically operated using the PS-PWM technique due to its advantageous features, as discussed in the previous chapter [30]- [31]. In this modulation scheme, each power cell employs a unipolar PWM strategy, wherein each leg of the CHB converter is modulated using a reference signal and another reference signal phase-shifted by 180°, both utilizing a single carrier signal. In a CHB converter operating with the PS-PWM method, a phase displacement must be applied between the carriers of adjacent power cells, as defined in 2.3 [18]. The advantages of PS-PWM in CHB converters are well established, primarily due to its inherent ability to equalize power distribution among the cells [32]. This natural balancing effect results in uniform power losses and junction temperatures across the power devices of the different cells, enhancing the overall reliability and efficiency of the system.

Furthermore, the PS-PWM method significantly increases the effective switching frequency of the CHB output voltage. By introducing a phase shift between

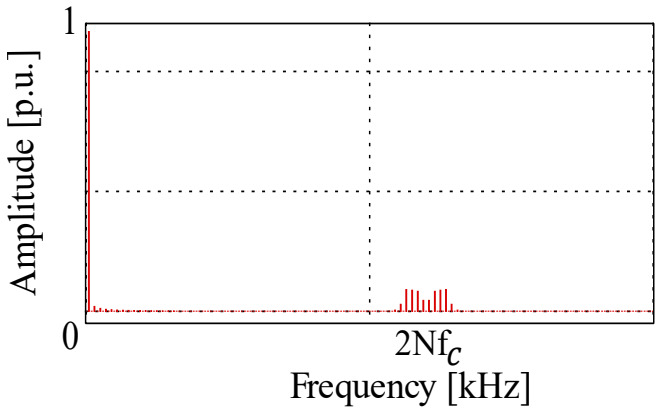


Figure 3.4: Generic harmonic spectrum of CHB output voltage.

the carriers of different cells, a multiplicative switching effect is achieved. Consequently, when the H-bridges operate with unipolar PWM at a switching frequency of f_c, the lowest-order harmonic distortion in the CHB output voltage appears at $2Nf_c$, where N is the number of cascaded cells, as shown in Fig. 3.4. The phasor representation of the voltage harmonic component at the x-th cell output, using a unipolar PWM technique, is expressed analytically as follows [18]:

$$H_x = A_x \frac{4\cos\left[(m+n-1)\pi\right]}{2m\pi} \tag{3.1}$$

where A_x is given by:

$$\begin{aligned} A_x &= V_{DC,x} J_{2n-1}\left(m\pi M_x\right) e^{j(2m\phi_x)} \\ &= V_{DC,x} J_{2n-1}\left(m\pi M_x\right) \left[\cos(2m\phi_x) + j\sin(2m\phi_x)\right] \end{aligned} \tag{3.2}$$

Here, J_{2n-1} denotes the Bessel function of the first kind of order $2n-1$. Additionally, $V_{DC,x}$ represents the DC voltage, and M_x is the modulation index of the x-th cell. The indices m and n uniquely identify each harmonic component; specifically, m corresponds to the carrier harmonic index, while n refers to the sideband harmonic index. ϕ_x represents the phase displacement (in radians) of the x-th cell

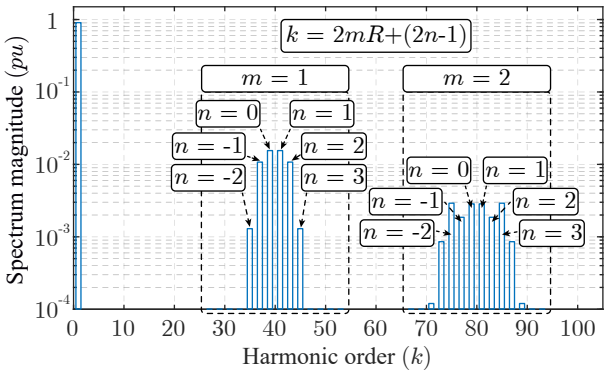


Figure 3.5: Harmonic spectrum of an H-bridge output voltage operated with unipolar PWM with R=20.

carrier with respect to the phase angle of the first cell carrier. The harmonic order k is defined as:

$$k = 2mR + (2n - 1) \tag{3.3}$$

where R is the ratio of the carrier signal frequency to the modulating signal frequency. These parameters are shown in Fig. 3.5 considering R=20, where the harmonic spectrum of a single H-bridge cell voltage is represented; it can be seen that m represents each harmonic group and n represents each harmonic inside each harmonic group.

For a CHB converter with N cells, the analytical expression for the phasor corresponding to the k-th harmonic component of the output voltage can be obtained by summing the contributions from all cells, as given below:

$$H_x = \frac{4\cos\left[(m+n-1)\pi\right]}{2m\pi} \sum_{x=1}^{N} A_x. \tag{3.4}$$

To eliminate a specific k-th harmonic, the corresponding phasor H_x must be set to

zero, i.e.:

$$\begin{aligned}\sum_{x=1}^{N} V_{DC,x} J_{2n-1}\left(m\pi M_x\right)\cos(2m\phi_x) = 0 \\ \sum_{x=1}^{N} V_{DC,x} J_{2n-1}\left(m\pi M_x\right)\sin(2m\phi_x) = 0.\end{aligned} \tag{3.5}$$

Under balanced operating conditions of the CHB, where the DC voltage and modulation indices are identical for each cell, the elimination of the generic H_k harmonic is achieved by satisfying the following conditions:

$$\begin{aligned}\sum_{x=1}^{N} \cos(2m\phi_x) = 0 \\ \sum_{x=1}^{N} \sin(2m\phi_x) = 0.\end{aligned} \tag{3.6}$$

When PS-PWM with conventional modulation angles is employed, all harmonic components for $m = 1, 2, \ldots, N-1$ are eliminated, demonstrating that the harmonic groups up to $m = N-1$ are fully suppressed. This result also provides a mathematical explanation for the multiplicative switching effect inherent in the PS-PWM method when applied to a CHB operating under balanced conditions.

3.2 Hybrid modulation technique

The proposed hybrid PWM technique for the three-cell CHB involves applying a fundamental frequency waveform to two power modules, while a conventional unipolar PWM technique is used for the third module [33]. The fundamental frequency operation in the power modules offers a promising solution for very high-power applications due to its inherently lower switching losses, although this comes at the cost of reduced output waveform quality. To address this limitation, the power module using the unipolar PWM technique helps improve the harmonic quality of

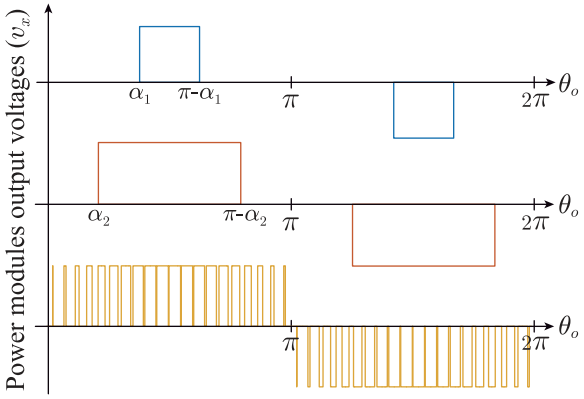


Figure 3.6: Power module output voltages applying the proposed hybrid PWM scheme for a three-cell CHB.

the output, ensuring it meets or exceeds the standards set by grid codes. In summary, the proposed hybrid PWM method, termed Hybrid H Cell-PWM (HHC-PWM), generates the output voltages of the power modules, as shown in Fig. 3.6. The HHC-PWM technique aims to reduce the switching losses of two power modules by generating fundamental frequency output waveforms for the power modules. However, it is well-established that the harmonic spectrum of such output waveforms typically contains several undesirable low-order harmonic components. To address this issue, the HHC-PWM method incorporates variable fundamental frequency power module output waveforms, which are determined by the corresponding switching angles (α_1 and α_2) of the power modules. These switching angles are utilized within the HHC-PWM method, following the established principles of SHE/SHM, where the angle values are selected to effectively control the harmonic distortion in the converter's output voltage [21]- [22].

First of all, it is useful to define the following value:

$$M = \frac{1}{3}\sum_{x=1}^{N=3} M_x \tag{3.7}$$

where M_x (x=1,2,3) is the modulation index of the power cell x. in addition, M_x is

defined as

$$M_x = \frac{H_{1,x}}{V_{DC,x}} \tag{3.8}$$

where $V_{DC,x}$ and $H_{1,x}$ are the DC voltage and the amplitude of the fundamental harmonic produced by the power cell x, respectively. This last equation is imposed because a symmetrical CHB converter is considered, therefore all power modules have the same DC voltage.

3.2.1 Operation of the blocking switching power cells

As previously stated, two of the three cells of the CHB converter are operated at fundamental frequency. The fundamental harmonic of the output voltage from the CHB converter is the sum of the fundamental components of the voltages generated by each individual power cell. To determine the amplitude of the harmonic components produced by the fundamental frequency power modules, the Fourier series can be applied with Fourier coefficients a_n and b_n (where b_n is zero by selecting the appropriate waveform symmetry). This approach allows for the calculation of the harmonic components of the sum of the output voltages from the fundamental frequency power modules, as follows:

$$H_n = \frac{a_n}{2V_{DC}} = \frac{4}{n\pi}[cos(n\alpha_1) + cos(n\alpha_2)] \tag{3.9}$$

Here, n denotes the harmonic order. From equation 3.9, the amplitudes of both the fundamental harmonic (H_1) and the third harmonic (H_3), can be expressed as:

$$H_1 = \frac{4}{\pi}[cos(\alpha_1) + cos(\alpha_2)] \tag{3.10}$$

$$H_3 = \frac{4}{3\pi}[cos(3\alpha_1) + cos(3\alpha_2)] \tag{3.11}$$

Given that there are two equations with two unknowns, a solution can be obtained by applying the appropriate constraints [21]. Specifically, the amplitude of the fundamental harmonic must be set to two-thirds of the required fundamental voltage (due to the operation of two cells in block switching mode), while the amplitude of the third harmonic is set to zero. This leads to the following set of equations:

$$\frac{2}{3}\frac{M\pi}{4} = [cos(\alpha_1) + cos(\alpha_2)] \tag{3.12}$$

$$0 = [cos(3\alpha_1) + cos(3\alpha_2)]. \tag{3.13}$$

After solving the system of equations with an appropriated symbolic mathematical solver tool, and after some mathematical manipulation, the analytical solution is given by:

$$\alpha_1 = 2\pi - arccos(\frac{\pi M'}{8} - \sigma) \tag{3.14}$$

$$\alpha_2 = 2\pi - arccos(\frac{\pi M'}{8} + \sigma) \tag{3.15}$$

where M' is the portion of the required fundamental voltage and σ is an auxiliary variable defined as:

$$\sigma = \frac{1}{24}(\sqrt{3}\sqrt{48} - M'^2\pi^2). \tag{3.16}$$

However, the analytical solution derived does not yield the necessary waveform symmetry required by the fundamental BS modulation technique. Moreover, the

mathematical expressions become increasingly complex, necessitating the reformulation of the system of equations as a multivariable optimization problem. The primary constraint in this optimization is to generate the desired portion of the fundamental harmonic component while ensuring zero third-harmonic injection. Generally, the cost function can be expressed as follows:

$$\tau = \frac{2H_1}{3} + \lambda_n H_n + \lambda A \tag{3.17}$$

where λ_n and λ are weighting factors, and the factor A considers the rest of the harmonic spectrum. A factor can be considered as the well-known figure of merit weighted total harmonic distortion (WTHD) or WTHD0, defined as follows:

$$WTHD = \frac{1}{H_1}\sqrt{\sum_{n=1}^{\infty}(\frac{H_n}{n})^2} \tag{3.18}$$

$$WTHD0 = \frac{1}{3V_{DC}}\sqrt{\sum_{n=2}^{\infty}(\frac{H_n}{n})^2} \tag{3.19}$$

because of the complexity in solving this optimization problem, the use of metaheuristic algorithms is very usual in power electronics [34]. For example, the genetic algorithm is inspired by the process of natural selection, which drives biological evolution [35]. Similarly, the particle swarm optimization algorithm is based on the social behavior of animals [36]. The exchange market algorithm (EMA), which combines both of these techniques, leverages the advantages of each, achieving an effective balance between computational complexity and convergence performance while avoiding local minima [37]. The EMA is inspired by share trading in the stock market and is the chosen method for harmonic optimization in this study. In terms of computational complexity, the algorithm requires a number of operations

per iteration that grows linearly with both the population size and the dimensionality of the optimization problem, in addition to the cost associated with evaluating the objective function. With respect to convergence, EMA exhibits strong global search capabilities due to its stochastic nature and its ability to balance exploration and exploitation; however, as with most metaheuristic approaches, convergence to the global optimum is not guaranteed and is typically probabilistic rather than deterministic. The implementation of EMA in real-time or high-power industrial contexts presents several challenges, including the need for fast and reliable objective function evaluations, careful tuning of algorithm parameters, and scalability to large-scale or high-dimensional problems. Nevertheless, EMA remains an attractive optimization strategy due to its conceptual simplicity, flexibility, and proven effectiveness across a wide range of complex nonlinear optimization problems. However, it is important to note that other metaheuristic methods could also be applied. The EMA, whose implementation is shown in Fig. 3.7, has been executed in order to minimize the cost function defined in 3.17 depending on the modulation index that has to be applied to the power cells and simultaneously forcing the required output voltage quarter symmetry in the power cells operated with BS modulation. The obtained results are represented in Fig. 3.8, where the values of the switching angles α_1 and α_2 and the corresponding values of WTHD and WTHD0 of the summation of the output voltages of the two BS cells are plotted as well.

3.2.2 Operation of the unipolar PWM cell

In the proposed HHC-PWM technique, one power cell of the CHB operates using a unipolar PWM strategy. The grid is assumed to be distorted, with distortion occurring at lower frequency orders, specifically considering a grid voltage that includes a third-harmonic component with defined magnitude and phase. From the analysis in Figs. 3.1 and 3.2, it can be observed that if the CHB output voltage consists solely

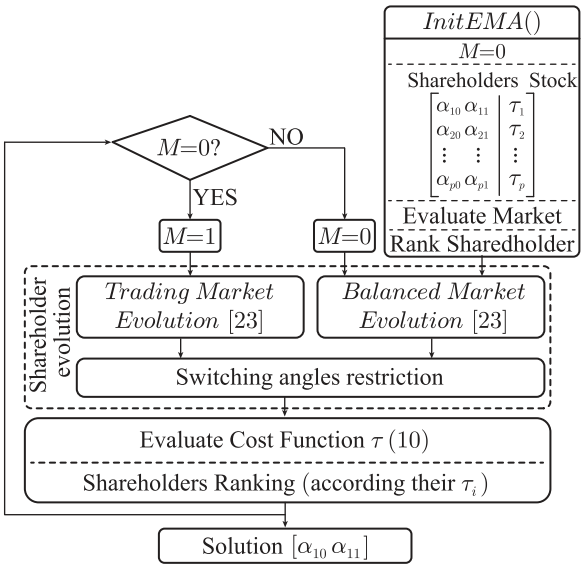


Figure 3.7: EMA implementation to determine the most proper switching angles in order to minimize the cost function τ.

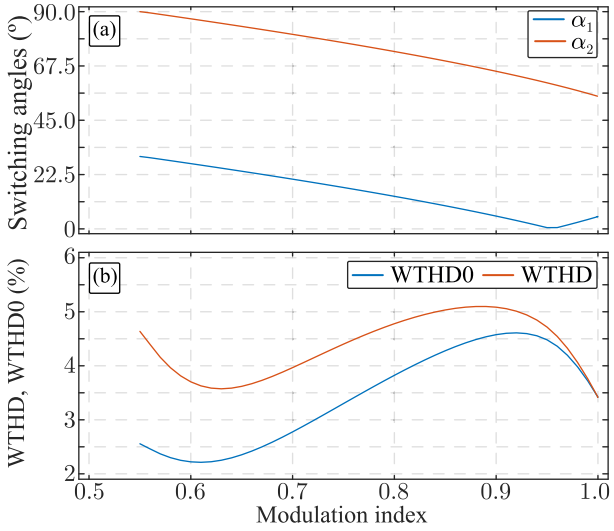


Figure 3.8: Results of the optimization cost function τ. (a) Optimal switching angles. (b) Resulting value of the figure of merit WTHD0 and WTHD.

of a fundamental harmonic, the resulting grid current will exhibit third-harmonic distortion. However, by measuring the magnitude of the third-harmonic component in the grid voltage and accounting for the grid filter to determine its phase, it becomes possible to generate grid currents that eliminate this third-harmonic distortion. This can be achieved by producing a CHB output voltage containing both

the fundamental harmonic and a third harmonic with the same magnitude as the grid's third-harmonic component. Furthermore, the third-harmonic component of the CHB output voltage must have the opposite phase to the third-harmonic component of the uncompensated grid current. This approach is clearly demonstrated in Fig. 3.2, which illustrates both the grid current with and without compensation applied to the CHB output voltage. The figure shows that high-quality grid currents can be achieved even in the presence of distorted grid voltages, by generating converter output voltages that counteract the distortion.

This concept is applied to the third power cell in the CHB, responsible for generating the remaining portion of the fundamental harmonic. Additionally, this power cell generates the necessary amplitude and phase for the third-harmonic component, thereby canceling out the unwanted harmonic content present in the grid. In this way, this power module is designed to handle:

$$\begin{aligned} H_1 &= MV_{DC} \\ H_3 &= H_{v_{g3}} \angle (H_{i_{g3}} + \pi) \end{aligned} \tag{3.20}$$

where $H_{v_{g3}}$ is the third-harmonic content of the grid voltage and $H_{i_{g3}}$ is the third-harmonic content of the grid current without applying any compensation.

3.2.3 Power loss analysis

An essential consideration in the design and operation of the converter is its efficiency, as well as the power losses that must be managed by the cooling system. In this context, the proposed modulation technique is evaluated in comparison to conventional state-of-the-art modulation methods, focusing on both the power loss generated and its effectiveness in injecting harmonics to mitigate disturbances.

1. Traditional BS-based SHE modulation techniques result in the lowest switching losses, as each power cell switches only once per fundamental period.

Table 3.1: Parameters used for loss calculation

Parameter	Symbol	Value
DC Voltage	$V_{DC,x}$ [V]	400
Capacitance	C [mF]	2
Resistance	R [Ω]	5
Inductance	L [mH]	4.16
PWM carrier frequency	f_c [kHz]	1

However, this approach imposes a significant limitation on the harmonic spectrum of the output voltage, reducing its ability to mitigate harmonic disturbances during converter operation.

2. In SHE/SHM modulation techniques, the generated power loss and the quality of the output voltage and current are influenced by the number of switching angles used in each power cell. By limiting the number of switching angles, it is possible to achieve acceptable output voltage quality while controlling power loss. However, SHE/SHM techniques are limited in their ability to effectively suppress harmonic disturbances.

3. PS-PWM offers superior controllability because the modulating reference for each power cell can be tailored to include the desired harmonic components. Unfortunately, PS-PWM also results in higher power losses, requiring the carrier frequency to be kept as low as possible to minimize these losses.

The proposed hybrid modulation technique provides a balanced solution by combining the low switching losses of the BS modulation with the capability to effectively mitigate harmonic disturbances over a wide operational range. Based on calculation parameters reported in Table 3.1, a quantitative switching power loss analysis for the presented techniques has been performed to demonstrate the previous dissertation, as shown in Fig. 3.9.

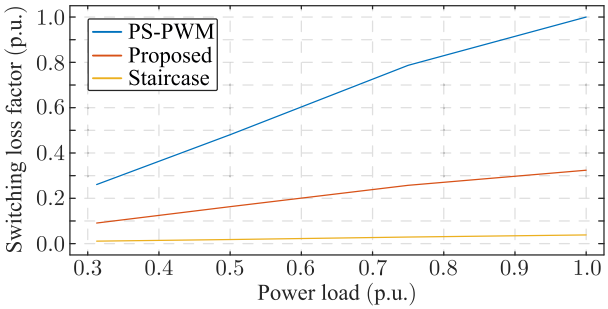


Figure 3.9: Switching loss evaluation for different power loads.

3.2.4 Power loss mismatch management

Another critical consideration in the power module operated with a unipolar PWM strategy is its power loss. In comparison to the two cells operating at the fundamental BS frequency, this power cell experiences significantly higher switching losses, resulting in a power loss imbalance across the CHB modules. This imbalance can negatively affect the converter's overall lifetime [38]. This issue can be addressed by implementing, for instance, a simple role rotation strategy [39]. Under this strategy, the role of each power module can be rotated after a set number of fundamental periods. Over time, each power module would operate with BS modulation for two-thirds of the time, while the remaining one-third would use the unipolar PWM strategy. This role rotation balances the power loss across the modules, ensuring an even distribution of aging. Alternatively, active thermal control could be employed, taking into account the accumulated conducting and switching losses, to determine the most suitable role for each power cell, thereby equalizing aging [38]. However, it should be noted that this approach is not the primary focus of the current study.

3.2.5 Experimental results

To evaluate the performance of the proposed technique, the experimental setup shown in Fig. 3.10 was utilized. The experimental rig consists of a single-phase CHB converter configured with three power cells, connected to a grid emulator.

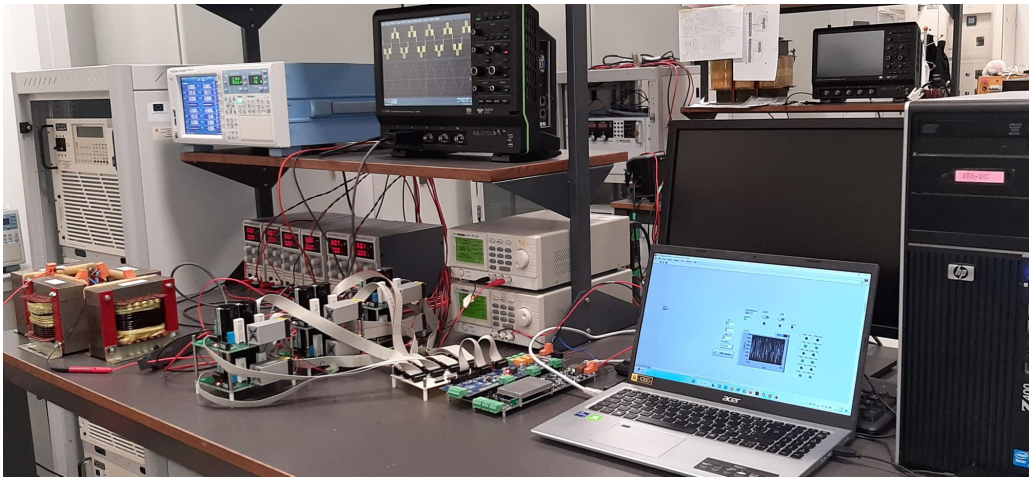


Figure 3.10: Down-scaled single-phase three-cell CHB prototype.

The key parameters of the experimental setup are summarized in Table 3.2. The experimental tests are organized into three distinct cases. In each of the reported scenarios, as detailed in Table 3.3, the power modules, operating at the fundamental switching frequency, are controlled to achieve two-thirds of the desired fundamental harmonic magnitude, with the third-harmonic component set to zero as a primary constraint. Additionally, the goal is to minimize the WTHD, as outlined in the cost function τ (3.17). The experimental results obtained from applying the proposed HHC-PWM strategy to the single-phase three-cell CHB converter, under the operational conditions specified in scenarios I, II, and III, are presented in Figs. 3.11-3.13, respectively. As demonstrated by these results, the CHB converter operates as expected, with the output voltage meeting the desired performance. Specifically, both the fundamental component and the third-harmonic injection (in terms of magnitude and phase) satisfy the prescribed requirements, effectively canceling the unwanted third-harmonic component in the output current.

To compare the proposed method with more conventional modulation techniques, additional experimental results were obtained under scenario I. Initially, a BS-based SHE modulation method was applied, yielding a CHB output voltage with the desired fundamental component. This method also eliminated the

Table 3.2: Experimental CHB setup parameters

Parameter	Symbol	Value
Power module DC Voltage	$V_{DC,x}$ [V]	120
Desired modulation index	M	0.9
Fundamental frequency	f_o [Hz]	50
PWM carrier frequency	f_c [kHz]	3

Table 3.3: Test scenarios

Scenario I		
Unipolar PWM magnitude injection	$[H_1, H_3]$ [V]	[108,12]
Unipolar PWM phase injection	$[P_1, P_3]$ [°]	[0,120]
Scenario II		
Unipolar PWM magnitude injection	$[H_1, H_3]$ [V]	[108,21]
Unipolar PWM phase injection	$[P_1, P_3]$ [°]	[0,130]
Scenario III		
Unipolar PWM magnitude injection	$[H_1, H_3]$ [V]	[108,21]
Unipolar PWM phase injection	$[P_1, P_3]$ [°]	[0,60]

fifth-harmonic component while imposing a target magnitude (12 V) for the third-harmonic component. The corresponding switching angles to achieve these objectives are $[\alpha_1, \alpha_2, \alpha_3] = [22.61°, 22.64°, 79.62°]$. The resulting output, shown in Fig. 3.14, reveals that a significant third-harmonic component remains in the output current due to an incorrect third-harmonic phase in the generated output voltage.

Additionally, a conventional PS-PWM method was applied, where each power module operates using a unipolar PWM technique with a carrier frequency of 3 kHz. In this setup, each power module generates one-third of the fundamental and desired third-harmonic components. The results, presented in Fig. 3.15, show that the third-harmonic component is successfully eliminated in the output current, as the third-harmonic component was specifically controlled in both magnitude and phase in the CHB output voltage. However, it is important to note the increase in switching losses in the CHB converter when using this method.

Thus, it can be emphasized that the proposed HHC-PWM method strikes an effective balance between harmonic suppression and efficiency, making it a highly promising solution for industrial applications where minimizing switching losses is

crucial.

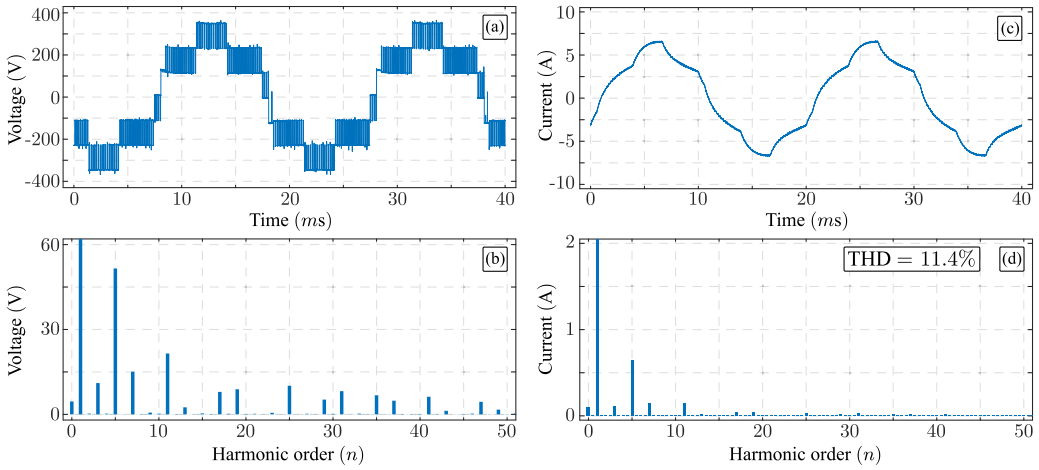


Figure 3.11: Experimental results for case I applying the HHC-PWM method. (a) CHB output voltage. (b) CHB output voltage harmonic spectrum. (c) Phase current. (d) Phase current harmonic spectrum.

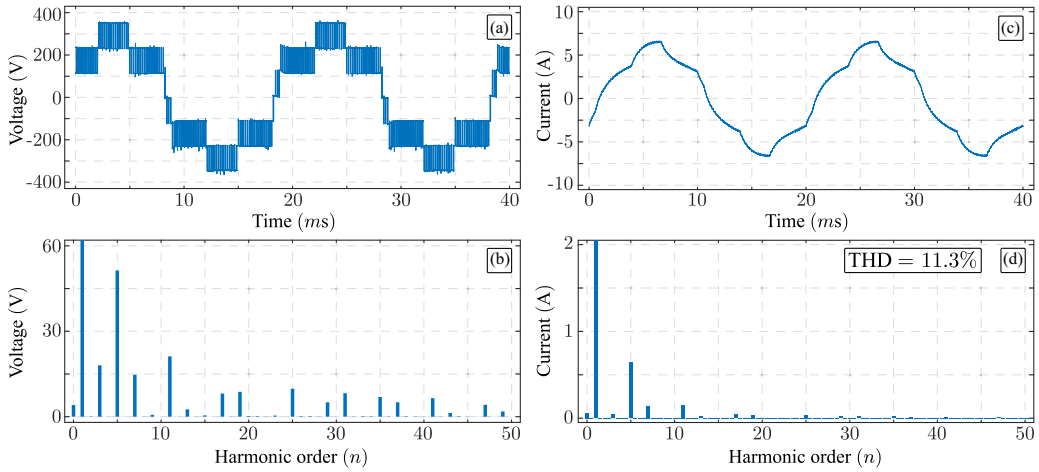


Figure 3.12: Experimental results for case II applying the HHC-PWM method. (a) CHB output voltage. (b) CHB output voltage harmonic spectrum. (c) Phase current. (d) Phase current harmonic spectrum.

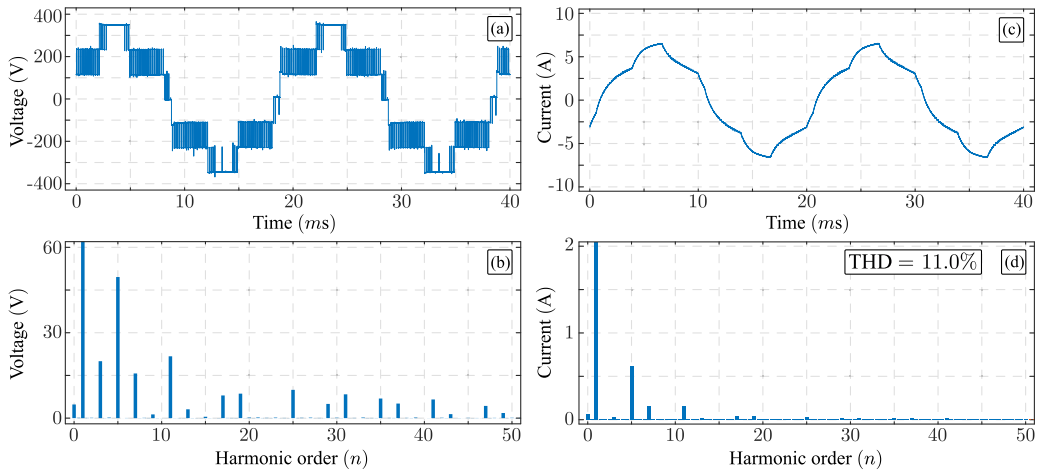


Figure 3.13: Experimental results for case III applying the HHC-PWM method. (a) CHB output voltage. (b) CHB output voltage harmonic spectrum. (c) Phase current. (d) Phase current harmonic spectrum.

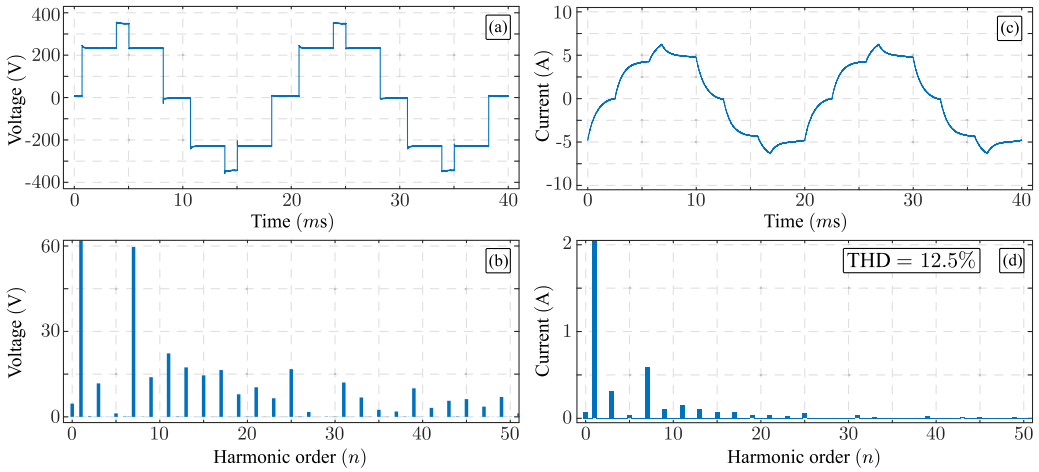


Figure 3.14: Experimental results for case I applying the BS-based SHE method. (a) CHB output voltage. (b) CHB output voltage harmonic spectrum. (c) Phase current. (d) Phase current harmonic spectrum.

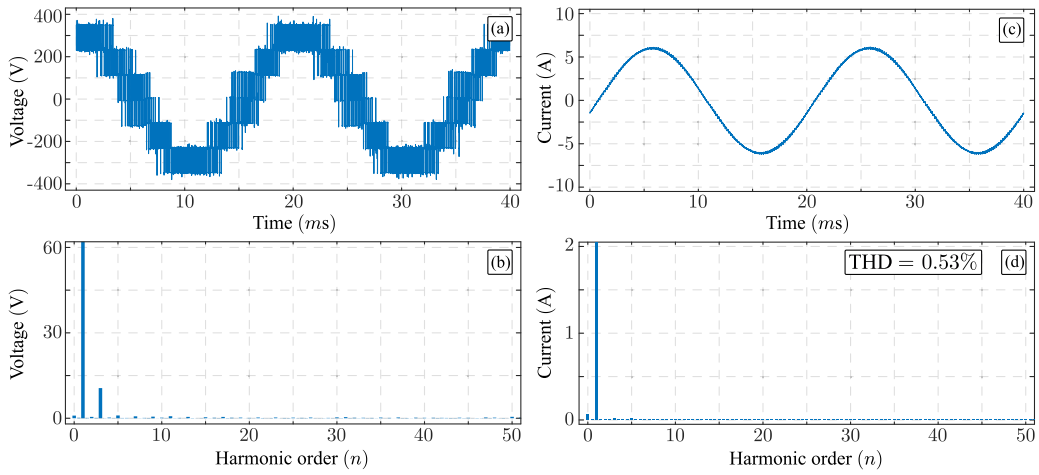


Figure 3.15: Experimental results for case I applying the PS-PWM method. (a) CHB output voltage. (b) CHB output voltage harmonic spectrum. (c) Phase current. (d) Phase current harmonic spectrum.

3.3 Extremely low-frequency PS-PWM based technique

The proposed ultra-low-frequency PS-PWM technique involves the use of conventional PS-PWM with a significantly reduced switching frequency, aiming to minimize switching losses and extend the lifespan of semiconductor devices. Simultaneously, assuming the converter is connected to a distorted grid, the technique requires the generation of a CHB voltage that compensates for the grid disturbances.

3.3.1 Mathematical description of the CHB voltage with the proposed method

In contrast to the conventional PS-PWM method, which provides only a single degree of freedom per cell, specifically, the carrier phase-displacement angle between the carriers of the power cells, the proposed modulation technique offers additional degrees of freedom. This is achieved by generalizing the unipolar PWM method to incorporate not only the modulating signal and its 180°-shifted counterpart, but

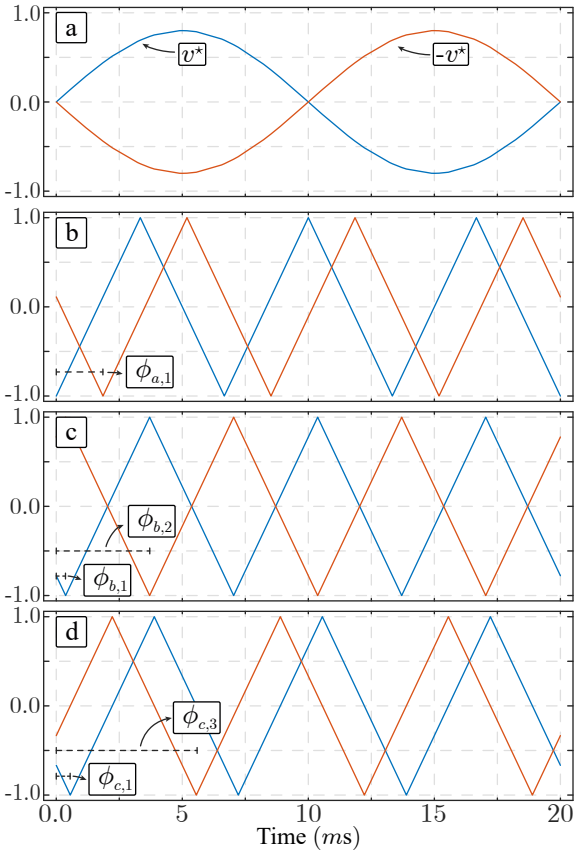


Figure 3.16: Implementation of the proposed modified unipolar PWM technique.

also two carrier signals with distinct phase-displacements, each corresponding to one of the H-bridge legs. Consequently, in the case of a three-cell CHB converter, five carrier phase-displacement angles can be independently adjusted to optimize the quality of the resulting CHB output voltage (being the first angle set to zero), as illustrated in Fig. 3.16.

In order to study the harmonic behavior of the output waveforms generated by each power cell, the double Fourier Integral can be used. As a general rule, this mathematical tool allows to describe any periodical signal as follows:

$$f(t) = f_0 + f_1(t) + f_{bb}(t) + f_{sb}(t) \tag{3.21}$$

where f_0 and $f_1(t)$ are the DC and the fundamental harmonic components, whereas $f_{bb}(t)$ and $f_{sb}(t)$ are referred to the basebands and sideband harmonic components,

respectively. Following this notation, the resulting output voltage of each individual branch in a H-bridge is determined by:

$$\begin{aligned} v_{a,x}(t) &= H_{0,x} + H_{1,x}cos(w_o t + \Theta_o) \\ &+ \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} H_{mn,x}cos(zt + (m\phi_{a,x} + n\Theta_o)) \end{aligned} \tag{3.22}$$

and

$$\begin{aligned} v_{b,x}(t) &= H_{0,x} + H_{1,x}cos(w_o t + \Theta_o) \\ &+ \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} H_{mn,x}cos(zt + (m\phi_{b,x} + n\Theta_o)) \end{aligned} \tag{3.23}$$

where variables w_o and Θ_o are referred to reference signal frequency and phase, and the index x is referred to the particular power cell of the CHB. The coefficients z, $H_{0,x}$, $H_{1,x}$ and $H_{mn,x}$ are calculated as follows:

$$\begin{aligned} z &= mw_c + nw_o \\ H_{0,x} &= \frac{V_{DC,x}}{2} \\ H_{1,x} &= \frac{V_{DC,x}M_x}{2} \\ H_{mn,x} &= \frac{2V_{DC,x}}{m\pi} J_n(\frac{m\pi M_x}{2}) sin(\frac{(m+n)\pi}{2}) \end{aligned} \tag{3.24}$$

where J_n is the first kind Bessel function of order n; m determines the harmonic group and n is referring to a specific harmonic component within the group m (the notation example figure is shown in Fig. 3.5). The resulting output voltage in the H-bridge does not contain baseband components as the converter is not operated in overmodulation region. M_x is referred to the desired modulation index, defined as:

$$V_{DC}^T = \sum_{x=1}^{N} V_{DC,x} \tag{3.25}$$

$$M = \frac{H_1}{V_{DC}^T} \tag{3.26}$$

where $V_{DC,x}$ is the DC voltage of the power cell x and H_1 is the desired fundamental voltage.

The resulting output voltage of each power cell can be then determined as:

$$v_{ab,x}(t) = v_{an,x}(t) - v_{bn,x}(t) \tag{3.27}$$

and finally the CHB output voltage can be calculated as:

$$v(t) = \sum_{x=1}^{N} v_{ab,x}(t). \tag{3.28}$$

It can be observed that harmonic components of the odd groups in (3.22) and (3.23) do not cancel each other as it happens in the conventional unipolar PWM technique. This is essential for harmonic disturbance cancellation purposes. In general, a specific carrier and sideband harmonic component of the x-th power cell can be expressed as:

$$\begin{aligned} v_{mn,x}(t) = H_{mn,x}[&cos(zt + (m\phi_{a,x} + n\Theta_o)) \\ &-cos(zt + (m\phi_{b,x} + n\Theta_o + n\pi))]. \end{aligned} \tag{3.29}$$

After some mathematical manipulation in (3.29), cosine terms can be decoupled and each particular harmonic component of the resulting output voltage can be described in magnitude and phase as:

$$\begin{aligned} v_{mn,x}(t) = -2H_{mn,x} &sin(\frac{m(\phi_{a,x} - \phi_{b,x})}{2}) \\ &sin(zt + \frac{m(\phi_{a,x} - \phi_{b,x}) + n\pi}{2} + n\Theta_o) \end{aligned} \tag{3.30}$$

that is:

$$\begin{aligned} |H_x| = |v_{mn,x}(t)| &= 2H_{mn,x}sin(\frac{m(\phi_{a,x} - \phi_{b,x}) - n\pi}{2}) \\ \angle(H_x) = \angle(v_{mn,x}(t)) &= \frac{m(\phi_{a,x} - \phi_{b,x}) + n\pi}{2} + n\Theta_o \end{aligned} \tag{3.31}$$

As shown in (3.31), it is possible to manipulate the magnitude and phase of the resulting CHB output voltage as a function of the phase-displacement angles $\phi_{a,x}$ and $\phi_{b,x}$, and obtain the desired harmonic achievement.

3.3.2 Proposed modulation technique for the CHB converter

The proposed modulation technique enables the adjustment of each individual carrier phase-displacement angle relative to the carrier of the first branch of the first power cell. This approach facilitates the use of variable carrier phase-displacement angles within each power module, thereby altering the conventional operation of the unipolar PWM. Consequently, the proposed technique offers $2N - 1$ degrees of freedom, corresponding to the carrier phase-displacement angles of each H-bridge branch in the CHB converter, allowing for the optimization of the resulting CHB output voltage.

As previously discussed, deriving the harmonic description of the CHB output voltage involves solving a complex mathematical problem. Furthermore, as the number of power cells increases, the complexity of optimizing the harmonic performance of the CHB converter grows accordingly. To address this, it is more effective to transform the problem into a multivariable nonlinear minimization problem by defining an appropriate cost function, as follows:

$$\begin{aligned} e_1 &= (H_1^* - H_1)^2 \\ e_k &= (H_k^* - H_k)^2 \\ \tau &= e_1 + e_k + \lambda \cdot WTHD0 \end{aligned} \tag{3.32}$$

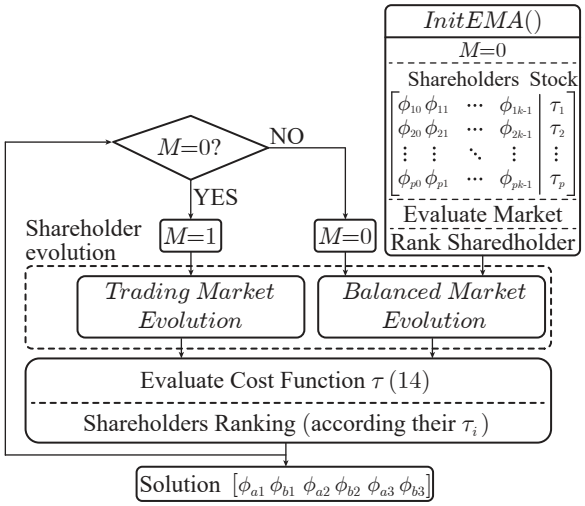


Figure 3.17: EMA implementation for the phase displacements identification.

where H_1^* and H_k^* represent the desired fundamental harmonic component and the required harmonic component to compensate the distorted grid, respectively. H_1 and H_k represent the fundamental and the k-th harmonic components, respectively, derived from the application of the proposed phase displacement angle set. Consequently, the cost function τ is defined to minimize both error variables as outlined in (3.32). For practical implementation, the expressions for magnitude and phase presented in (3.31) can be utilized. Additionally, the WTHD0 value is incorporated into the cost function τ to account for the reduction of higher-order harmonic components. A weighting factor λ is introduced to appropriately balance the cost function, giving greater emphasis to minimizing the first two terms, while treating the reduction of WTHD0 as a secondary objective. Similar to the approach used for the hybrid modulation technique, the EMA has been applied to optimize the harmonic performance and derive the most suitable carrier phase displacement angles, with the goal of minimizing the cost function defined in (3.32), as illustrated in Fig. 3.17.

An example application for the theoretical evaluation of the proposed method is provided in Table 3.4. Notably, the carrier frequency is set to a low value (150 Hz), resulting in significantly reduced switching losses. Table 3.4 also presents

Table 3.4: Operational conditions for the theoretical validation

CHB operation parameters		
DC voltage	$V_{DC,x}$ [V]	200
Desired modulation index	M	0.9
Fundamental frequency	f_o [Hz]	50
PWM carrier frequency	f_c [Hz]	150
Undesired distortion	H_3^*	$30V\angle 300$
EMA-based solutions		
Power cell 1	$[\phi_{a,1}, \phi_{b,1}]$ [°]	[0,289.75]
Power cell 2	$[\phi_{a,2}, \phi_{b,2}]$ [°]	[301.36,237,20]
Power cell 3	$[\phi_{a,3}, \phi_{b,3}]$ [°]	[156.82,60.33]
Resulting CHB output voltage		
Magnitude of fundamental component	$H_1\angle(H_1)$	$540V\angle 0$
Magnitude of third harmonic component	$H_3\angle(H_3)$	$30V\angle 60$

the set of carrier phase-displacement angles derived through the EMA algorithm. These phase-displacement angles are optimized to minimize the cost function τ for a desired output voltage with harmonic components $[H_1, H_3]$ equal to [540, 30] and corresponding phases $[P_1, P_3]$ equal to [0°, 60°]. The resulting output voltage magnitude spectrum and its phase are shown in Fig. 3.18, proving the effectiveness of the proposed modulation strategy.

3.3.3 Experimental results

In order to prove the effectiveness of the proposed modulation technique, experimental tests have been conducted on the same laboratory setup used for the hybrid modulation strategy proposed previously (Fig. 3.10). Setup parameters are summarized in Table 3.5. The three-cell single-phase CHB, with each cell independently supplied by a DC source, is connected toa grid emulator. Parameter λ in the cost function has been fixed to one to obtain good results.

The experiments explore two distinct scenarios to demonstrate the effectiveness of the proposed modulation technique in achieving the desired fundamental voltage while simultaneously rejecting an undesirable harmonic component present in

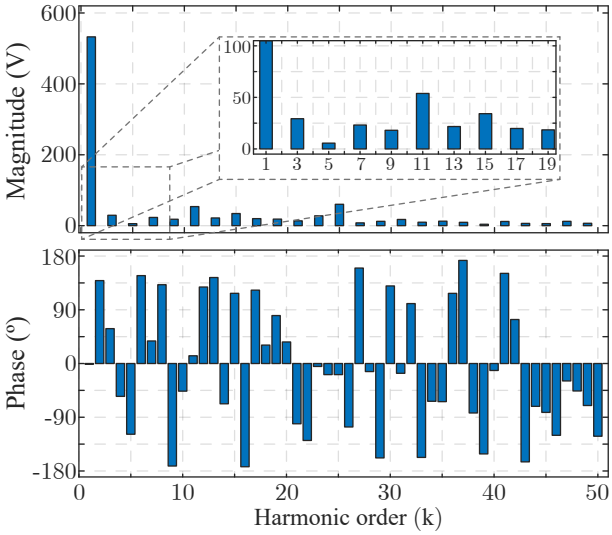


Figure 3.18: Theoretical evaluation of the particular operation point of the CHB output voltage given in Table 3.4

the grid. The required fundamental voltage specifications are detailed in Table 3.5, and the specific scenarios under investigation are outlined in Table 3.6. In these scenarios, a significant third harmonic content is present in the grid voltage. The proposed technique is employed to generate the desired fundamental component and to compensate for this negative low-order harmonic. The corresponding phase-displacement angles for the proposed modulation technique are also provided in Table 3.6. In each scenario, the EMA is executed to determine the optimal carrier phase-displacement angles, ensuring the achievement of all objectives by minimizing the cost function τ.

For each experiment, the resulting output voltage, current and their respective harmonic spectrum are obtained. First of all, conventional PS-PWM has been ap-

Table 3.5: Experimental CHB setup parameters

Parameter	**Symbol**	**Value**
Power module DC Voltage	$V_{DC,x}$ [V]	120
Desired modulation index	M	0.9
Fundamental frequency	f_c [Hz]	50
PWM carrier frequency	f_c [Hz]	150
Desired fundamental component	H_1^* [Hz]	$324\angle 0$

plied, with carrier frequency equal to 150 Hz, generating a fundamental voltage with modulation index equal to 0.9. The obtained results are represented in Fig. 3.19, where it can be observed the presence of a nonnegligible third harmonic component in the output current, due to the non-compensated distorted grid.

In contrast, the results obtained using the proposed technique are presented in Figs. 3.20 and 3.21. These results demonstrate superior performance, even in the presence of a distorted grid. Specifically, it is evident that the objectives defined in the cost function are successfully achieved, not only in terms of the fundamental voltage magnitude but also in the harmonic rejection capability of the resulting current injected into the grid emulator. The THD, calculated up to the 50th harmonic order as a figure of merit, is also provided in the respective figures, highlighting the improved performance of the proposed modulation strategy, as anticipated.

To evaluate the effectiveness of the proposed technique, a comparison with a well-established method from the literature was conducted. Initially, SHE/SHM techniques were tested, as these methods also aim to minimize switching losses. An experiment using the SHE/SHM technique was performed with a modulation index of 0.9, a specific third harmonic component of 12V, and the elimination of the fifth harmonic component. The resulting data, shown in Fig. 3.22, reveal that although the third and fifth harmonic contents meet the expected values in the output volt-

Table 3.6: Specific operational conditions of the proposed technique for two different scenarios

$H_3^\star$	**Phase-displacement angles**		**Values**
$20\angle 120$	Power Cell 1	$[\phi_{a,1}, \phi_{b,1}]$ (°)	$[0, 289.75]$
	Power Cell 2	$[\phi_{a,2}, \phi_{b,2}]$ (°)	$[301.36, 237.20]$
	Power Cell 3	$[\phi_{a,3}, \phi_{b,3}]$ (°)	$[156.82, 60.33]$
$30\angle 300$	Power Cell 1	$[\phi_{a,1}, \phi_{b,1}]$ (°)	$[0, 79.92]$
	Power Cell 2	$[\phi_{a,2}, \phi_{b,2}]$ (°)	$[55.37, 310.17]$
	Power Cell 3	$[\phi_{a,3}, \phi_{b,3}]$ (°)	$[303.83, 26.25]$

age, a significant third harmonic component remains in the output current. This demonstrates that SHE/SHM methods are unable to provide adequate harmonic compensation, as the phase of the harmonic components is not considered in the determination of switching angles. Furthermore, SHE methods do not account for higher-order harmonics that are not eliminated, leading to elevated THD values. The proposed method addresses this limitation by incorporating the WTHD0 term in the cost function, which improves harmonic performance.

An additional experiment was conducted to assess the performance of the PS-PWM method using a high-frequency carrier signal (3 kHz) and conventional carrier phase-displacement angles. Harmonic compensation was implemented by adding a required third harmonic component (both magnitude and phase) to the voltage reference of one of the power modules. The results, shown in Fig. 3.23, demonstrate that while the current harmonic quality is significantly improved, this comes at the cost of very high switching losses.

In summary, the proposed method serves as a balanced solution that bridges the gap between SHE/SHM methods and the PS-PWM technique with high-frequency carrier signals. It successfully compensates for the undesired third harmonic component and reduces higher-order harmonics, all while maintaining controlled switching losses.

3.4 Key outcomes

The key outcomes derived from the two studies discussed in this chapter can be summarized as follows:

- Both studies emphasize the decisive influence of the modulation technique and control strategy on the converter's performance. The careful design of these aspects not only impacts output quality but also plays a significant role in determining the converter's overall efficiency and operating costs.

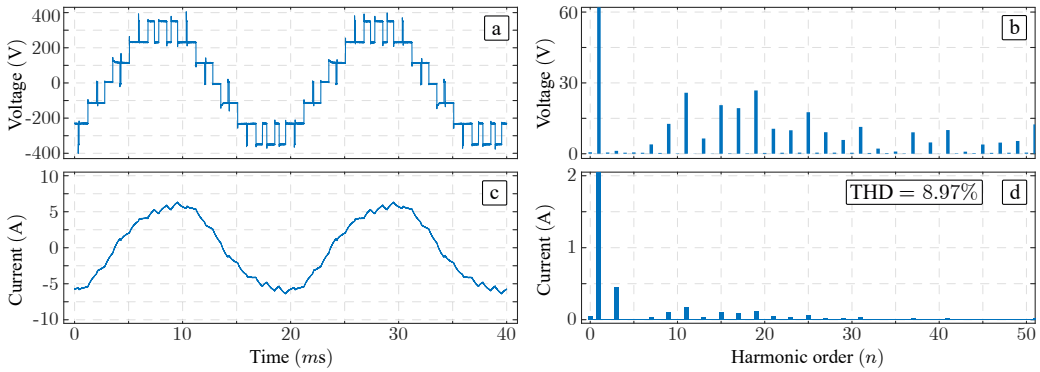


Figure 3.19: Experimental results considering the PS-PWM method applying the conventional carrier phase displacement angles: (a) Output voltage. (b) Output voltage harmonic spectrum. (c) Output current (d) Output current harmonic spectrum.

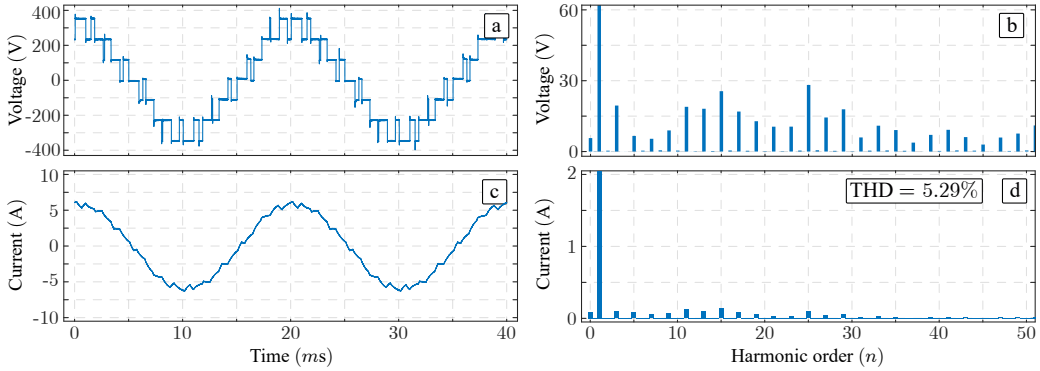


Figure 3.20: Experimental results for proposed modulation technique considering the operational point $H_3^* = 20\angle 120$ reported in Table 3.6. (a) Output voltage. (b) Output voltage harmonic spectrum. (c) output current (d) output current harmonic spectrum.

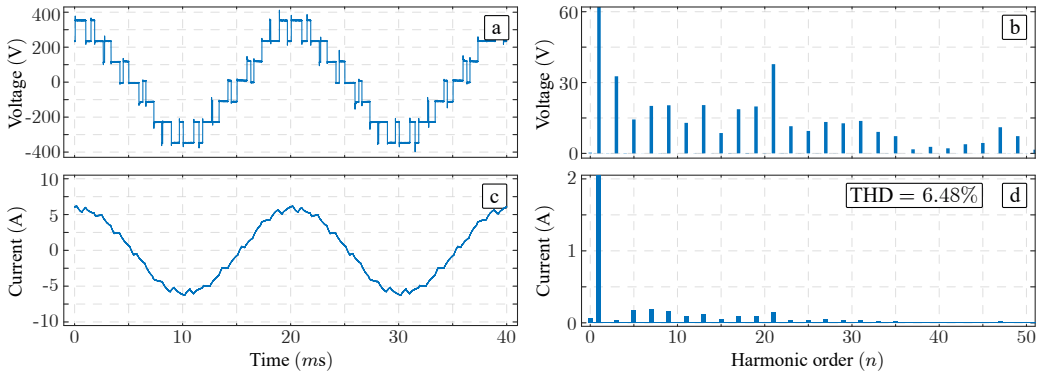


Figure 3.21: Experimental results for proposed modulation technique considering the operational point $H_3^* = 30\angle 300$ reported in Table 3.6. (a) Output voltage. (b) Output voltage harmonic spectrum. (c) output current (d) output current harmonic spectrum.

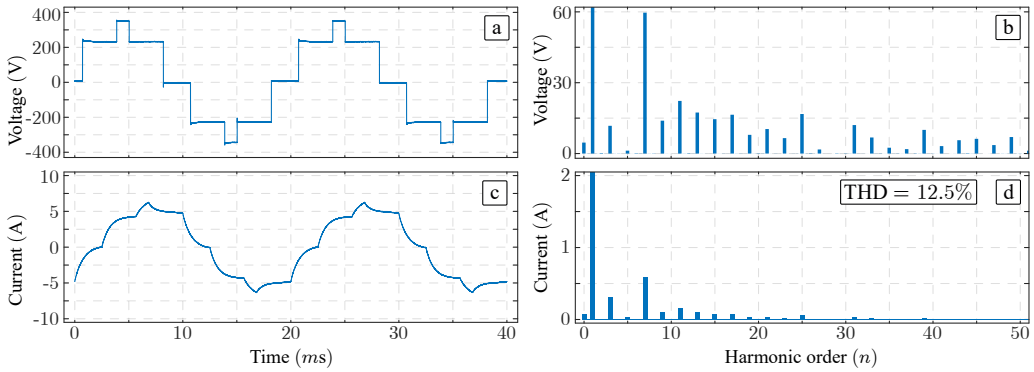


Figure 3.22: Experimental results for SHE/SHM technique considering a modulation index equal to 0.9, an specific third harmonic component equal to 12 V and the elimination of the fifth harmonic component. Switching angles are [$\alpha_1 = 22.61°$, $\alpha_2 = 22.64°$, $\alpha_3 = 79.62°$]. (a) Output voltage. (b) Output voltage harmonic spectrum. (c) Output current. (d) Output current harmonic spectrum.

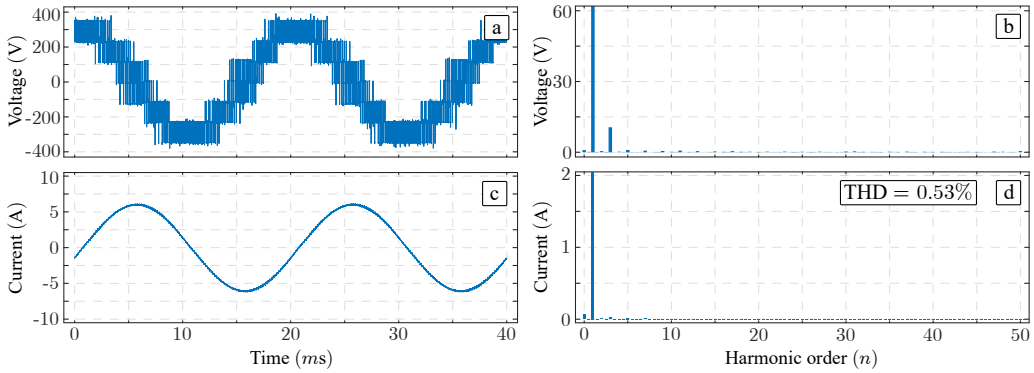


Figure 3.23: Conventional PS-PWM technique with harmonic cancellation capability considering a modulation index equal to 0.9. (a) Output voltage. (b) Output voltage harmonic spectrum. (c) Output current. (d) Output current harmonic spectrum

- A hybrid-PWM strategy has been proposed and validated experimentally, demonstrating its capability to achieve specific harmonic cancellation by limiting additional losses. This approach presents an excellent compromise between waveform quality and efficiency, by guaranteeing reduced operational and maintenance costs.

- Experimental results have shown that the hybrid-PWM method is particularly effective in addressing grid disturbances, suggesting its applicability in environments where grid quality is distorted.

- Similarly, a novel extremely low-frequency PS-PWM technique has been introduced, designed to extend the operational range of the converter while also mitigating the presence of undesirable grid low-order harmonics.

- The proposed low-frequency PS-PWM method has been supported by a rigorous mathematical analysis and then validated through experimental testing, confirming both its theoretical and practical feasibility.

- Collectively, these results highlight the potential of these two innovative PWM strategies to enhance the performance, reliability, and economic advantages of multilevel converters, especially in presence of energy system requirements.

Chapter 4

An Innovative Synthesis Technique of Control Signals for Power Converters Based on Pulse Position Modulation

The diffusion of diverse power converter topologies introduces significant challenges in modulation techniques, which must be carefully designed to meet specific performance requirements. These include improving the harmonic quality of output waveforms and minimizing switching losses, ultimately extending the operational lifespan of converters. As carefully stated in the previous chapters, the primary objective of a modulation technique is to generate a reference waveform with minimal low-order harmonic distortion. This is achieved by shifting unavoidable distortions to higher-order harmonics, which can be more efficiently filtered, thereby enhancing overall system performance [40–44].

In this sense, PWM technique, extensively studied since the 1960s, provides a straightforward approach for generating a switched voltage waveform, where the average voltage corresponds to the desired reference. In the output voltage spectrum of a PWM system, the first significant harmonic group is located around the carrier frequency f_c (corresponding to the R-th harmonic order), effectively eliminating

low-order harmonics. Increasing R shifts harmonics to higher frequencies, making them easier to filter; however, this also leads to increased switching losses and heat dissipation. The harmonic performance of PWM is highly influenced by the placement of each switching pulse within its sampling interval, T_c. When a triangular carrier is used, pulses are symmetrically centered within each carrier period, whereas a sawtooth carrier results in pulses positioned at the edges of T_c. Studies indicate that using a triangular carrier enhances harmonic performance due to the improved symmetry of pulse placement. However, since pulse positions are directly determined by the carrier-modulating signal comparison, they remain fixed, imposing inherent limitations on harmonic optimization.

As outlined earlier, to enhance harmonic performance while minimizing switching losses, SHE/SHM techniques are among the most widely studied approaches. In conventional SHE/SHM, the switching angles (specific instants at which the power converter's gating signals change) are precomputed for a given modulation index M. These angles are carefully selected to eliminate specific harmonics or reduce WTHD while maintaining the desired fundamental voltage level, by solving a system of nonlinear equations offline. The computed firing angles, covering an entire fundamental period T_o, are then stored in a look-up table (LUT) for real-time implementation. However, despite its effectiveness in harmonic control, SHE exhibits a slower dynamic response compared to carrier-based PWM. This limitation arises from SHE/SHM's operation at the fundamental frequency rather than the higher switching frequency, significantly restricting its adaptability in closed-loop control applications.

Therefore, a novel modulation strategy, termed Pulse Position Modulation (PPM), is introduced in this chapter to enhance the harmonic quality of voltage and current waveforms in DC/AC converters while simultaneously reducing switching losses and improving dynamic performance. Unlike conventional carrier-based PWM, which maintains fixed pulse positions dictated by the carrier waveform (triangu-

lar or sawtooth), the proposed PPM technique dynamically adjusts the placement of gate pulses within each sampling interval T_c. This adaptive positioning enables superior harmonic performance beyond the capabilities of traditional PWM techniques, offering a more flexible and efficient approach to power conversion.

This chapter presents a comprehensive analysis of the signal synthesis strategy employed for generating PPM control signals, including a detailed mathematical formulation. The proposed technique is then implemented in a basic Full-Bridge converter configuration to demonstrate its effectiveness, and then in a three-phase inverter configuration in order to reduce its common-mode voltage. Finally, experimental results are provided to validate the performance and practical feasibility of the proposed approach.

4.1 PPM signal synthesis strategy

The PPM technique is designed to generate gate-driving signals for DC/AC converter power devices without relying on the conventional comparison between a carrier and a modulating signal. Instead, it focuses on directly determining the switch-on instants within each sampling period, ensuring that the desired fundamental component is accurately achieved. The driving signal is synthesized as a sum of individual pulses, each confined to a specific sampling interval. This approach allows for precise control over the spectral composition of the waveform by positioning each pulse flexibly within its corresponding sampling period.

To illustrate the fundamental concept of PPM, it is useful to begin with conventional PWM, which is typically derived from the comparison of a triangular carrier signal with a modulating waveform. As shown in Fig. 4.1, the first graph represents a PWM signal over a fundamental period, with eight pulses (corresponding to $R = 8$), each centered within its respective sampling interval. It originates from a sinusoidal modulating signal, as will be discussed later. The subsequent graphs

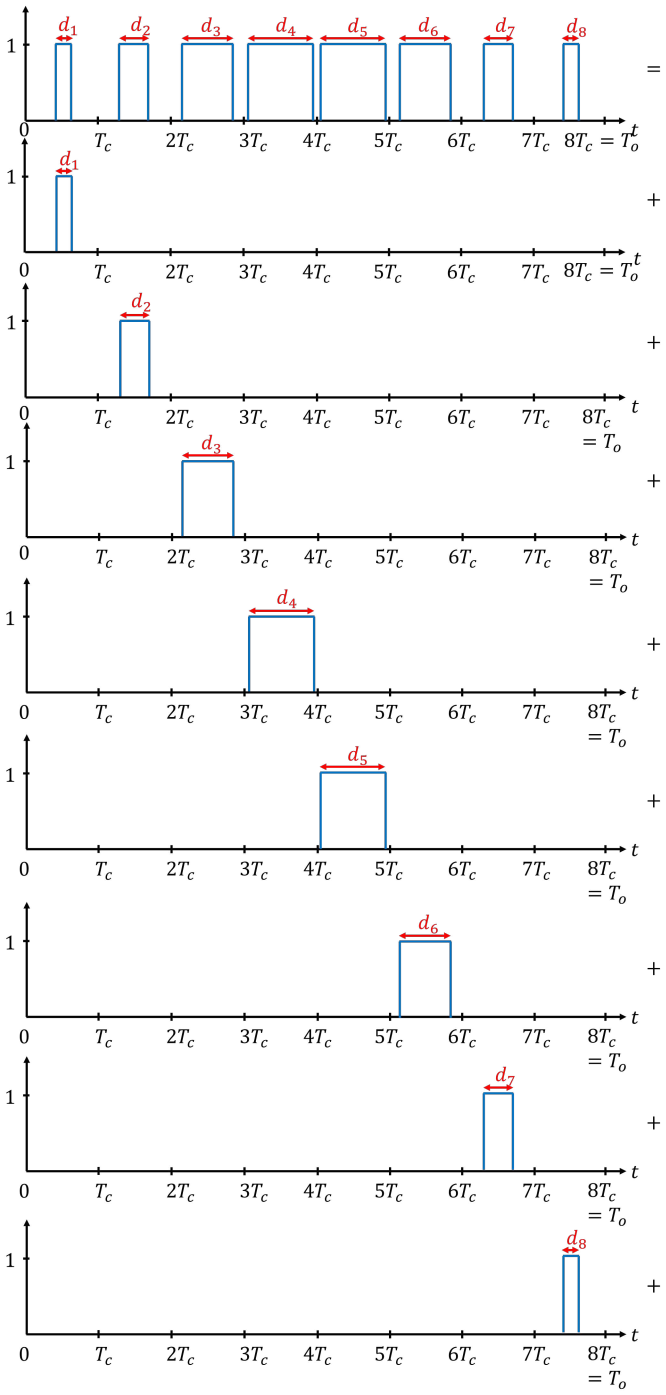


Figure 4.1: PWM signal synthesis.

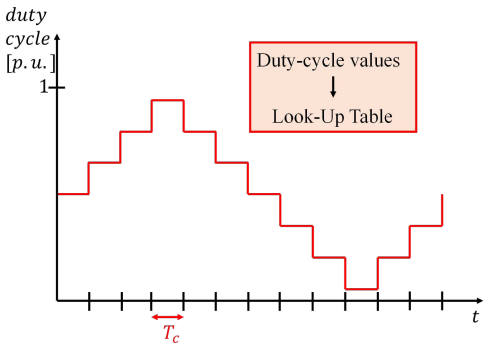


Figure 4.2: Discretized modulating signal.

demonstrate that the PWM signal can be expressed as the sum of R individual pulses over a fundamental period T_o, with each pulse occupying a distinct sampling interval T_c. Each of these pulses can be conceptualized as a square wave with a period T_o and a duty cycle that is either determined by a closed-loop control system or pre-set in an open-loop configuration. In fact, the modulation index, which dictates the fundamental component of the converter's output voltage, is either computed by the controller or specified by the user. Based on this modulation index, a discretized sinusoidal modulating signal is generated with a sampling period T_c, as depicted in Fig. 4.2. The amplitude of this sinusoidal waveform at each T_c corresponds to the duty cycles of the individual pulses that collectively form the PWM signal. Consequently, in a traditional PWM scheme, the width of each pulse is fixed according to the desired fundamental component and cannot be altered. When using a triangular carrier, the resulting driving pulses are symmetrically centered within their respective sampling intervals and cannot be repositioned due to the inherent structure of the triangular waveform.

In contrast, PPM introduces an additional degree of freedom by allowing each pulse to be repositioned within its sampling interval T_c, leading to enhanced performance characteristics. This flexibility improves harmonic quality by enabling an optimized pulse arrangement, as will be further explored. If a PWM signal can be synthesized as the sum of R pulses within a fundamental period, then its spectral

characteristics are determined by the collective contribution of the individual pulse spectra. This principle is illustrated in Fig. 4.3, where a PWM waveform is synthesized with a frequency ratio $R = 10$ and analyzed in both time and frequency domains. The left side of the figure presents a series of graphs, each showing an additional pulse contributing to the cumulative PWM signal within T_o. The right side displays the corresponding harmonic amplitude spectra, clearly revealing the characteristic harmonic groups of a PWM-modulated DC/AC converter waveform. As more pulses are incorporated, the spectral composition becomes more defined, with the first major harmonic group centered around the 10th harmonic order due to $R = 10$. Since the fundamental harmonic magnitude depends on the duration of each pulse, and the overall waveform is designed within a normalized range (0 to 1), the mean value of the signal is preserved. Moving away from conventional PWM generation, where the complete waveform results from the direct comparison of modulating and carrier signals, PPM enables the synthesis of the PWM signal without the need for such comparisons. Instead, by summing R pulses within their respective sampling periods using established signal synthesis principles, the modulation process gains additional flexibility. Each pulse can be precisely positioned within T_c, unconstrained by carrier-based limitations. However, shifting pulse positions impacts the harmonic spectrum, necessitating further analysis to optimize harmonic performance.

By analyzing each individual pulse in Fig. 4.1, it becomes evident that repositioning a pulse within its respective sampling interval T_c, while maintaining its original width, offers a novel approach to improve harmonic performance. This method overcomes the constraint of fixed pulse centering inherent in conventional carrier-based PWM techniques, enabling enhanced control over the harmonic characteristics of the synthesized waveform. By examining how each pulse contributes to the overall spectral composition when repositioned within its T_c, it is possible to understand the influence of pulse placement on the harmonic quality of the resulting

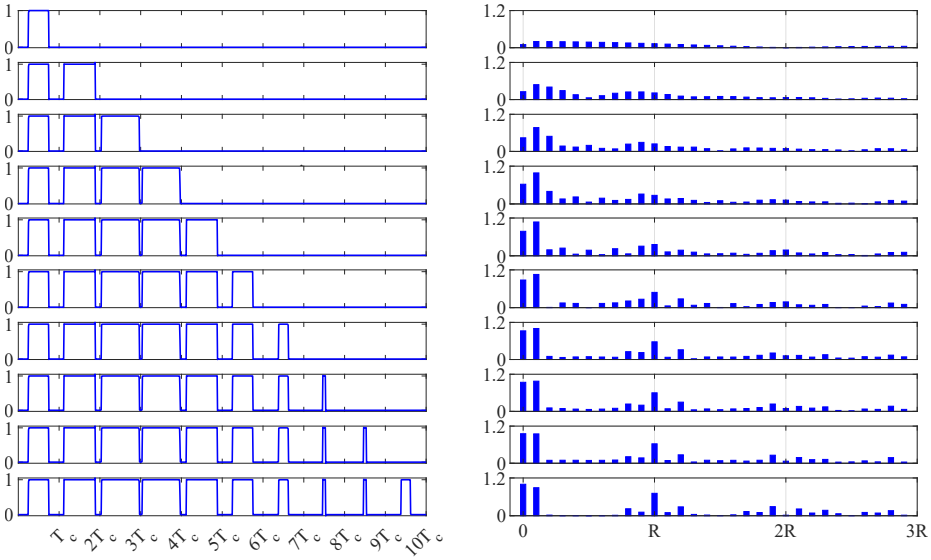


Figure 4.3: PWM signal synthesis in time and frequency domains.

signal. A particularly insightful analysis involves evaluating the harmonic impact of a single pulse as it is shifted within its sampling period. As illustrated in Fig. 4.4, shifting a pulse does not alter the harmonic amplitude spectrum but does affect the phase spectrum, as shown in Fig. 4.4b. This phenomenon is further explored in Figs. 4.4c- 4.4d, which highlight the behavior of the 10th and 15th harmonics under pulse shifting. It can be observed that shifting the pulse within its sampling interval results solely in a rotation of the harmonic vectors, meaning that it affects the phase of the harmonics but does not alter their magnitude. In other words, pulse displacement influences the harmonic phase while leaving the harmonic amplitude unchanged. As demonstrated in [45], the amplitude of the harmonics in the Fourier Series representation of a single rectangular pulse varies with the harmonic order k according to a cardinal sine (*sinc*) function. This dependency is determined exclusively by the pulse's duration and amplitude, not its position, as expressed in:

$$A_k = a \cdot d \cdot \text{sinc}(k \cdot d) \tag{4.1}$$

where A_k is the amplitude of the k-th harmonic, a is the pulse amplitude and d is

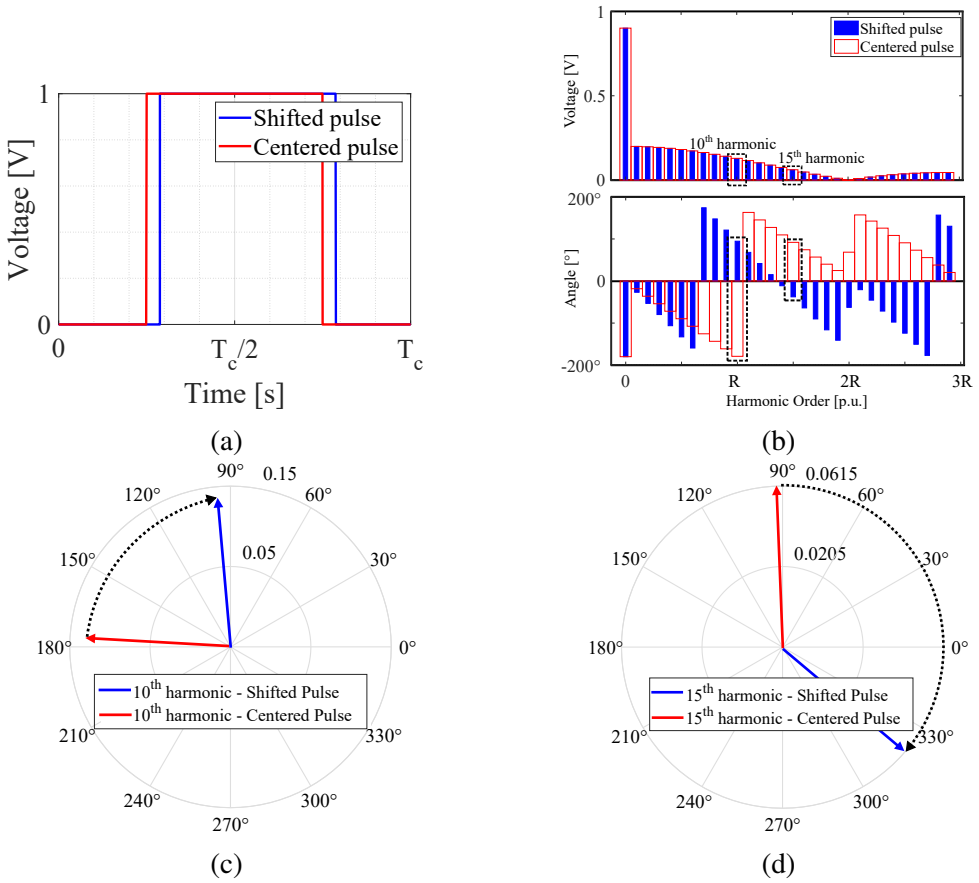


Figure 4.4: Effects of pulse shifting on the amplitude and phase harmonic spectra. (a) Time-domain pulse shifting. (b) Amplitude and phase harmonic spectra comparison. (c) Polar diagram of 10th harmonic for centered and shifted pulses. (d) Polar diagram of 15th harmonic for centered and shifted pulses.

its duration (i.e., duty cycle). However, the phase spectrum is directly influenced by the pulse's position within its sampling interval. As a result, in Fig. 4.3, progressing from the top to the bottom, the amplitude spectrum is continuously updated as each additional pulse, characterized by a specific duration and position within T_c, is incorporated. This transformation occurs due to the vector summation of harmonic components, which accounts for both their amplitudes and phase shifts, ultimately shaping the overall spectral composition of the signal.

4.2 Mathematical analysis

To create an analytical tool for directly synthesizing control/gate signal in the shape of a pulse train with adjustable positions of the single pulses, a thorough examination of individual pulse behavior is necessary. This can be done through Fourier analysis, a cornerstone of modern signal theory [45]. According to this theory, a generic periodic signal can be expressed as a sum of sinusoidal signals with specific amplitudes, frequencies, and phases, as shown in:

$$x(t) = A_0 + 2\sum_{k=1}^{\infty} A_k cos(2\pi k f_o t + \theta_k) \tag{4.2}$$

where a signal $x(t)$ can be seen as the sum of a constant term A_0 and a series where the k-th term has amplitude A_k, frequency kf_o and initial phase θ_k. For simplicity and to facilitate a clearer understanding of the relationship between the time and frequency domains during the synthesis of a control/gate signal in the form of a pulse train, a case study with only four pulses is presented. This approach allows for a detailed analysis of how each individual pulse contributes to the overall signal spectrum, as shown in Fig. 4.3, when summed in the time domain. While this case study is limited to four pulses, the synthesis process can be easily extended to a larger number.

Starting with the first pulse in Fig. 4.5, denoted as $x_1(t)$, the signal analysis can be elaborated. This pulse is a square wave with duration d_1 and period T_o, and its turn-on time is defined by $t_{on,1}$. The signal $x_1(t)$ can be expressed in this way:

$$x_1(t) = A_{1,0} + 2\sum_{k=1}^{\infty} A_{1,k} cos(2\pi k f_o t) \tag{4.3}$$

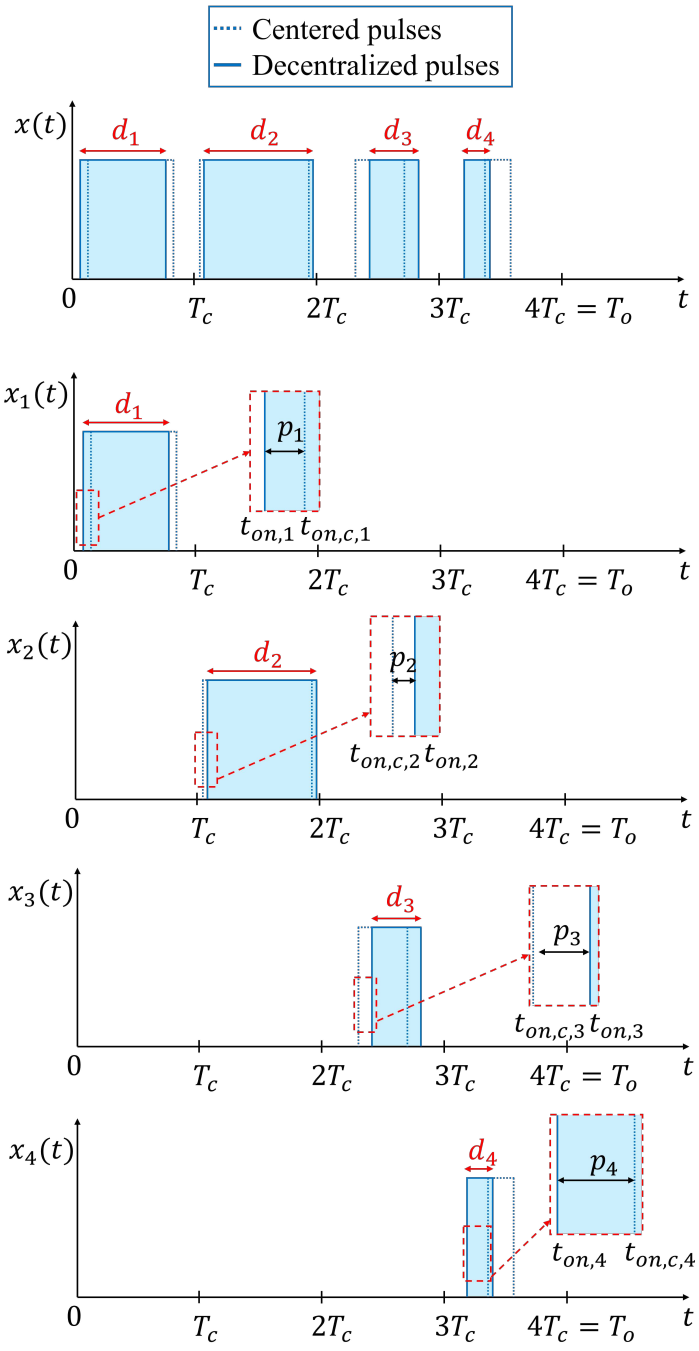


Figure 4.5: PPM signal building with R=4.

where:

$$A_{1,k} = \frac{1}{T_0}\int_0^{T_0} x_1(t)e^{-i2\pi k f_0 t}dt = \frac{1}{T_0}\int_{t_{on,1}}^{t_{t_{on,1}}+d_1} 1 \cdot e^{-i2\pi k f_0 t}dt = \frac{i}{2\pi k}e^{-i2\pi k f_0 t_{on,1}}(e^{-i2\pi k f_0 d_1} - 1) \tag{4.4}$$

and:

$$A_{1,0} = \frac{1}{T_0}\int_0^{T_0} x_1(t)e^{-i2\pi 0 f_0 t}dt = \frac{1}{T_0}\int_{t_{on,1}}^{t_{t_{on,1}}+d_1} 1 = \frac{1}{T_0}(t_{on,1} + d_1 - t_{on,1}) = \frac{d_1}{T_0} = d_1 f_0 \tag{4.5}$$

because $x_1(t)$ has unitary amplitude and is nonzero only between $t_{on,1}$ and $t_{on,1} + d_1$. Actually, the turn-on time $t_{on,1}$ can be expressed as the sum of $t_{on,c,1}$, the turn-on time if the pulse is centered in T_c, and the pulse shift introduced, p_1:

$$t_{on,c,1} = \frac{T_c - d_1}{2} \tag{4.6}$$

$$t_{on,1} = \frac{T_c - d_1}{2} + p_1 \tag{4.7}$$

where p_1 can take positive or negative values. Therefore, after proper substitutions, $x_1(t)$ becomes:

$$x_1(t) = d_1 f_0 + 2\sum_{k=1}^{\infty}(\frac{i}{2\pi k}e^{-i2\pi k f_0(\frac{T_c-d_1}{2}+p_1)(e^{-i2\pi k f_0 d_1}-1)})cos(2\pi k f_0 t) \tag{4.8}$$

4.8 represents the Fourier Series decomposition of the first pulse characterizing the signal in Fig. 4.5, i.e., a pulse with d_1 duration and delayed or anticipated of an unknown time quantity p_1, respect to its conventional centered position in the time interval [0,T_c]. Analogously, the same analysis can be carried out for the second

pulse of the same signal. It can be expressed as:

$$x_2(t) = A_{2,0} + 2\sum_{k=1}^{\infty} A_{2,k} cos(2\pi k f_o t) \tag{4.9}$$

where:

$$\begin{aligned} A_{2,k} = \frac{1}{T_0}\int_0^{T_0} x_2(t) e^{-i2\pi k f_0 t} dt = \\ \frac{1}{T_0}\int_{t_{on,2}+T_c}^{t_{t_{on,2}}+d_2+T_c} 1 \cdot e^{-i2\pi k f_0 t} dt = \\ \frac{i}{2\pi k} e^{-i2\pi k f_0 (t_{on,2}+T_c)} (e^{-i2\pi k f_0 d_2} - 1) \end{aligned} \tag{4.10}$$

and:

$$\begin{aligned} A_{2,0} = \frac{1}{T_0}\int_0^{T_0} x_1(t) e^{-i2\pi 0 f_0 t} dt = \frac{1}{T_0}\int_{t_{on,2}+T_c}^{t_{on,2}+d_2+T_c} 1 = \\ \frac{1}{T_0}(t_{on,2} + d_2 - t_{on,2}) = \frac{d_2}{T_0} = d_2 f_0 \end{aligned} \tag{4.11}$$

As for the first pulse, also in this case the turn-on time $t_{on,2}$ can be expressed as the sum of $t_{on,c,2}$, the turn-on time if the pulse is centered in T_c, and the pulse shift introduced, p_2. Differently from the first pulse analysis, the signal $x_2(t)$ is defined in the time interval [T_c,$2T_c$], therefore the turn-on time must be added to T_c. Therefore, $x_2(t)$, representing the second pulse in Fig. 4.5, with d_2 duration and delayed or anticipated of an unknown quantity p_2 can be decomposed in Fourier Series as:

$$x_2(t) = d_2 f_0 + 2\sum_{k=1}^{\infty} \left(\frac{i}{2\pi k} e^{-i2\pi k f_0 (\frac{T_c - d_2}{2} + p_2 + T_c)(e^{-i2\pi k f_0 d_2} - 1)}\right) cos(2\pi k f_0 t) \tag{4.12}$$

Equivalently, the third pulse of the signal in Fig. 4.5 can be treated in the same way of the previous two pulses. Therefore, the analytical expression of the Fourier

Series of the pulse is expressed as:

$$x_3(t) = d_3 f_0 + 2\sum_{k=1}^{\infty}(\frac{i}{2\pi k}e^{-i2\pi k f_0(\frac{T_c-d_3}{2}+p_3+2T_c)(e^{-i2\pi k f_0 d_3}-1)})cos(2\pi k f_0 t) \quad (4.13)$$

where d_3 is the time duration of the pulse, p_3 is the delay or the anticipation applied respect to the initial centralized position of the signal within its T_c, and the turn-on time must be added to $2T_c$, because the pulse in question is defined between $2T_c$ and $3T_c$.

Finally, the analytical expression of the fourth pulse in Fig. 4.5 is derived:

$$x_4(t) = d_4 f_0 + 2\sum_{k=1}^{\infty}(\frac{i}{2\pi k}e^{-i2\pi k f_0(\frac{T_c-d_4}{2}+p_4+3T_c)(e^{-i2\pi k f_0 d_4}-1)})cos(2\pi k f_0 t) \quad (4.14)$$

where d_4 is the time duration of the pulse, p_4 is the delay or the anticipation applied respect to the initial centralized position of the signal within its T_c, and the turn-on time must be added to $3T_c$, because the pulse is nonzero between $3T_c$ and $4T_c$. Therefore, it is possible to derive the Fourier series of the full signal in Fig. 4.5, adding the contributions of the four pulses that characterize it. The signal can be represented as the summation of the four analytical expressions derived in 4.8, 4.12, 4.13 and 4.14:

$$\begin{aligned} x(t) &= x_1(t) + x_2(t) + x_3(t) + x_4(t) \\ &= \sum_{n=1}^{4} d_n f_0 + 2\sum_{n=1}^{4}\sum_{k=1}^{\infty}\left(\frac{i}{2\pi k}e^{-i2\pi k f_0\left(\frac{T_c-d_n}{2}+p_n+(n-1)T_c\right)}\left(e^{-i2\pi k f_0 d_n}-1\right)\right) \\ &\quad \cos(2\pi k f_0 t) \end{aligned} \quad (4.15)$$

In 4.15, n represents the pulse index; the turn-on time of each pulse is added to $(n-1)T_c$, in order to take into account its position within the fundamental period T_0. Then, the analysis can be extended to a generic signal characterized by R pulses

within a fundamental period T_0, and the analytical expression derived is:

$$x(t) = \sum_{n=1}^{R} d_n f_0 + 2\sum_{n=1}^{R}\sum_{k=1}^{\infty}\left(\frac{i}{2\pi k} e^{-i2\pi k f_0\left(\frac{T_c - d_n}{2} + p_n + (n-1)T_c\right)\left(e^{-i2\pi k f_0 d_n} - 1\right)}\right) cos(2\pi k f_0 t) \tag{4.16}$$

where the number of pulses added in order to build the signal is set to R. The first term of the general expression represents the mean value of the signal, which is derived from adding the mean values of each individual pulse. The second term in 4.16 represents the sum of the infinite harmonics that make up each pulse of the signal. This indicates that the overall signal's spectrum is influenced by the spectrum of each individual pulse and is directly affected by the displacement of these pulses. It is important to note that each pulse can only be shifted within its own T_c, thus each p_n value is constrained within specific limits. Examining a single pulse in Fig. 4.6, initially centered within its own T_c, it is possible to determine the maximum allowable delay or advance $p_{n,max}$:

$$p_{n,max} = \frac{T_c - d_n}{2} \tag{4.17}$$

ensuring that the pulse does not encroach into the adjacent T_c.

The analysis conducted to determine the harmonic content of a PWM signal

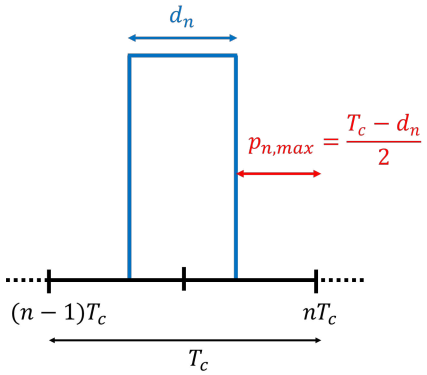


Figure 4.6: Maximum shifting value of the single pulse applying PPM.

directly has led to a spectrum that varies with the position of each pulse as a variable parameter. This approach overcomes the limitations of carrier-based PWM, where pulse positions are fixed by the shape of the carrier signal. The added degrees of freedom enable significant harmonic improvements that would not be achievable if the pulses were fixed within their T_c.

4.3 Case study: Full-Bridge converter

The innovative modulation approach introduced in the previous section can be applied to each kind of converter, but in order to prove its effectiveness and to explain its practical digital implementation, the analysis is first conducted on a conventional Full-Bridge converter (also known as H-bridge), as the one shown in Fig. 4.7. First of all, the expression of leg A voltage $v_{Ao}(t)$, can be derived, based on PPM approach. Anyway, it assumes values between $-\frac{V_{DC}}{2}$ and $\frac{V_{DC}}{2}$, with zero mean value, reproducing the shape of $x(t)$. However, the output voltage is modulated based on the modulation index m set by the user in an open-loop configuration. Therefore, the expression of $v_{Ao}(t)$ can be derived as:

$$\begin{aligned} v_{Ao}(t) &= m\left(\frac{V_{DC}}{2}x(t) - \frac{V_{DC}}{2}\right) \\ &= \sum_{n=1}^{R} m\frac{V_{DC}}{2}d_n f_0 - m\frac{V_{DC}}{2} \\ &\quad + mV_{DC}\sum_{n=1}^{R}\sum_{k=1}^{\infty}\left(\frac{i}{2\pi k}e^{-i2\pi k f_0\left(\frac{T_c-d_n}{2}+p_n+(n-1)T_c\right)}\left(e^{-i2\pi k f_0 d_n}-1\right)\right) \\ &\quad \times \cos(2\pi k f_0 t) \end{aligned} \tag{4.18}$$

The analysis can be extended to leg B of the Full-Bridge by considering a new duty cycle array. The necessity of synthesizing a leg voltage $v_{Bo}(t)$, whose funda-

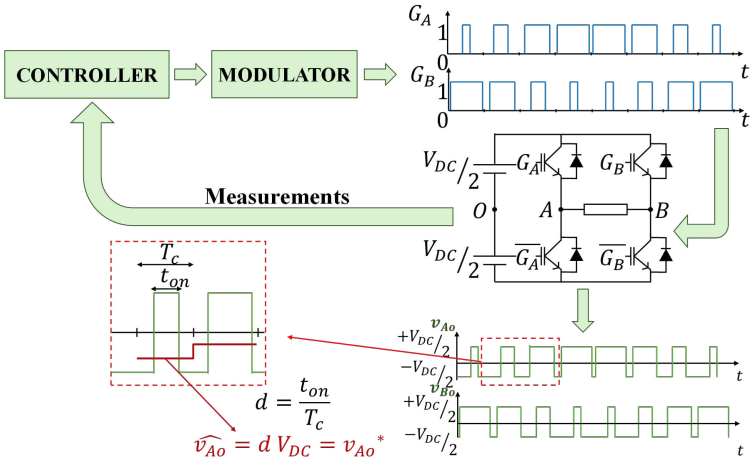


Figure 4.7: Typical structure of a control and modulation method of a Voltage Source Inverter.

mental harmonic has equal amplitude but opposite phase with respect to the fundamental harmonic of $v_{Ao}(t)$, leads for leg B to the definition of pulses duration array $d_{180,n}$ that is different from the d_n array defined for the leg A. Following a similar analysis as for leg A, the expression for $v_{Bo}(t)$ can be obtained:

$$
\begin{aligned}
v_{Bo}(t) = = & \sum_{n=1}^{R} m\frac{V_{DC}}{2} d_{180,n} f_0 - m\frac{V_{DC}}{2} \\
& + mV_{DC} \sum_{n=1}^{R}\sum_{k=1}^{\infty} \left(\frac{i}{2\pi k} e^{-i2\pi k f_0 \left(\frac{T_c - d_{180,n}}{2} + p_{180,n} + (n-1)T_c \right)} \left(e^{-i2\pi k f_0 d_{180,n}} - 1 \right) \right) \\
& \times \cos(2\pi k f_0 t)
\end{aligned}
\tag{4.19}
$$

In 4.19 it can be seen the introduction of $p_{180,n}$, an array containing the displacements of the pulses characterizing the leg B gate signal, respect to their centered positions. Hence, the Full-Bridge output voltage expression, $v_{AB}(t)$, can be imme-

diately calculated as difference between the voltages of the two legs:

$$
\begin{aligned}
v_{AB}(t) &= v_{Ao}(t) - v_{Bo}(t) \\
&= \sum_{n=1}^{R} m\frac{V_{DC}}{2}(d_n - d_{180,n})f_0 \\
&\quad + mV_{DC}\sum_{n=1}^{R}\sum_{k=1}^{\infty}\frac{i}{2\pi k}e^{-i2\pi k f_0(n-1)T_c}\Bigg[e^{-i2\pi k f_0\left(\frac{T_c-d_n}{2}+p_n\right)}\left(e^{-i2\pi k f_0 d_n}-1\right) \\
&\quad - e^{-i2\pi k f_0\left(\frac{T_c-d_{180,n}}{2}+p_{180,n}\right)}\left(e^{-i2\pi k f_0 d_{180,n}}-1\right)\Bigg] \\
&\quad \times \cos(2\pi k f_0 t)
\end{aligned}
\tag{4.20}
$$

The R values of pulses' displacements p_n and $p_{180,n}$ in 4.20 for leg A and leg B, respectively, can be considered as parameters to be optimized. Therefore, there are $2R$ unknown parameters to be determined. By adjusting the pulses that constitute the gate signals for the Full-Bridge switches, it is possible to modify the voltage spectrum to meet specific requirements.

4.3.1 Identification of pulse displacements through an optimization process

After determining the analytical expression of $v_{AB}(t)$, it is essential to identify the optimal pulse displacements to achieve specific targets. Hence, a clear optimization target must be established to determine the optimal pulse positions. The proper displacements of pulses should be determined through a harmonic optimization process. This can be achieved by minimizing a cost function using algorithms or numerical methods to identify the unknown parameters. To enhance the harmonic spectrum of the H-Bridge output voltage, any cost function designed to shape specific harmonics can be employed. WTHD of the converter's voltage is a valuable metric for both the design of output filters and the evaluation of the proposed mod-

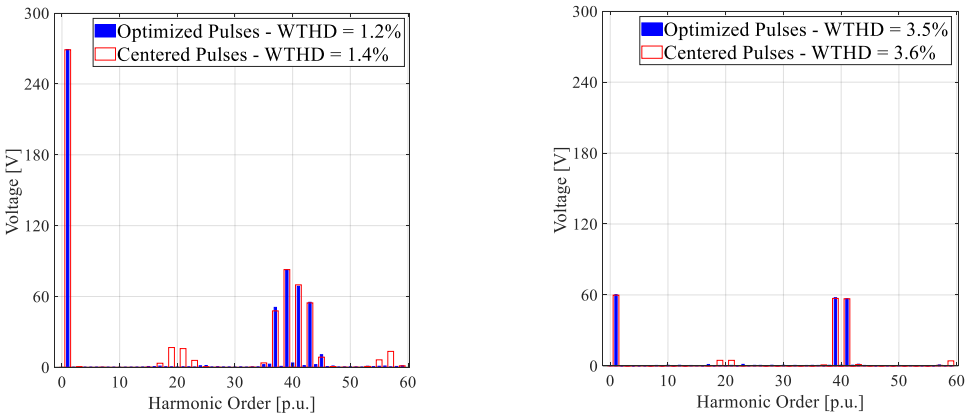
ulation technique. It provides a comprehensive measure of the voltage harmonic content by weighting each harmonic component according to its order, highlighting the impact of lower-order harmonics. Thus, the WTHD of the H-Bridge output voltage can be used as the cost function for the optimization problem:

$$WTHD_{v_{AB}} = \frac{1}{V_{AB,1}} \sqrt{\sum_{k=2}^{\infty} (\frac{V_{AB,k}}{k})^2} \tag{4.21}$$

where $V_{AB,k}$ represents the k-th harmonic component of the Full-Bridge output voltage expressed in 4.20, and $V_{AB,1}$ the fundamental harmonic. An offline optimization process using MATLAB's "*fmincon*" nonlinear programming solver has been employed. It must be pointed out that any optimization technique can be applied to minimize the harmonic content of the voltage waveform, but it is not the primary focus of this work. Since $V_{AB,k}$ depends on the $2R$ displacement values p_n and $p_{180,n}$, minimizing $WTHD_{v_{AB}}$ implies determining $2R$ unknowns. Consequently, a LUT is created, containing a set of $2R$ displacement values, each corresponding to a different value of the above defined variable m (i.e. the normalized value of the fundamental harmonic).

If p_n and $p_{180,n}$ are null vectors, the pulses are centered, resulting in a spectrum for the Full-Bridge output voltage typical of triangular carrier-based PWM. By considering the parameter values reported in Table 4.1 with $R = 20$ and by optimizing $WTHD_{v_{AB}}$ up to the 35-th harmonic, the optimization tool generates a set of 20 non-null displacement values for each leg.

The significant result is illustrated in Figs. 4.8a-4.8b, which display the amplitude spectra of $v_{AB}(t)$ for both centered and optimized gate signals with $m = 0.9$ and $m = 0.2$, respectively. These figures clearly show the reduction of the first harmonic group around the 20-th harmonic component. The harmonic improvement is evident from a notable decrease in $WTHD_{v_{AB}}$, which drops from 1.4% to 1.2%



(a) (b)

Figure 4.8: Comparison of $v_{AB}(t)$ harmonic amplitude spectra when gate signals are centered an optimized. (a) $m = 0.9$. (b) $m = 0.2$.

for $m = 0.9$, with a percentage reduction of 10%; for $m = 0.2$, $WTHD_{v_{AB}}$ drops from 3.6% to 3.5%, determining a percentage reduction of 2.8%. By merely adjusting the position of each driving pulse within its T_c, the harmonic performance of the converter's voltage is enhanced. To further demonstrate the effectiveness of the proposed technique, Fig. 4.9 shows the $WTHD_{v_{AB}}$ values for various values of the variable m. The results clearly indicate a decrease in $WTHD_{v_{AB}}$ when pulses are rearranged. In particular, it is observed the maximum percentage reduction value of 16.6% for $m = 1$. Therefore, the proposed technique offers a novel perspective by adjusting each individual pulse, achieving further improvements beyond the traditional carrier and modulating signal comparison.

4.3.2 Experimental validation

The experimental setup shown in Fig. 4.10 has been used to evaluate the performance of the proposed technique. The adopted Full-Bridge features Si IGBTs RGS50TSX2D from Rohm and feeds an R-L load on its AC side. All the considered parameters for the execution of the experimental tests are outlined in Table 4.1. The proposed technique has been implemented on an FPGA-based controller adopting

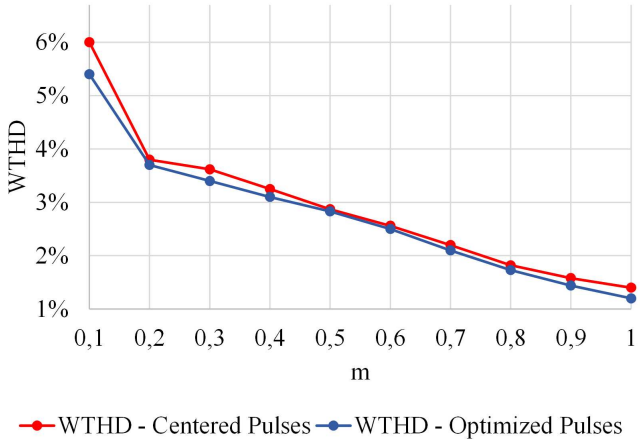


Figure 4.9: Comparison of $WTHD_{v_{AB}}$ values calculated when driving pulses are centered and optimized, for each value of the variable m.

Table 4.1: Experimental setup parameters

Parameter	Symbol	Value
DC input voltage	$V_{DC,x}$ [V]	300
Switching frequency	f_c [Hz]	1000
Fundamental frequency	f_o [Hz]	50
Load resistance	R_{load} [Ω]	40
Load inductance	L_{load} [H]	0.055
Proportional gain	K_p	0.1
Integral gain	K_i	1

the System on Module (SoM) sbRIO-9651. On the DSP of the same control board a closed-loop current control has been implemented.

A. Technique implementation

As previously established, the proposed technique updates the information regarding pulse duration at each control period T_c. When integrated into a closed-loop current control system, both PPM and PWM facilitate the execution of the control action (i.e., the duty cycle) computed by the controller during the preceding control interval T_c. Compared to PWM, PPM offers the additional advantage of incorporating information from the previous control interval to optimize pulse positioning. In contrast, SHE/SHM do not update pulse duration information at every T_c. Instead, in these techniques, the pulse train configuration, including both pulse duration and position, is determined at the fundamental frequency f_o. This configuration is based

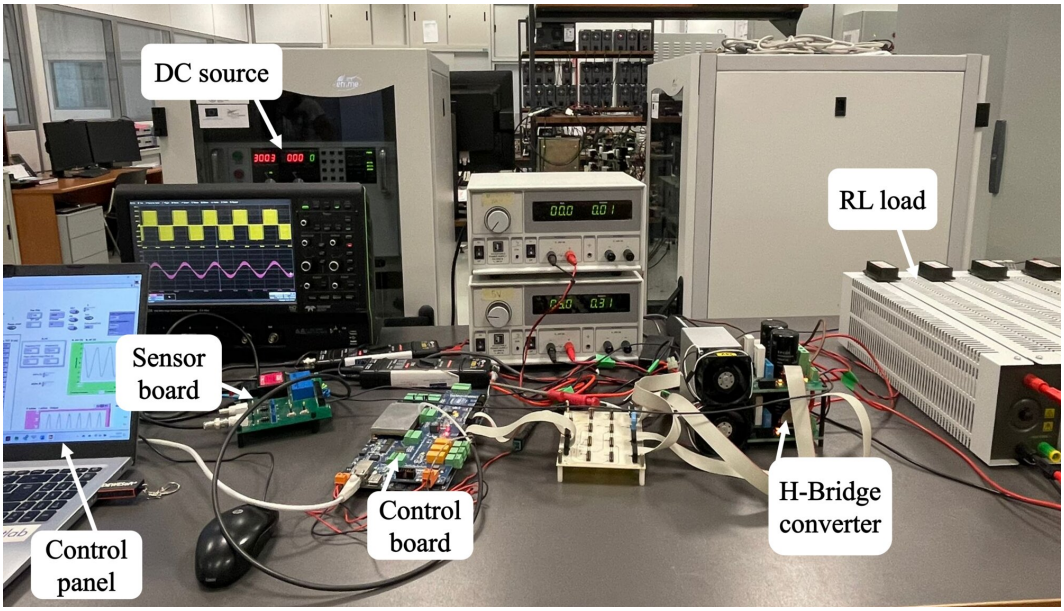
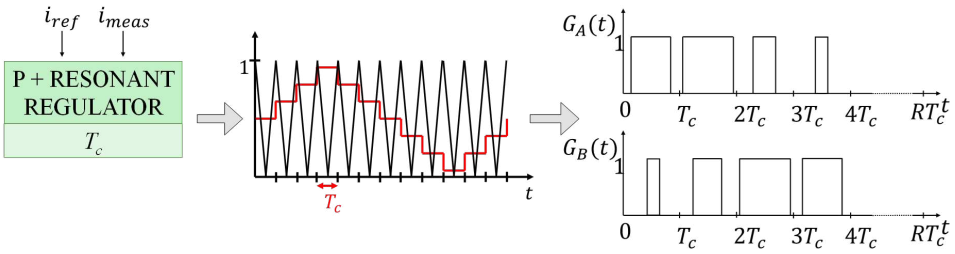


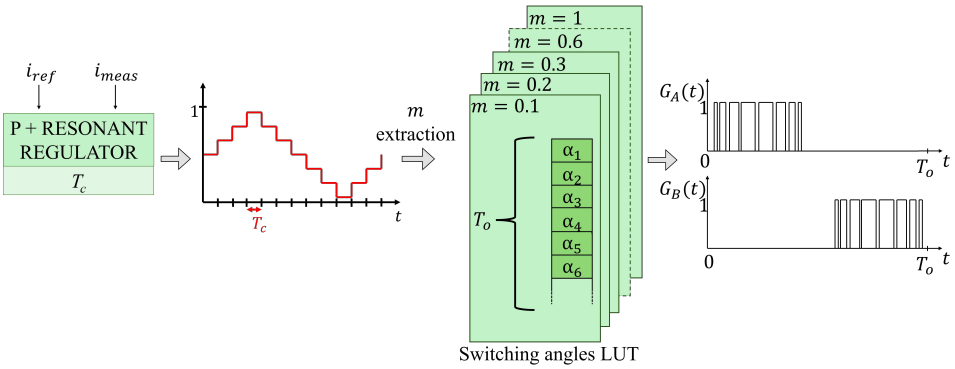
Figure 4.10: Experimental setup.

on the amplitude of the desired fundamental harmonic of the output voltage, which is computed by the controller during the preceding fundamental period T_o.

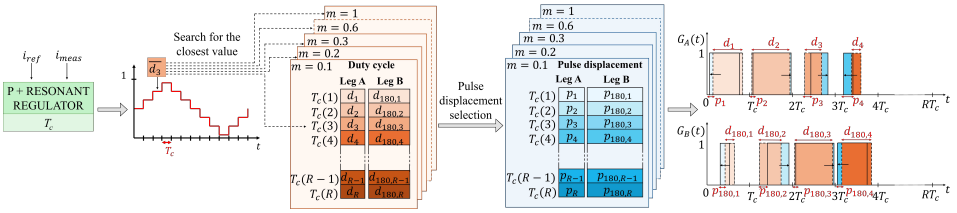
Fig. 4.11 illustrates the closed-loop implementations of the three previously mentioned techniques, with current control managed by a PR regulator. In particular, Fig. 4.11a provides a more detailed view of the implementation of a triangular carrier-based PWM. This method is relatively simple: at each control period T_c, the PR controller determines the updated control action, which corresponds to the discretized sinusoidal modulating signal used for comparison with the triangular carrier. As a result, the system requires only a single T_c interval to respond to a step variation in the current reference. On the other hand, Fig. 4.11b illustrates the implementation of SHE/SHM techniques in conjunction with a PR regulator. These techniques are realized by determining the switching angles through an offline optimization process aimed at minimizing the WTHD of v_{AB} [46, 47]. This approach enables the generation of 20 pulses per fundamental period T_o, consistent with the configurations used for PPM and PWM. As a result, a fair comparison with these benchmark techniques can be performed under equivalent loss conditions.



(a)



(b)



(c)

Figure 4.11: Implementation of the three modulation techniques working in closed-loop mode with a PR controller on the FPGA-based control system. (a) PWM. (b) SHE/SHM. (c) PPM.

The precomputed switching angles for each fundamental period T_o are stored in a LUT, where each value of the modulation index m corresponds to a specific array of angles, as depicted in Fig. 4.11b. However, as previously mentioned, a key limitation of SHE/SHM techniques lies in their dynamic performance. Since the switching angles are precomputed for the entire fundamental period, they must remain constant throughout this interval. Consequently, when a new current reference is set, the system must wait for the complete period T_o to pass before applying

the updated control action, thereby delaying the current adjustment to match the reference value.

In Fig. 4.11c the implementation of the proposed PPM technique is illustrated. Initially, two LUTs are generated, storing arrays of duty cycle values and pulse displacement values obtained from the optimization procedure. For each value of the variable m, distinct arrays containing R duty cycle values are compiled for each leg. This allows the system to generate gate signals for both legs using the precomputed parameters stored in these LUTs.

In closed-loop operation, the controller determines the duty cycle value for a given control period $T_c(k)$. Once the PR regulator computes this duty cycle, the system searches for the closest matching value within the arrays corresponding to $T_c(k)$, specifically in the duty cycle LUT for leg A, as shown in Fig. 4.11c. The identified duty cycle value allows for the determination of the corresponding modulation index m, since it belongs to a specific array associated with a given m. With this value of m, the second LUT can be queried to retrieve the corresponding pulse displacement value at the indexed position within the array for m and $T_c(k)$.

Similar to PWM, the proposed PPM technique enables the execution of the control action within a single T_c interval. Specifically, during $T_c(k)$, once the controller computes the control action to be applied in $T_c(k+1)$, the LUTs can be queried to retrieve the optimal pulse position required for the subsequent T_c interval.

B. Steady-state harmonic performance of PPM

In order to prove the effectiveness of the proposed PPM technique across different scenarios, the steady-state behavior has been evaluated for different m values. Fig. 4.12 shows the voltage and current output waveforms, v_{AB} and i_{AB}, along with their respective spectra for PPM (Fig. 4.13a), PWM (Fig. 4.12b) and SHE/SHE (Fig. 4.12c) when $m = 0.9$. It can be noticed that the first harmonic group disappears when PPM and SHE/SHM are applied, unlike PWM, which fixes pulses within their T_c, leading to worst harmonic performance. Fig. 4.12 also shows

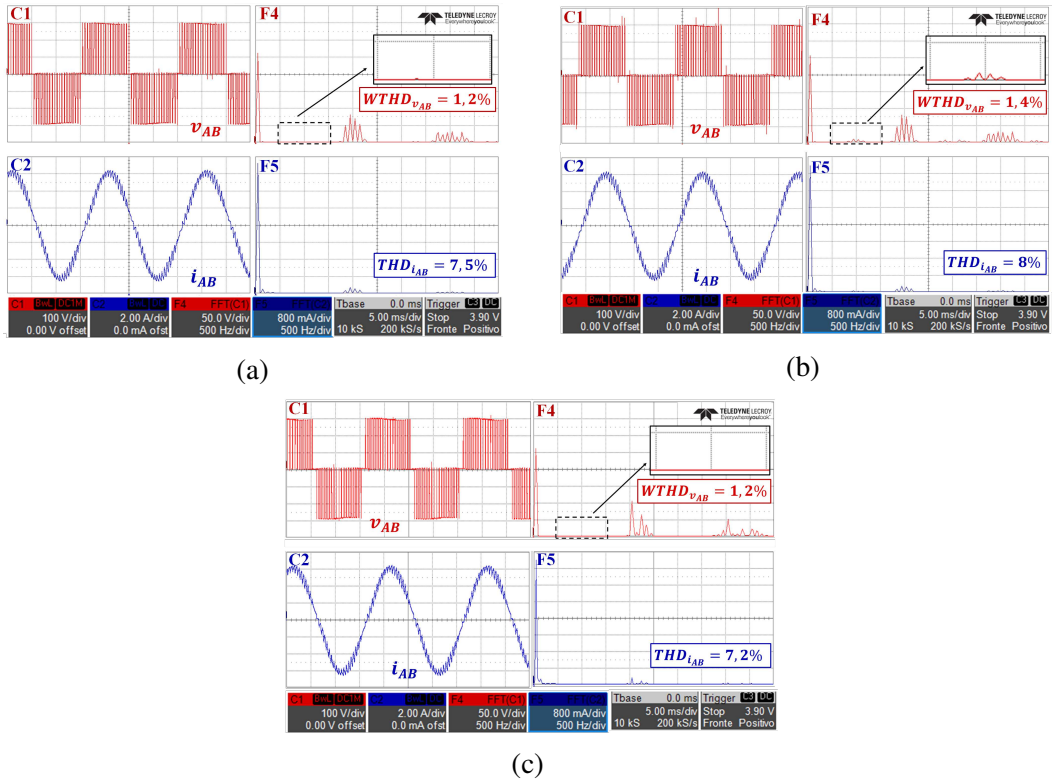


Figure 4.12: Experimental results showing H-Bridge voltage and current waveforms with their harmonic spectra when (a) PPM, (b) PWM and (c) SHE are applied, for $m = 0.9$.

$WTHD_{v_{AB}}$ and $THD_{i_{AB}}$ values for the three cases: PPM achieves $WTHD_{v_{AB}}$=1.2% (like SHE/SHM), whereas PWM reaches 14%; as for $THD_{i_{AB}}$, PPM performs 7.5%, against 8% of PWM.

Fig. 4.13 shows the same results for $m = 0.2$, highlighting that the proposed technique remains effective also for lower values of m. In fact, $WTHD_{v_{AB}}$ drops from 3.6% to 3.5%, while $THD_{i_{AB}}$ drops from 19.9% to 19.3%. Therefore, also for lower values of m the proposed PPM technique performs better than PWM.

Figs. 4.14a-4.14b present a comparative chart of $WTHD_{v_{AB}}$ and $THD_{i_{AB}}$ values for m ranging in the interval [0.1;1], respectively, applying the three aforementioned techniques. The significant result to underline is that PPM consistently achieves superior harmonic performance compared to PWM across all values of m. This aspect is highlighted in the graph of Fig.4.15, where the percentage reduction

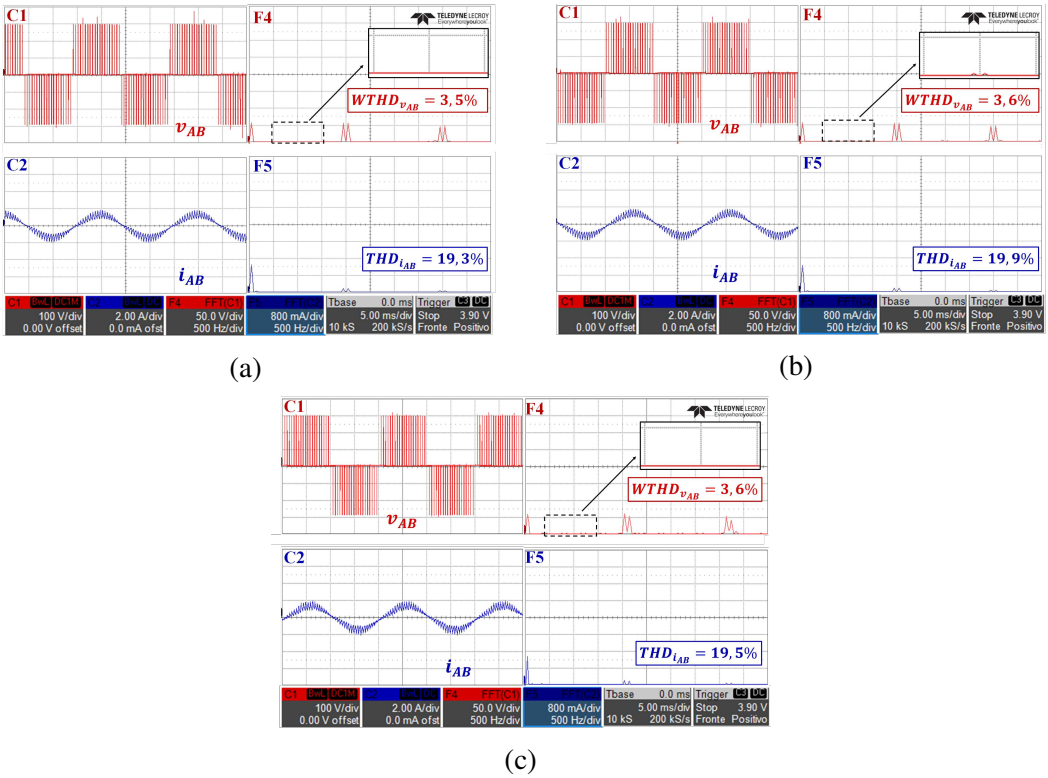


Figure 4.13: Experimental results showing H-Bridge voltage and current waveforms with their harmonic spectra when (a) PPM, (b) PWM and (c) SHE are applied, for $m = 0.2$.

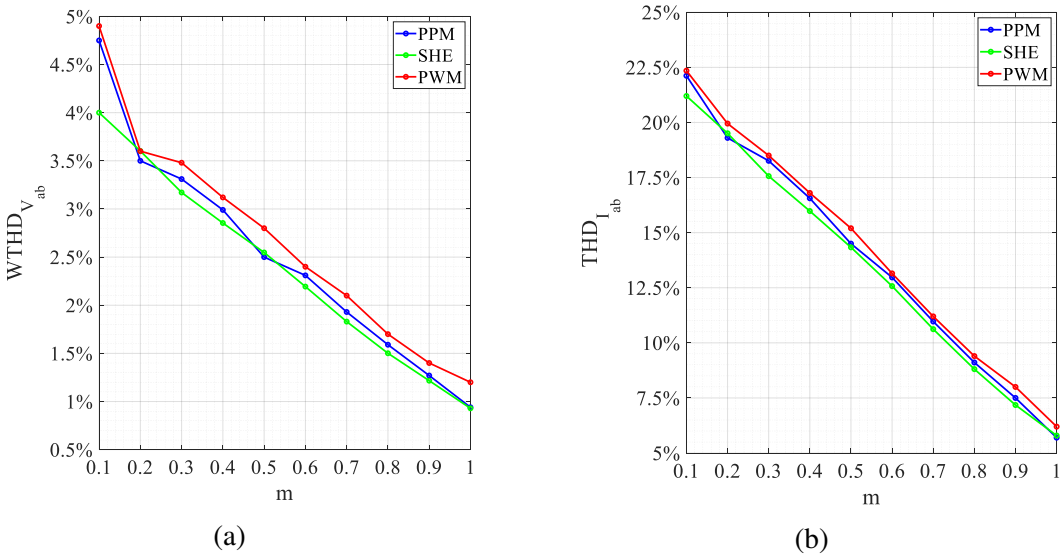


Figure 4.14: Measured (a) $WTHD_{v_{AB}}$ and (b) $THD_{i_{AB}}$ for m ranging in the interval [0.1;1] when PPM, SHE and PWM are applied.

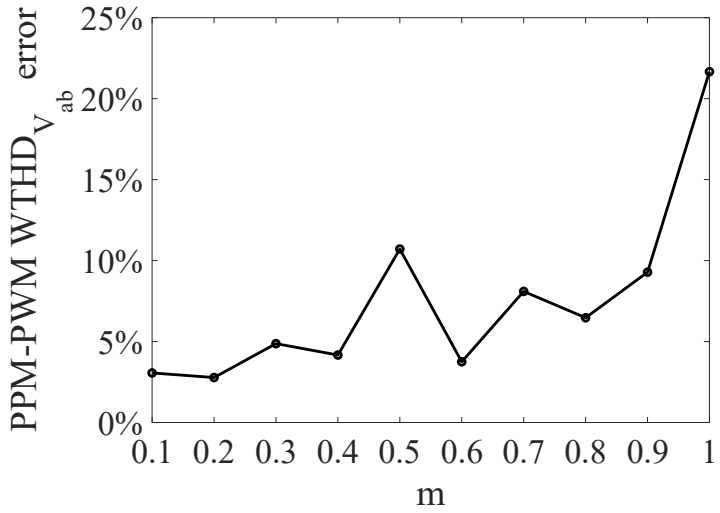


Figure 4.15: Percentage reduction in $WTHD_{v_{AB}}$ using PPM compared to PWM for m ranging in the interval [0.1;1].

of $WTHD_{v_{AB}}$ for m ranging in the interval [0.1;1] is illustrated. It is observed an increasing reduction as m increases, with the maximum percentage decrease of 22% reached at $m = 1$. It can be observed a precise match between simulations previously presented and experimental results, with a good match of $WTHD_{v_{AB}}$ values, proving the effectiveness of the proposed PPM technique in achieving significantly better harmonic performance compared to conventional carrier-based PWM. PPM shows comparable harmonic behavior respect to SHE/SHM, although SHE/SHM techniques perform better, particularly at $m = 0.1$. This can be understood by considering the generation of driving signals for the two techniques. With SHE/SHM, the optimization algorithm determines the optimal switching angles to generate a sequence of pulses within a fundamental period T_o, without being confined within their respective control periods T_c. Conversely, the PPM optimization method constrains each pulse to its designated control period, thereby limiting the potential for harmonic reduction. Despite this restriction, the proposed PPM approach achieves $WTHD_{v_{AB}}$ values that are nearly equivalent to those obtained with SHE/SHM. Moreover, for two modulation indices ($m = 0.2$ and $m = 0.5$), PPM even surpasses SHE/SHM in performance. This outcome is particularly significant given

the stricter pulse placement constraints in PPM compared to SHE/SHM.

C. Dynamic performance of PPM

To highlight the exceptional dynamic performance of the proposed method, the transient response of the system to a step change in the current reference under PPM operation has been analyzed and compared with the system's response when operated using PWM and SHE/SHM. The results are illustrated in Fig. 4.16. Specifically, a step change in the current reference from 1 A to 6 A has been applied, also shown in the oscilloscope snapshot by the green waveform. Fig. 4.16a illustrates

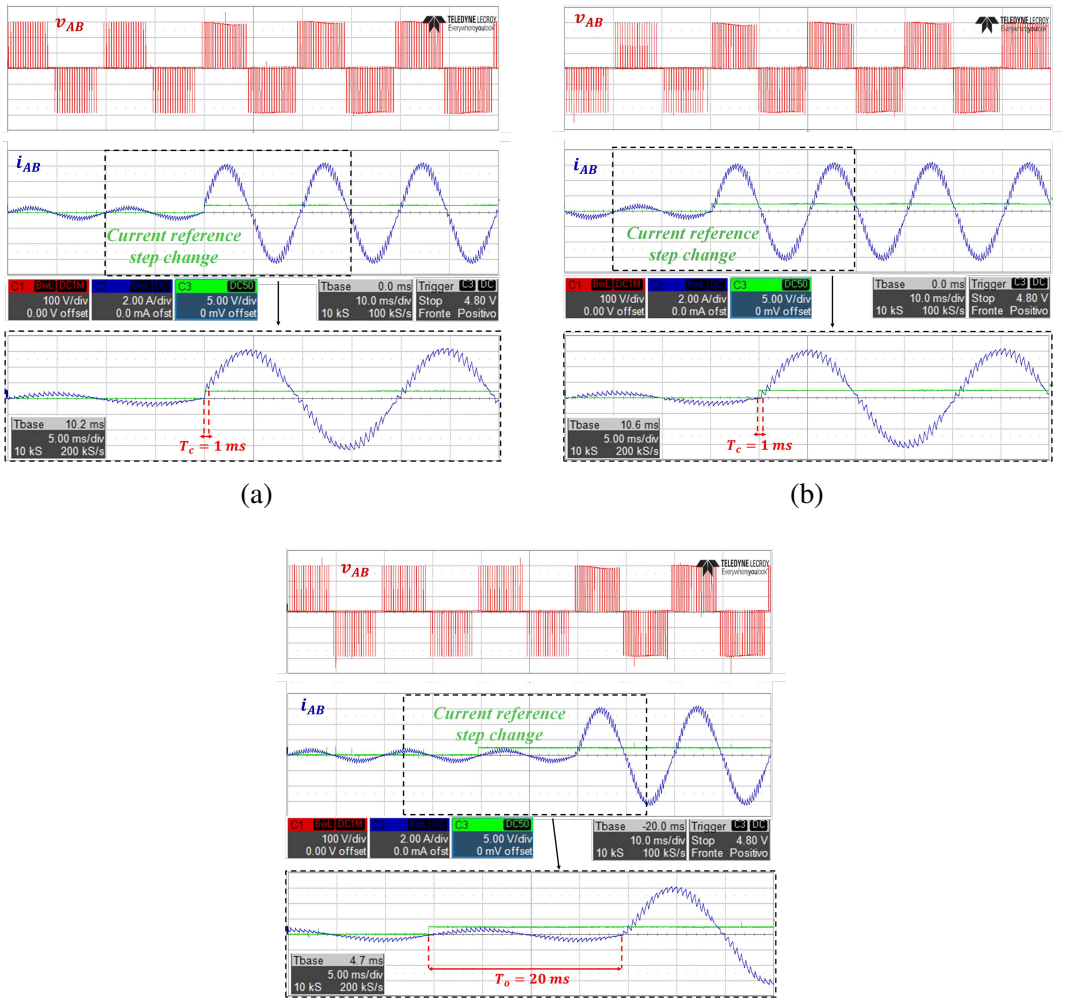


Figure 4.16: Dynamic behavior of Full-Bridge voltage and current waveforms when a current reference step from 1 A to 6 A is applied, with a detail of the current signal when (a) PPM, (b) PWM, and (c) SHE are applied.

the exceptional dynamic performance of PPM, showing a rapid response following the step change in the current reference. Within a single T_c (1 ms), the controller effectively adjusts the current amplitude to match the reference. This rapid adaptation is achieved by updating duty cycle values at each T_c, instantly selecting the appropriate pulse displacement and generating the corresponding gate signal, leading to an immediate waveform adjustment. Similarly, as shown in Fig. 4.16b, under PWM operation, the converter output current promptly tracks the reference after the step change, achieving amplitude regulation within a single T_c. This confirms the fast dynamic response of PWM, despite its previously mentioned harmonic drawbacks. In contrast, Fig. 4.16c highlights the poor dynamic response of SHE/SHM, where the system requires an entire period T_o (20 ms) to adjust the converter current after the step change. This delay is due to the inherent limitations of SHE/SHM, as discussed earlier.

Table 4.2 summarizes the harmonic and dynamic performance of the three compared techniques, clearly highlighting the superiority of the proposed PPM strategy.

4.4 Case study: Common-Mode Voltage Reduction in Three-Phase Inverters

Three-phase two-level voltage-source inverters play a fundamental role in modern power electronics, particularly in applications such as motor drives and photovoltaic systems, where their efficiency and flexibility are highly valued. Despite their widespread use, these inverters are prone to generating common-mode voltage

Table 4.2: Summary Comparison

Modulation Strategy	$WTHD_{v_{AB}}$ for $m = 0.9$	Dynamic Time Response [ms]
PWM	1.4%	1
SHE	1.2%	20
PPM	1.2%	1

(CMV), a phenomenon that can cause serious drawbacks. In motor drives, CMV is a known contributor to premature bearing failure, while in photovoltaic installations it can accelerate panel aging due to leakage currents. Numerous mitigation strategies have been proposed from hardware modifications to advanced control algorithms, but many of these solutions introduce new challenges, including increased system complexity or degradation of output waveform quality.

In this context, the advantages of the innovative PPM are leveraged also to address the CMV issue from a control-oriented perspective. As carefully described previously, the core idea of the method lies in optimizing the position of each switching pulse within its control period, thereby increasing the available degrees of freedom and allowing for more effective harmonic and common-mode voltage control. A detailed analytical derivation of the CMV associated with PPM is provided, forming the basis for an optimization framework capable of determining the pulse positions that minimize CMV. Importantly, the proposed technique achieves CMV reduction without compromising the quality of the output waveforms. On the contrary, it delivers a simultaneous improvement in current harmonic distortion, outperforming conventional methods such as the phase-shift approach. Experimental results discussed in this chapter confirm the effectiveness of the proposed method, highlighting the potential of PPM-based strategy to overcome long-standing limitations in inverter operation and suggest a new direction for high-performance and reliability-oriented converter design.

4.4.1 Overview of existing methods for common-mode voltage mitigation

In recent years, the rapid evolution of power electronics technologies, together with the growth of renewable energy and energy storage solutions, has significantly influenced the structure of modern energy systems. These innovations have been pivotal

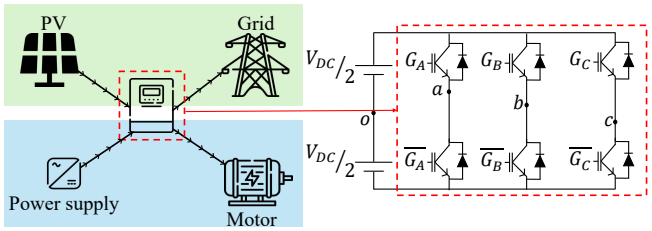


Figure 4.17: Scheme of a three-phase, two-level VSI designed for applications in grid-connected systems and motor drives.

in the global transition towards cleaner energy, aiming to reduce reliance on fossil fuels and minimize greenhouse gas emissions [48], [49]. Power converters now serve a wide spectrum of industrial applications, ranging from grid-tied systems for renewable integration and storage to electric motor drives used in equipment such as fans, pumps, conveyors, and electric vehicles. Within this technological ecosystem, the three-phase two-level voltage-source inverter (VSI), illustrated in Fig.4.17, plays a foundational role [50–52].

A key feature of these inverters is the use of PWM strategy, which allows precise control of the switching states to synthesize desired output voltages with high fidelity. Despite its widespread use, traditional PWM introduces a significant drawback: the generation of CMV, which remains a persistent issue in many applications. In the case of a conventional three-phase two-level VSI, CMV is defined as the voltage between the neutral point of the load and the midpoint of the inverter's DC link (o), and is mathematically described as:

$$\mathbf{CMV(t)} = \frac{v_{ao}(t) + v_{bo}(t) + v_{co}(t)}{3} \tag{4.22}$$

where v_{ao}, v_{bo}, and v_{co} represent the instantaneous phase-to-midpoint voltages. In motor drive systems, elevated CMV levels combined with rapid switching transitions can induce bearing currents that lead to premature motor degradation. Moreover, CMV is the major source of electromagnetic interference (EMI), which can trigger faults in the inverter itself or disrupt nearby electronic devices. In pho-

tovoltaic (PV) applications, CMV contributes to the generation of leakage currents, which reduce overall system efficiency and weaken the electrical insulation. Prolonged exposure to such leakage currents accelerates the aging process of PV components, ultimately decreasing the operational life of the entire installation [53], [54].

This study centers on investigating both passive and active strategies for minimizing or mitigating CMV. Passive techniques typically involve incorporating additional hardware components, which significantly increase the overall cost and structural complexity of the drive system [55], [56]. Although some recent works, such as [57] and [58], propose solutions that avoid extra passive components, they necessitate alterations to the inverter topology, making them less feasible for practical applications. In contrast, active methods strive to reduce CMV by modifying the switching patterns of conventional two-level inverters without increasing system cost. Among the various reduced common-mode voltage PWM (RCMV-PWM) techniques explored in the literature [59], [60], the Active Zero-State PWM (AZSPWM) and Near-State PWM (NSPWM) stand out for their relative simplicity and ease of implementation. These methods operate by injecting a zero-sequence component (v_o) into the reference voltage signals, effectively vertically shifting the modulating waveforms relative to the carrier signal. This manipulation alters the switching instants and contributes to improving the CMV profile [61–63]. However, despite their apparent effectiveness, these approaches are inherently limited by a lack of flexibility, as the only adjustable parameter is the shape of the modulating signal itself [64]. This limitation constrains the achievable performance enhancements, particularly in applications demanding more aggressive CMV suppression. A more sophisticated solution is introduced in [65], where a novel space vector PWM (SVPWM) approach is developed to control CMV. While this method can yield better results, it introduces additional complexity due to its dependence on the modulation index, complicating its practical deployment.

It is worth noting that in three-phase VSIs, not only the modulation signals can be designed and modified, but also the carrier signals for each phase can be independently defined. Carriers can be phase-shifted relative to each other or operated at varying frequencies. For instance, [66] presents a uniformly sampled sine-triangle PWM scheme using interleaved carriers for each phase to enhance CMV performance, with or without third-harmonic injection. Similarly, studies such as [67–69] analyze CMV mitigation by employing unconventional carrier phase-shifting techniques. A more advanced strategy is proposed in [70], which leverages a detailed mathematical framework to determine optimal phase-shift angles that minimize CMV harmonic content. Among phase-shifted PWM (PS-PWM) methods, this approach proves to be the most effective due to its analytical derivation. By adjusting carrier signals shifting, this method enables the synthesis of a wide range of PWM patterns tailored to suppress CMV.

Nonetheless, the main drawback of PS-PWM schemes lies in their structural rigidity, as each pulse within the control interval is uniformly shifted while maintaining symmetrical distribution, limiting further adaptability.

4.4.2 Proposed PPM-based CMV reduction approach

This study introduces a fundamentally new approach to enhance the harmonic profile of the CMV in three-phase VSIs. The proposed methodology is grounded in the PPM strategy first outlined in [71], which enables direct generation of control signals for power electronic converters. By doing so, it eliminates the traditional requirement for comparing a carrier waveform with a modulating signal. Unlike standard PWM methods, where pulses are constrained to fixed positions within each sampling interval, the PPM technique strategically places gate pulses of specific width within each control cycle T_c, optimizing harmonic performance and offering fast dynamic response.

The core concept of PPM is exemplified in Fig. 4.5 [71], which depicts a simplified waveform $x(t)$ composed of four pulses. While both centered and time-shifted pulses maintain the same duty cycle, thus preserving the fundamental frequency, the ability to independently adjust each pulse's timing represents a shift in modulation philosophy. This flexibility bypasses the limitations of traditional carrier-based methods and introduces a broader modulation space, enabling targeted objectives such as CMV reduction to be more efficiently achieved.

To determine optimal pulse timing, PPM employs LUTs, drawing a parallel with SHE/SHM techniques. However, unlike SHE/SHM, which typically operate over the fundamental period T_o, PPM maintains a fixed switching frequency f_c and recalculates pulse placement for every control cycle T_c. This allows for faster responsiveness, similarly to PWM, while preserving the harmonic tuning capabilities of SHE/SHM. Additionally, the ability to vary the position of each pulse within T_c enhances harmonic control beyond the capabilities of conventional PWM. This work leverages these advantages to target CMV minimization and its associated leakage currents. To facilitate this, an analytical expression for CMV has been derived based on Fourier Series expansion, explicitly formulated in terms of the pulse positions as variable parameters [72–74]. The theoretical framework builds upon the detailed spectral analysis of PPM pulse sequences presented in the previous chapter [71]. Each individual pulse within a control interval T_c, forming part of the overall pulse train within one output period T_o, is independently analyzed in the frequency domain to extract its Fourier components. The full signal sent to the gate drivers is then reconstructed from the sum of these components. The primary innovation introduced by the PPM approach lies in treating the temporal displacement of each pulse as a design variable within the Fourier representation, thus enabling modulation schemes that explicitly target performance criteria like CMV attenuation. To realize this goal, an offline optimization process is applied. This involves minimizing a specifically defined objective function, namely, the root mean square

(RMS) value of the CMV, while respecting predefined constraints. This optimization determines the pulse positions that yield the lowest CMV distortion, ensuring both theoretical and practical performance benefits.

a. PPM-based CMV analytical expression

In the previous chapter, an in-depth mathematical framework has been developed to analyze the behavior of individual pulses within their control periods, resulting in a powerful analytical tool capable of directly synthesizing gate or control signals as pulse trains with variable pulse positions. This analytical foundation plays a central role in the present work, serving as the theoretical basis for the proposed modulation strategy. In this study, the methodology is applied to a three-phase voltage source inverter, as illustrated in Fig. 4.17, with the primary objective of enhancing the CMV performance.

To regulate the inverter and generate three sinusoidal output voltages, it is necessary to produce three distinct gate signals, one for each inverter leg. Traditionally, in PWM schemes, this is achieved by comparing three sinusoidal reference waveforms, shifted by 120°, with triangular carrier signals. These comparisons yield fixed-position pulses centered within each sampling interval T_c. However, this inherent constraint of fixed pulse positioning limits the achievable performance, particularly in applications requiring enhanced CMV control. The proposed technique addresses this limitation by allowing each gate pulse to be optimally placed within its corresponding sampling interval. To apply the PPM approach, the duty-cycle values for each control interval T_c must first be calculated by the controller. Using these values, the output leg voltages ($v_{ao}(t)$, $v_{bo}(t)$, and $v_{co}(t)$) can then be expressed in closed-form, accounting explicitly for the temporal displacement of each pulse, as shown in 4.23, 4.24, and 4.25.

In this formulation, the arrays $d_{n,A}$, $d_{n,B}$, and $d_{n,C}$ contain the duty-cycle val-

ues for each control interval and correspond to phases A, B, and C, respectively. The modulation index m quantifies the amplitude of the fundamental component of the output waveform relative to $V_{DC}/2$ [18], while f_o denotes the fundamental frequency, and R represents the ratio between the switching frequency and the fundamental frequency. The index n identifies the pulse number, k specifies the harmonic order, and V_{DC} is the DC-link voltage. Meanwhile, the vectors $p_{n,A}$, $p_{n,B}$, and $p_{n,C}$ hold the displacement values of the gate pulses for each inverter leg, referenced with respect to their nominal centered positions.

According to 4.22, the CMV can be explicitly derived, and its analytical expression is provided in 4.26. It is evident from this expression that CMV is directly influenced by the positional shifts of the gate pulses in each inverter leg. These displacement values become the critical unknowns in the optimization process aimed at minimizing CMV. The method used to solve this optimization problem is discussed in the following paragraph.

b. PPM-based CMV optimization

Once the harmonic formulation of the CMV, expressed as a function of the pulse positions within their respective control intervals T_c, has been established, it becomes necessary to define a suitable optimization objective to guide the determination of optimal pulse displacements. The chosen objective must reflect the specific performance goals of the system under consideration.

In this context, a widely adopted criterion for assessing and mitigating the impact of CMV, particularly in applications such as PV systems and electric drives, is the RMS value of the CMV waveform. This metric serves as a figure of merit for quantifying both the stress imposed on PV arrays and leakage currents introduced into bearings in drives circuits. Accordingly, the objective function for the optimization problem is defined as follows:

$$
\begin{aligned}
v_{ao}(t) = & \sum_{n=1}^{R} m\frac{V_{DC}}{2} d_{n,A} f_o - m\frac{V_{DC}}{2} \\
& + mV_{DC} \sum_{n=1}^{R} \sum_{k=1}^{+\infty} \frac{i}{2\pi k} e^{-i2\pi k f_o \left(\frac{T_c - d_{n,A}}{2} + p_{n,A} + (n-1)T_c\right)} \\
& \cdot \left(e^{-i2\pi k f_o d_{n,A}} - 1\right) \cos(2\pi k f_o t)
\end{aligned} \tag{4.23}
$$

$$
\begin{aligned}
v_{bo}(t) = & \sum_{n=1}^{R} m\frac{V_{DC}}{2} d_{n,B} f_o - m\frac{V_{DC}}{2} \\
& + mV_{DC} \sum_{n=1}^{R} \sum_{k=1}^{+\infty} \frac{i}{2\pi k} e^{-i2\pi k f_o \left(\frac{T_c - d_{n,B}}{2} + p_{n,B} + (n-1)T_c\right)} \\
& \cdot \left(e^{-i2\pi k f_o d_{n,B}} - 1\right) \cos(2\pi k f_o t)
\end{aligned} \tag{4.24}
$$

$$
\begin{aligned}
v_{co}(t) = & \sum_{n=1}^{R} m\frac{V_{DC}}{2} d_{n,C} f_o - m\frac{V_{DC}}{2} \\
& + mV_{DC} \sum_{n=1}^{R} \sum_{k=1}^{+\infty} \frac{i}{2\pi k} e^{-i2\pi k f_o \left(\frac{T_c - d_{n,C}}{2} + p_{n,C} + (n-1)T_c\right)} \\
& \cdot \left(e^{-i2\pi k f_o d_{n,C}} - 1\right) \cos(2\pi k f_o t)
\end{aligned} \tag{4.25}
$$

$$
\begin{aligned}
CMV(t) = & \sum_{n=1}^{R} m\frac{V_{DC}}{2} f_o \frac{d_{n,A} + d_{n,B} + d_{n,C}}{3} - m\frac{V_{DC}}{2} \\
& + \frac{mV_{DC}}{3} \sum_{n=1}^{R} \sum_{k=1}^{+\infty} \Big(\frac{i}{2\pi k} e^{-i2\pi k f_o \left(\frac{T_c - d_{n,A}}{2} + p_{n,A} + (n-1)T_c\right)} \left(e^{-i2\pi k f_o d_{n,A}} - 1\right) \\
& + \frac{i}{2\pi k} e^{-i2\pi k f_o \left(\frac{T_c - d_{n,B}}{2} + p_{n,B} + (n-1)T_c\right)} \left(e^{-i2\pi k f_o d_{n,B}} - 1\right) \\
& + \frac{i}{2\pi k} e^{-i2\pi k f_o \left(\frac{T_c - d_{n,C}}{2} + p_{n,C} + (n-1)T_c\right)} \left(e^{-i2\pi k f_o d_{n,C}} - 1\right) \Big) \cos(2\pi k f_o t).
\end{aligned} \tag{4.26}
$$

$$RMS_{CMV} = \sqrt{\sum_{n=1}^{R} \sum_{k=1}^{+\infty} CMV(t)^2} \tag{4.27}$$

To minimize this quantity, an offline numerical optimization procedure has been implemented using MATLAB's *fmincon* solver for constrained nonlinear programming [75]. Nonetheless, the choice of optimization algorithm is not fundamental to the validity of the proposed control strategy; alternative techniques could equally be employed, depending on the specific requirements of the application. In the implemented procedure, constraints are imposed to ensure that each pulse remains confined within its assigned control period T_c. Consequently, the displacement of each pulse is bounded such that it does not overlap into adjacent periods. The maximum permissible displacement, either in advance or delay, is defined as in 4.17, in the previous chapter. Since the CMV expression is a function of three distinct arrays of pulse displacements, each comprising R optimization variables, the overall problem involves $3R$ unknowns. The optimization process is performed iteratively for each selected value of the modulation index m, and the resulting optimized pulse displacements are subsequently employed to generate the PPM control signals. These signals are then used in the experimental validation of the proposed methodology, as described in the following paragraphs.

4.4.3 Experimental validation

The experimental evaluation of the proposed PPM-based CMV reduction strategy has been conducted using the setup illustrated in Fig. 4.18.

The three-phase inverter used in the setup is based on silicon IGBT technology and is equipped with Rohm's RGS50TSX2D Si-IGBT modules. The inverter supplies a passive R-L load on the AC side, replicating typical operating conditions. All electrical and control parameters relevant to the experiments are comprehensively summarized in Table 4.3. As in the previous chapter with the H-bridge configura-

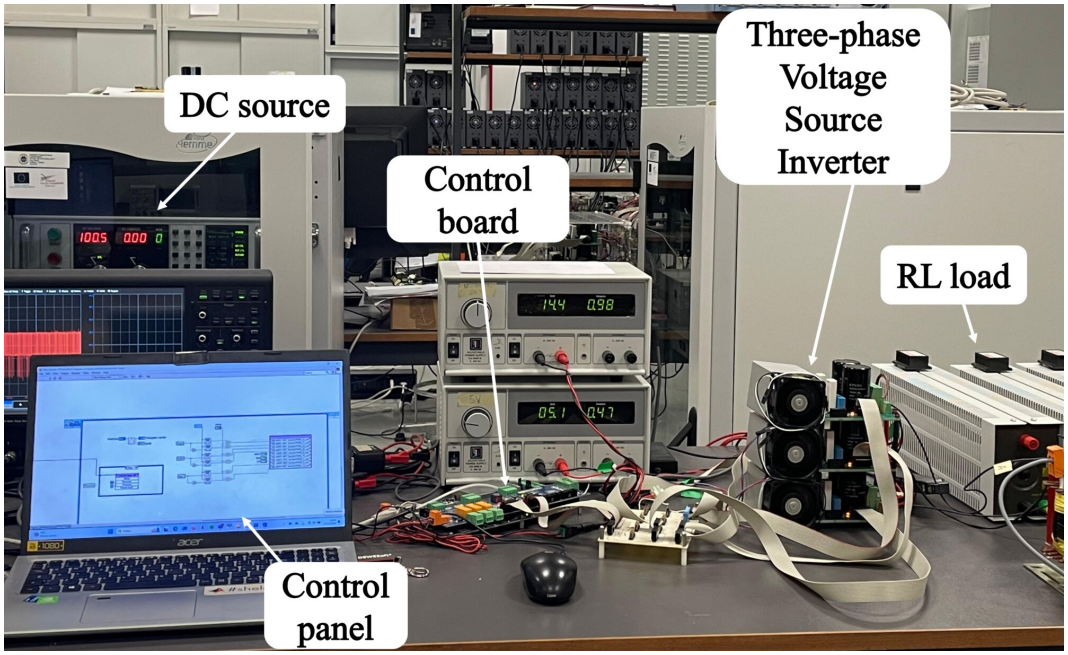


Figure 4.18: Experimental test bench.

Table 4.3: Experimental Setup Parameters

Parameter	**Symbol [Unit]**	**Value**
DC link voltage	V_{DC} [V]	600
Switching frequency	f_c [Hz]	1000
Fundamental frequency	f_o [Hz]	50
Load resistance	R_{load} [Ω]	50
Load inductance	L_{load} [mH]	6
Modulation index	m [–]	0.9
Dead time	– [μs]	1
Rated power	P_n [kW]	10

tion, the real-time implementation of the modulation algorithm has been carried out using a FPGA-based control platform. Specifically, the proposed method has been deployed on a National Instruments sbRIO-9651 System-on-Module (SoM), which integrates an FPGA and a dual-core processor, enabling deterministic control and high-speed computation required for precise pulse positioning.

a. Experimental comparison between PPM technique and established methods for CMV reduction

To rigorously evaluate the effectiveness of the proposed PPM strategy in mitigating CMV, a comprehensive comparative analysis has been conducted against several established modulation techniques, namely conventional PWM, AZSPWM, NSPWM, and PS-PWM. All tests have been performed under identical operating conditions, with a constant frequency ratio $R = 20$, in order to ensure a uniform switching frequency and, consequently, comparable switching losses across all methods, and using 80% of the rated power ($10kW$). For the PPM case, the inverter control signals have been generated using pulse positions derived from the optimization procedure aimed at minimizing the RMS_{CMV}, as described in the previous paragraph. The implementation of the PPM algorithm is based on the framework extensively discussed and validated in the previous chapter [71], which provides a detailed account of its formulation and practical deployment. Since AZSPWM and NSPWM inherently rely on space vector modulation techniques incorporating third-harmonic injection, a fair comparison requires that third-harmonic injection be consistently applied across all modulation strategies. Accordingly, PWM and PS-PWM have been adapted by superimposing a third-harmonic component into the modulating signals. For PPM, a custom-designed LUT has been constructed to embed duty-cycle values obtained from a third-harmonic-injected sinusoidal PWM. This approach ensures that all methods under evaluation benefit from the improved DC bus utilization typically associated with third-harmonic injection.

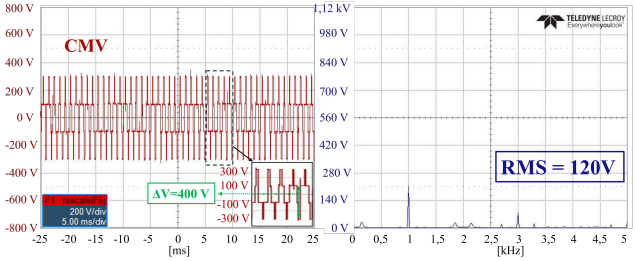
The results of the experimental comparison are presented in Fig. 4.19, which show both the time-domain CMV waveforms and the corresponding harmonic spectra for each modulation technique at a modulation index of $m = 0.9$. To quantify the CMV reduction effectiveness, the RMS values have been computed for each case. As anticipated, the RCMV-oriented techniques (Figs. 4.19b-4.19e) yield bet-

ter results than conventional PWM (Fig. 4.19a), which records a RMS_{CMV} of 120 V. Among the evaluated methods, AZSPWM offers limited improvement, reducing the RMS to 110 V. More substantial reductions are achieved by NSPWM and PS-PWM, with RMS values of 91 V and 68.1 V, respectively. Notably, PS-PWM exhibits significant attenuation of the carrier-related harmonics.

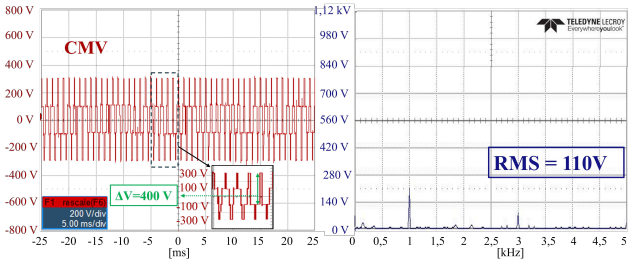
The PPM technique, illustrated in Fig. 4.19e, demonstrates the highest performance in CMV suppression, achieving an RMS value of only 65.8 V. Furthermore, the amplitude of the dominant carrier harmonic is reduced to 47 V, underscoring the superior spectral shaping capabilities of the method. Compared to PS-PWM, this represents a 3.4% additional reduction in RMS_{CMV}, highlighting a tangible advancement in harmonic quality. An interesting spectral observation is the absence of the typical harmonic clustering found in conventional techniques. In the case of PPM, the harmonic energy is spread across a broader frequency range, an expected consequence of the nonuniform pulse positioning mechanism. However, this spectral dispersion is not detrimental. On the contrary, the primary objective, namely, the suppression of leakage currents, remains fully addressed. This is because leakage current is closely tied to the time derivative of CMV (dv/dt); minimizing abrupt voltage variations directly contributes to reduced leakage current peaks, thereby protecting critical components such as motor bearings and photovoltaic modules.

To further support this analysis, Fig. 4.19 highlights the ΔV values (in green) for each method. It becomes immediately evident that PPM is the only technique capable of limiting CMV swings to 200 V. All other methods exhibit $\Delta V = 400$ V, resulting in considerably higher associated leakage currents.

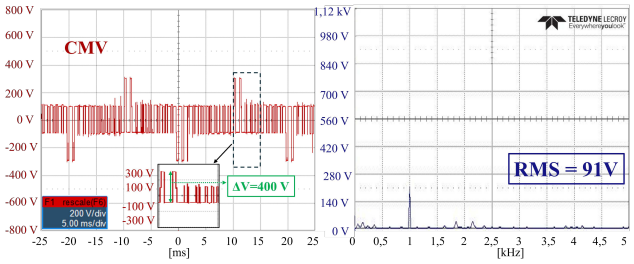
The exceptional results achieved by the PPM approach are primarily attributed to its intrinsic capability to independently control the position of each individual switching pulse. This unique feature significantly increases the modulation system's degrees of freedom, allowing a more precise and effective shaping of the inverter's output waveform and associated CMV profile. As such, PPM offers a fundamen-



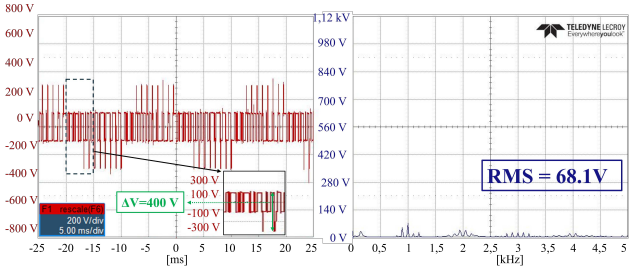
(a)



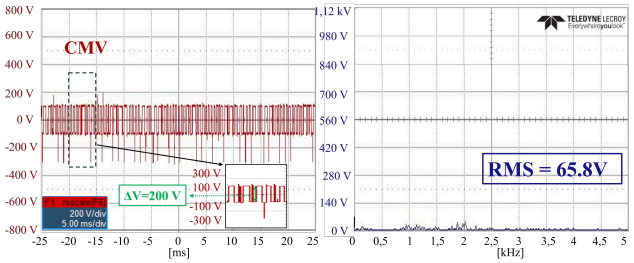
(b)



(c)



(d)



(e)

Figure 4.19: Experimental results showing CMV and its harmonic spectrum when (a) PWM, (b) AZSPWM, (c) NSPWM, (d) PS-PWM, and (e) PPM are applied, for $m = 0.9$.

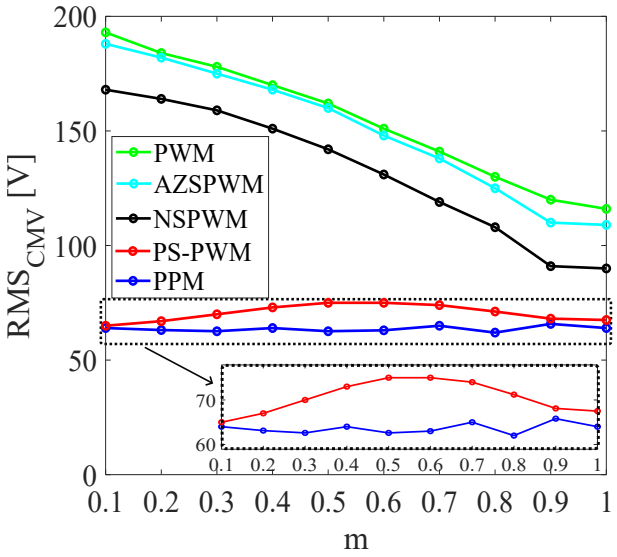


Figure 4.20: Experimentally measured RMS_{CMV} values for PPM, PWM, PS-PWM, AZSPWM, and NSPWM techniques across all modulation index (m) values.

tally novel and highly effective solution for CMV mitigation, clearly outperforming conventional techniques currently available in the literature.

To assess the robustness of the proposed PPM-based CMV mitigation strategy across varying operating conditions, a comprehensive set of experimental measurements has been performed. In particular, the RMS values of the resulting CMV have been recorded over the full modulation index range $m \in [0.1; 1]$ for each of the compared modulation techniques, as reported in Fig. 4.20. The results reveal that AZSPWM and NSPWM exhibit a behavior analogous to conventional PWM, wherein the RMS CMV decreases progressively as m increases. Conversely, PS-PWM and PPM demonstrate a much more stable RMS profile, remaining within the $60V–75V$ range throughout the entire modulation index spectrum. A closer inspection of the magnified portion of Fig. 4.20 highlights that PPM consistently yields lower RMS values compared to PS-PWM, particularly in the mid-range values of m. This improvement is of considerable practical relevance, especially in drive applications where the modulation index varies dynamically across its entire range during operation.

Although PS-PWM and PPM present comparable levels of performance in terms

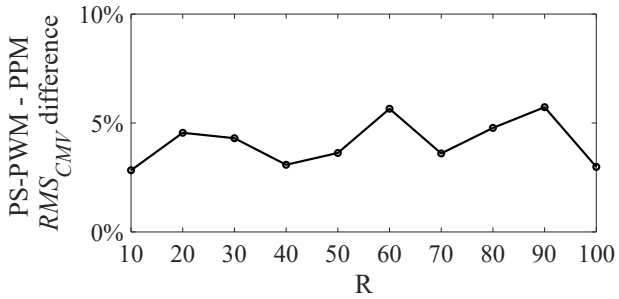


Figure 4.21: Percentage RMS_{CMV} difference between PS-PWM and PPM techniques across different frequency ratio (R) values.

of average RMS values, their CMV waveform characteristics differ significantly. As shown previously in Fig. 4.19, the PPM method inherently constrains the common-mode voltage to within the interval $[-V_{DC}/6, +V_{DC}/6]$, with rare excursions toward $\pm V_{DC}/2$. In contrast, PS-PWM typically produces a CMV profile oscillating across the full range $[-V_{DC}/2, +V_{DC}/2]$. This distinction is not merely qualitative but directly impacts application-level metrics: limiting the $\mathrm{d}v/\mathrm{d}t$ of the CMV reduces leakage currents, which are known to contribute to accelerated aging in motor bearings and PV panel degradation, depending on the use case. The CMV waveforms presented in Fig. 4.19 confirm that PPM is the only approach among those evaluated that successfully restricts the steepness of CMV transitions, thus enhancing system reliability.

Furthermore, to explore whether the superior CMV suppression observed with PPM remains effective at higher switching frequencies, a numerical study has been conducted. The results, summarized in Fig. 4.21, compare the percentage error in simulated RMS_{CMV} values between PPM and PS-PWM as the frequency ratio R increases. The error remains bounded between 1% and 6%, with minima observed around $R = 40$ and $R = 100$. Crucially, these findings confirm that PPM consistently outperforms PS-PWM even as the switching frequency increases, suggesting that the method remains advantageous within a broad practical operating range.

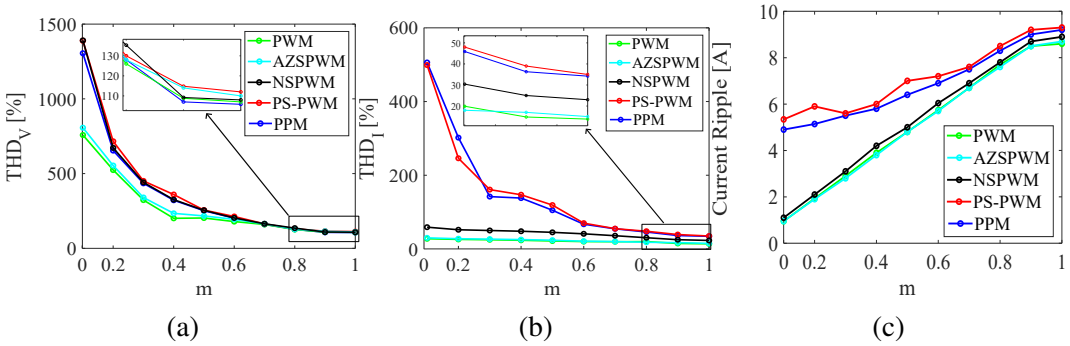


Figure 4.22: Experimental evaluation of output voltage THD (a), current THD (b), and current ripple (c) for different modulation strategies.

b. Simultaneous optimization of CMV and inverter current - PS-PWM and PPM comparison

The reduction of the RMS value of the CMV waveform is widely acknowledged to introduce a degradation in the harmonic quality of the inverter output currents, as reported in previous studies [70, 76–78]. To systematically investigate this effect, experimental measurements have been conducted for each of the modulation strategies discussed, evaluating the total harmonic distortion of the output voltage (THD_V), the total harmonic distortion of the output current (THD_I), and the output current ripple across a modulation index range of $m \in [0.1; 1]$. The results of these measurements are presented in Figs. 4.22a–4.22c. As anticipated, an inverse correlation is observed between CMV suppression and the harmonic performance of the output waveforms: modulation strategies that achieve better CMV mitigation tend to exhibit higher output distortion. Nonetheless, although the proposed PPM technique demonstrates the greatest effectiveness in reducing CMV, as previously demonstrated, it does not incur the worst deterioration in output current quality. On the contrary, Figs.4.22b–4.22c reveal that PS-PWM produces the highest THD_I and the most pronounced current ripple, indicating a poorer output performance relative to PPM.

To address this limitation, it becomes advantageous to refine the PPM technique

by incorporating output current quality (specifically, THD_I) into the optimization framework. While AZSPWM and NSPWM achieve CMV reduction by injecting v_o into the modulating signal, PS-PWM and PPM differ fundamentally, as they rely on optimization-based approaches. Therefore, extending the optimization criterion beyond the sole minimization of RMS_{CMV} to also include current harmonic content offers an approach to enhanced performance.

In this context, an improved cost function is proposed, which balances CMV suppression with harmonic quality of the output current. Since minimizing THD_I implicitly enhances voltage waveform quality as well, the proposed cost function is defined as:

$$CF = \lambda \cdot RMS_{CMV} + \gamma \cdot THD_I \tag{4.28}$$

where λ and γ are weighting coefficients that determine the relative importance of each term. In this study, both coefficients have been set to unity, ensuring equal consideration of CMV and current distortion. The cost function has been minimized offline using MATLAB's *fmincon* solver, as outlined in the previous paragraphs, for both the PPM and PS-PWM techniques. This process yielded a set of $3R$ optimized pulse displacements for PPM and three optimal carrier phase shifts for PS-PWM, determined to be 0°, 192°, and 168°. These optimized parameters have been implemented experimentally, with the corresponding CMV and phase-A current waveforms for $m = 0.9$ shown in Figs. 4.23a-4.23b. The results clearly demonstrate that the PPM technique achieves a superior balance between CMV mitigation and current waveform quality. Specifically, THD_I is reduced from 30.7% to 25%, representing an 18% improvement over PS-PWM. In parallel, the output current ripple is also reduced, decreasing from 11.5 A to 11.2 A (a 2.6% improvement) highlighting the improved performance of PPM in preserving current quality. As expected, a minor compromise in CMV performance is observed relative to the

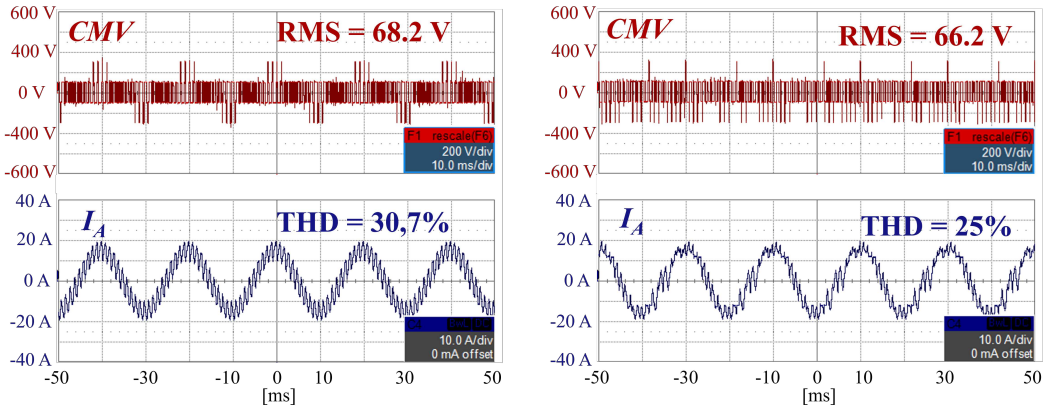


Figure 4.23: Experimental results illustrating CMV and I_A under two modulation strategies: (a) PS-PWM and (b) PPM, after simultaneous harmonic optimization for both quantities, for $m = 0.9$.

previous scenario where only RMS_{CMV} was minimized. For PS-PWM, RMS_{CMV} increases slightly from 68.1 V to 68.2 V, while for PPM it increases from 65.8 V to 66.2 V. Despite this slight degradation, the optimized PPM continues to outperform PS-PWM, confirming its effectiveness in multi-objective scenarios. This advantage stems from the greater degrees of freedom available in PPM, which allow for more flexible and targeted optimization in response to specific performance requirements. Finally, it is worth noting that all THD_I calculations were limited to the 60th harmonic. Higher-order harmonics were found to contribute negligibly to the distortion metrics, validating the sufficiency of this truncation and ensuring computational efficiency without sacrificing accuracy.

c. Impact of CMV generated by PS-PWM and PPM techniques on leakage current

As discussed at the beginning of this chapter, the presence of high CMV is a well-recognized source of accelerated aging in critical electrical and electronic systems, particularly electric drives and PV installations. The rapid transitions in CMV ($\mathrm{d}v/\mathrm{d}t$) induce corresponding high-frequency components in the resulting leakage

currents ($\mathrm{d}i/\mathrm{d}t$), which in turn lead to harmful effects such as bearing degradation in electric motors and reduced longevity of PV panels. In electric drives, steep CMV transitions contribute to increased shaft currents that exacerbate bearing wear. Similarly, in PV systems, elevated CMV slew rates are responsible for significant leakage currents through parasitic capacitance, ultimately compromising the long-term reliability of the installation [79].

Among the various strategies proposed for CMV mitigation, PS-PWM and PPM have demonstrated the most promising results. However, a key distinction emerges in their respective CMV characteristics: while PS-PWM produces CMV waveforms within the range $[-V_{DC}/2, V_{DC}/2]$, PPM confines the CMV within a narrower band, typically $[-V_{DC}/6, V_{DC}/6]$, except for infrequent excursions. This reduction in amplitude range leads to a correspondingly lower $\mathrm{d}v/\mathrm{d}t$, thereby mitigating the generation of leakage currents. By contrast, the broader voltage swing inherent to PS-PWM results in higher CMV derivatives, increasing the risk of component stress and failure. Consequently, PPM offers a structurally superior approach to CMV suppression.

To quantitatively evaluate the leakage current mitigation capabilities of PPM in comparison to PS-PWM, dedicated simulations have been carried out in MATLAB. Two representative case studies were considered: one for electric drive systems and another for PV systems. Each study employed a suitable parasitic equivalent circuit model to replicate the primary leakage paths. In the first case, the parasitic model adopted from Fig. 9 in [79] has been implemented to represent the leakage mechanisms in an inverter-fed motor drive. Both modulation techniques have been tested under identical operating conditions, with a modulation index of $m = 0.9$, and the system parameters have been set according to the referenced study. The CMV waveforms generated by PS-PWM and PPM (both optimized for RMS_{CMV}) have been applied as input stimuli. The simulation results, shown in Figs. 4.24a-4.24b, reveal that the use of PPM leads to a measurable reduction in RMS leakage

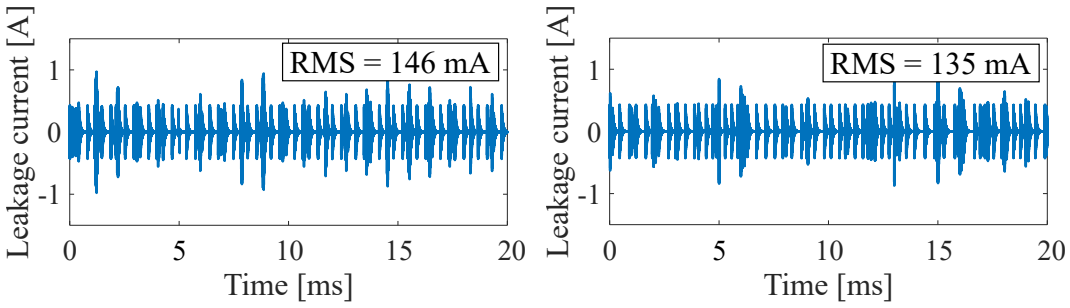


Figure 4.24: Resulting leakage current from the simulation circuit in [79] applying (a) PS-PWM and (b) PPM.

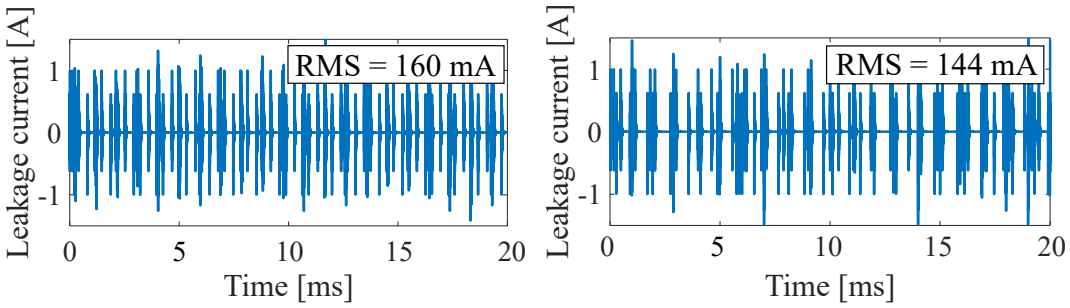


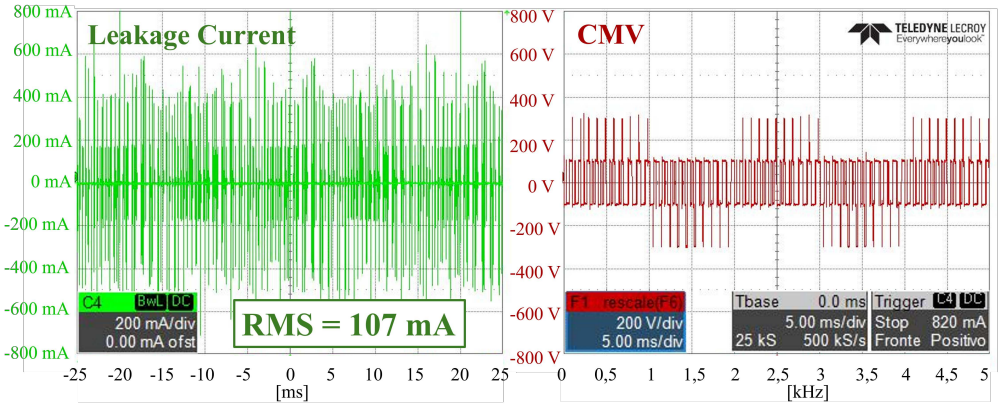
Figure 4.25: Resulting leakage current from the simulation circuit in [80] applying (a) PS-PWM and (b) PPM.

current, from $146\,\mathrm{mA}$ for PS-PWM to $135\,\mathrm{mA}$ for PPM, corresponding to a 7.5% improvement. A similar analysis has been conducted for a PV system using the parasitic model proposed in [80], which captures the common-mode behavior of a PV inverter. Again, simulative results depicted in Figs. 4.25a-4.25b, show that the RMS leakage current is significantly lower with PPM, decreasing from $160\,\mathrm{mA}$ (PS-PWM) to $144\,\mathrm{mA}$, representing a 10% reduction. These outcomes confirm the effectiveness of PPM in both motor and PV applications.

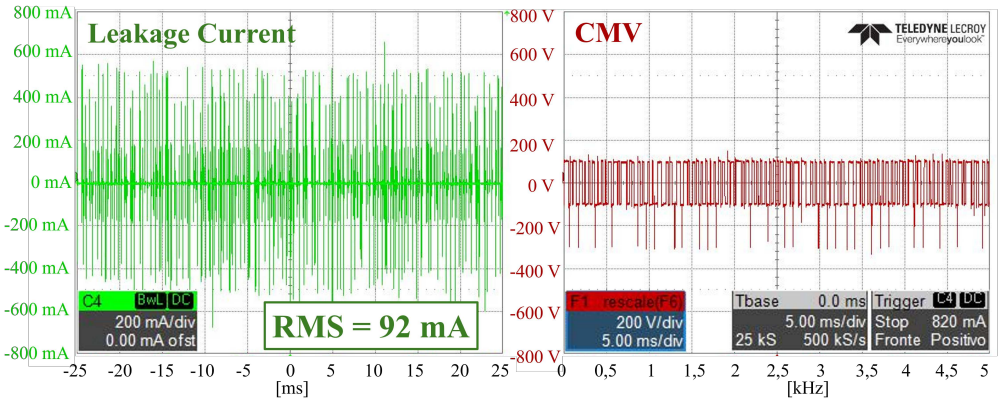
To further substantiate the simulation findings, an experimental validation has been performed. The setup consisted of a $15\,\mathrm{nF}$ capacitor placed between the load star point and the midpoint of the DC-link to emulate the capacitive leakage path. The current flowing through this capacitor serves as a proxy for the leakage current. The experimentally measured waveforms, along with their corresponding

CMV profiles, are presented in Fig. 4.26 for both PS-PWM and PPM (Figs. 4.26a and 4.26b, respectively). Consistent with the simulation results, PPM achieved a lower RMS leakage current of $92\,\mathrm{mA}$ compared to $107\,\mathrm{mA}$ for PS-PWM, equating to a 14% reduction.

In summary, the proposed PPM technique not only achieves superior CMV limitation by reducing its amplitude and rate of change, but also effectively mitigates the associated leakage currents in practical applications. This dual benefit translates into tangible improvements in system reliability, longevity of motor bearings and PV modules, and overall electromagnetic compatibility. These results affirm the suitability of PPM as a robust solution for enhancing the durability and performance



(a)



(b)

Figure 4.26: Experimental evaluation of leakage current and common-mode voltage for the PS-PWM (a) and PPM (b) techniques.

of modern power electronic systems.

4.4.4 Efficiency and reliability analysis

After comprehensively validating the superior capability of the PPM strategy in mitigating CMV and, consequently, in reducing leakage currents, it becomes essential to evaluate its performance in terms of loss minimization, an aspect that directly affects the thermal behavior of power devices. To address this, further experimental measurements have been carried out, comparing the PPM approach with the previously discussed CMV-reduction techniques, as illustrated in Fig. 4.27. The figure reports both conduction and switching losses, normalized in per unit (p.u.) with reference to 80% of the converter's rated power, which corresponds to its nominal operating point.

A thorough analysis reveals that the PPM technique delivers outstanding results, achieving switching losses as low as 2.13×10^{-4} p.u. and conduction losses of 3.4×10^{-3} p.u., the lowest among all the evaluated strategies. This high-efficiency behavior translates into a 1.4% reduction in total power losses compared to AZSPWM, which stands out as the most competitive alternative in the benchmark. Consequently, PPM ensures the highest overall efficiency among the investigated methods. This outcome is of particular significance, as the reduction in power losses directly implies a decrease in heat dissipation. Under equivalent thermal management conditions, this leads to a lower temperature rise in the semiconductor devices, thereby enhancing their longevity and contributing to the extended operational lifespan of the power converter [81].

Further reliability assessment has been performed by analyzing the lifetime expectancy of the DC-link capacitor, through the computation of the DC current ripple associated with each modulation technique. As summarized in Table 4.4, the PPM strategy yields a ripple current of only 2.53 A, marking a 2% decrease compared to

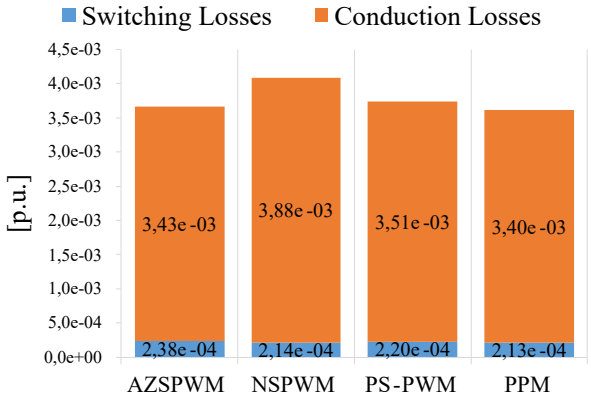


Figure 4.27: Switching and conduction losses measured in per unit with respect to 80% of the rated power for all CMV reduction techniques under comparison.

the closely performing PS-PWM technique. This reduction is particularly relevant, as the lifespan of electrolytic capacitors is highly dependent on their operating temperature [82]. Lower ripple currents lead to reduced internal heat generation and, consequently, diminished thermal stress, thereby extending component life.

In summary, beyond its remarkable efficiency, the PPM strategy emerges as a superior choice for enhancing the overall reliability of the converter. By alleviating the thermal and electrical stress imposed on passive components such as the DC-link capacitor, PPM contributes to the development of more robust and durable power electronic systems.

4.5 Key outcomes

The main achievements and insights of the proposed innovative PPM technique are summarized as follows, covering both the fundamental advancements in control signal synthesis and the superior performance demonstrated in the CMV reduction strategy:

- Independent pulse position optimization: the method allows for the individual optimization of each pulse position within a control period, offering a high degree of flexibility and enabling precise control in waveform synthesis.

- Improved harmonic performance: the proposed method enables a significant reduction of harmonic distortion, achieving results that are comparable to those obtained through advanced strategies such as SHE/SHM.

- Fast dynamic response: experimental validation demonstrates that the technique exhibits a dynamic behavior similar to that of conventional PWM, ensuring excellent responsiveness during transient operating conditions.

- Synergistic integration of PWM and SHE/SHM advantages: by effectively merging the benefits of PWM (in terms of dynamic response) and SHE/SHM (in terms of harmonic optimization), the proposed approach constitutes a significant advancement over traditional techniques.

- Potential to overcome intrinsic limitations of existing methods: the results suggest that this technique may pave the way for future developments capable of overcoming the constraints typically associated with both PWM and SHE/SHM, thereby representing a promising direction for high-performance power converter control.

- Three-phase inverter CMV mitigation: When optimizing solely the RMS_{CMV}, the PPM technique achieves a 3.4% RMS reduction compared to PS-PWM, confirming its enhanced capability in suppressing common-mode disturbances.

- Combined CMV and current quality optimization: When both RMS_{CMV} and THD_I are simultaneously minimized, PPM outperforms PS-PWM with a 3% lower RMS_{CMV} and an 18.5% reduction in THD_I, indicating superior current waveform quality.

- Leakage current reduction: The implementation of PPM results in a 14% decrease in leakage current RMS value relative to PS-PWM, demonstrating improved PV and motor drives safety.

- Efficiency and loss reduction: PPM ensures the highest efficiency among all tested strategies, mainly due to its ability to reduce overall converter losses by 1.4% compared to AZSPWM, the best-performing alternative in terms of energy efficiency. The reduction in losses achieved through PPM leads to lower heat generation, minimizing the temperature rise of power devices and thereby extending their operational lifetime under the same thermal management conditions.

- Enhanced DC-link capacitor reliability: The PPM approach reduces the DC-link current ripple to 2.53 A, representing a 2% decrease compared to PS-PWM. This reduction lowers thermal stress on the capacitor, contributing to a longer component lifespan and improved system reliability.

- Suitability for motor drive systems: In electric drives, where high CMV can lead to increased losses, vibrations, and thermal loading, the application of PPM contributes to enhanced system efficiency, reduced mechanical stress, and improved motor durability.

- Benefits in photovoltaic applications: In PV systems, CMV-induced leakage currents can cause corrosion of metallic structures and long-term degradation of modules. The adoption of the PPM technique mitigates these effects, improving the overall robustness and reliability of the installation.

In conclusion, the PPM strategy has proven to be a versatile and effective solution that, thanks to its ability to offer flexible waveform optimization and a high dynamic response with improved harmonic performance, enhances the overall converter efficiency. Concurrently, its specific application to three-phase inverter CMV reduction significantly contributes to minimizing thermal and electrical stress on components and increasing long-term reliability in both motor drive and photovoltaic systems. The main results and insights obtained from the analysis of the

Table 4.4: Results Comparison

Modulation Strategy	RMS_{CMV} **[V]**	ΔV **[V]**	**Losses [p.u.]**	**DC-Link Ripple [A]**
AZSPWM	110.0	400	3.66e-3	2.73
NSPWM	106.2	400	4.09e-3	2.68
PS-PWM	68.1	400	3.73e-3	2.58
PPM	65.8	200	3.61e-3	2.53

PPM-based CMV reduction strategy are summarized in Table 4.4, evidencing its superiority in terms of electrical performance, efficiency, and practical applicability.

Chapter 5

Pulse Position Modulation for Harmonic Distortion Reduction in Cascaded H-Bridge Converters with Cell Imbalance

In the previous chapter, the innovative PPM technique has been introduced and validated on simpler converter topologies, in order to illustrate its operating principles and assess its benefits. Since the main focus of this PhD thesis is the analysis and control of multilevel power converters, this chapter extends the application of the PPM strategy to the CHB converter. Particular attention is devoted to evaluating the performance of the proposed modulation under conditions of cell-level modulation index imbalance (such as those arising in photovoltaic, battery-based or other heterogeneous sources) where each submodule operates with a different index. In these scenarios, the PPM strategy is assessed for its ability to preserve a high-quality harmonic profile of both output voltage and current, thereby ensuring superior power quality despite non-uniform operating conditions.

5.1 Overview of existing methods for mitigating cell imbalance in CHB converters

As deeply analyzed in the previous chapters, cascaded multilevel converters represent a mature and widely adopted technology for medium-voltage motor drives and the grid integration of medium- to high-power systems, including distributed energy resources. Among these, the CHB topology stands out for its versatility and scalability. This modular structure, illustrated in the lower part of Fig. 5.1, offers notable advantages in terms of fault tolerance and ease of maintenance. Furthermore, the number of cells can be adapted to the required voltage level, making the topology highly flexible and suitable for a wide range of applications [83].

As already stated, in CHB converters, the PS-PWM strategy is frequently employed to enhance both waveform quality and power distribution across the cells

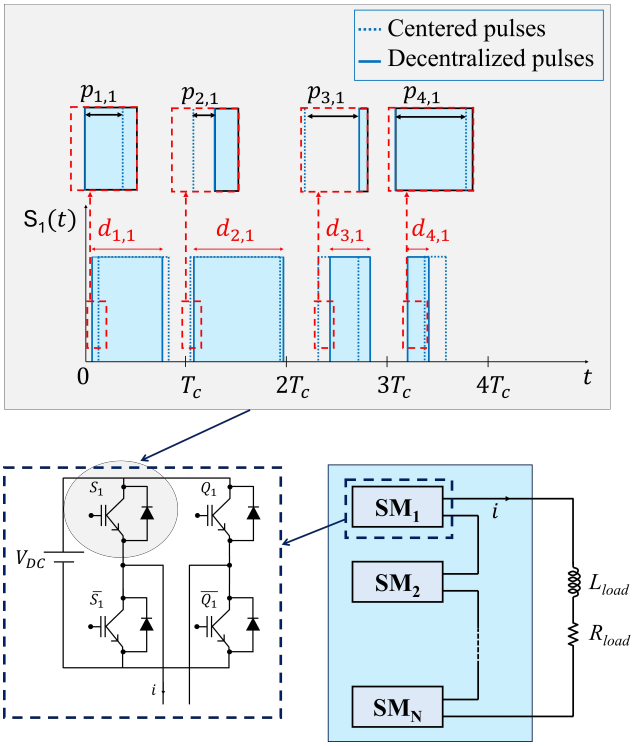


Figure 5.1: Schematic representation of a single phase Cascaded H-Bridge inverter topology modulated through the proposed PPM technique.

[84, 85]. This approach involves driving each H-bridge module using standard unipolar PWM, where triangular carrier signals of identical frequency are applied. To enable PS-PWM, these carriers are phase-shifted relative to one another, with the shift increasing progressively along the series-connected cells ($\phi_x = (x - 1)\pi/N$, where x represents the cell number and N is the number of cells per phase). This phase displacement causes the output voltage of the converter to exhibit a remarkable harmonic cancellation and a significantly higher equivalent switching frequency, improving the spectral content of the waveform by shifting dominant harmonics to higher frequencies [86, 87]. This behavior is illustrated in Fig.5.2, which shows the output waveform of a three-cell CHB converter along with its harmonic spectrum (in blue - balanced case), operating at a switching frequency of $f_c = 1\,\text{kHz}$. As expected, the first significant harmonic group appears at $2N f_c$, i.e., at $6\,\text{kHz}$. In addition, a key advantage of this modulation technique is its inherent ability to balance power among cells, which reduces thermal stress across devices and enhances reliability.

However, the CHB converter may occasionally operate under unbalanced conditions, where the reference voltages of the individual cells differ due to various underlying causes. One common scenario arises in CHB configurations where each cell is interfaced with PV arrays [88–90]. In such cases, the power processed by each cell can vary as a result of the Maximum Power Point Tracking (MPPT) algorithm, which independently adjusts the operating point of each PV array to maximize energy extraction from solar irradiation. Another potential source of imbalance occurs when the input power sources are batteries, which may have different states of charge. This disparity can lead to non-uniform power distribution across the cells, further contributing to voltage unbalance [91, 92].

However, when the CHB converter operates under unbalanced conditions, the benefits associated with PS-PWM are significantly compromised. This phenomenon is illustrated by the red waveform and its corresponding frequency spectrum in

Fig. 5.2. It is evident that low-order harmonic groups emerge under such conditions, which are typically suppressed during balanced operation. The presence of these harmonics leads to a degradation in the quality of both the output voltage and the resulting current, thereby negatively impacting the overall performance of the converter. To address this issue, the literature has investigated both closed-loop control schemes and open-loop modulation strategies. In particular, the works in [93–95] tackle the unbalancing problem by implementing model predictive control approaches within a closed-loop framework. Similarly, in [96] a closed-loop harmonic suppression strategy for CHB converters is proposed, which adaptively adjusts the carrier displacement angles in the *dq* frame to minimize the harmonic content under unbalanced operating conditions. Conversely, several contributions have focused exclusively on optimized modulation techniques for mitigating unbalanced conditions. For example, [97] introduces a selective harmonic elimination approach that compensates for unbalanced operation in CHB converters while suppressing third-order harmonics. Among open-loop strategies, the most widely adopted approach for addressing unbalancing issues relies on modifying the phase-shift angles of the carriers to suppress undesired low-frequency harmonics. In particular, [98] proposes a phasor-diagram-based method to compute optimal phase-shift angles in CHB converters with unbalanced DC voltages, thereby reducing double switching-frequency harmonics without requiring complex optimization procedures. Similarly, the studies in [70, 99–102] investigate the optimization of the carrier phase-shift angles in CHB converters, aiming to improve the harmonic performance of the output voltage and current. In these works, the phase-shift among the modulation carriers associated with each H-bridge cell is not kept fixed, as in the conventional PS-PWM technique, but is instead treated as an additional degree of freedom. By appropriately adjusting these phase-shift angles, the resulting output waveform can be analytically shaped to suppress or even cancel specific harmonic groups, particularly those around low-order components that most affect the

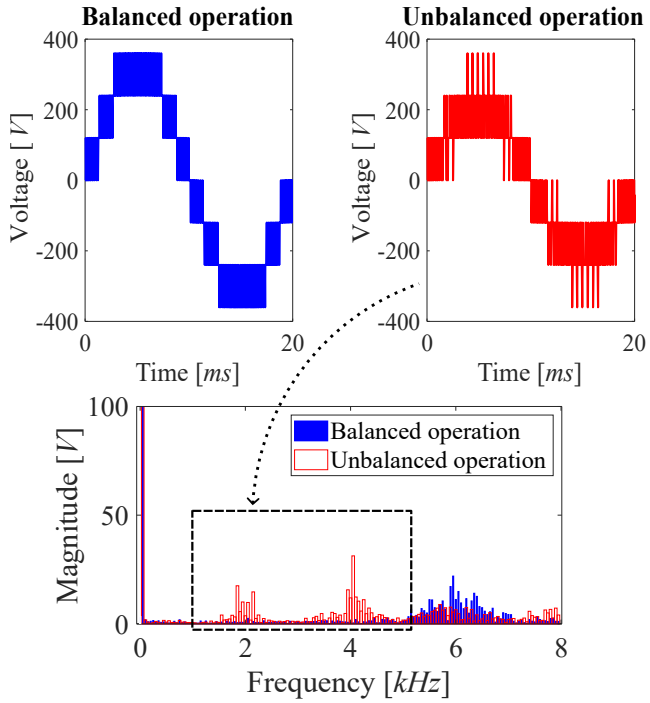


Figure 5.2: Output voltage and harmonic spectrum of the three-cell CHB converter under balanced (blue) and unbalanced (red) conditions.

THD/WTHD. The proposed methods generally rely on an analytical modeling of the converter output voltage, where the harmonic content is expressed as a function of the carrier phase-shift angles and modulation index. Optimization algorithms are then employed to minimize selected harmonic amplitudes or a global cost function related to the THD/WTHD. In some cases, these strategies allow the cancellation of dominant harmonics without modifying the fundamental amplitude, achieving a quasi-sinusoidal waveform while maintaining full utilization of the DC-link voltage. However, all these methods are ultimately based on optimizing the carrier phase-shift, which corresponds to a global adjustment of the control signal and does not explicitly account for the behavior within each individual control period.

In this chapter, a completely new approach to enhance the harmonic quality of CHB output waveforms under unbalanced operating conditions, based on PPM, is presented.

5.2 A PPM-based approach to mitigate cell imbalance in CHB converters

The method proposed in this paper to address the harmonic issues caused by unbalanced operation in CHB builds upon the innovative PPM technique presented in the previous chapter [71, 103]. As deeply analyzed before, unlike conventional PWM strategies, which rely on fixed-position pulses within each sampling period and on the comparison between modulating and carrier signals, PPM directly synthesizes the gate signals of the power converter. This direct synthesis eliminates the need for carrier-modulator comparison and, by optimally positioning gate pulses of appropriate width within each control interval T_c, significantly improves harmonic quality while achieving fast dynamic performance. Fig. 5.1 illustrates the fundamental concept underlying the PPM strategy. The control signal of a single switch is shown at the top of the figure, emphasizing that its individual pulses are no longer fixed within the control period but can be shifted to different positions, thereby increasing the number of degrees of freedom.

In this work, the enhanced degrees of freedom offered by the PPM strategy, are exploited to mitigate undesired harmonics in CHB output waveforms under unbalanced operating conditions. The PPM strategy allows direct control of the harmonic spectrum by generating individual pulses with specified durations and precisely assigning their positions within each control interval T_c. This ensures both the correct average output voltage and a targeted harmonic profile. Unlike traditional PWM approaches, this method does not rely on comparing carrier and modulating signals, yet it maintains fixed-frequency operation, allowing consistent control actions at every T_c. The pulse duration, determined by the desired value of the fundamental voltage component, is computed by the controller at each control step. As illustrated in Fig. 5.1, this value defines the duty cycle, while the pulse position is treated as

an additional degree of freedom. This decentralized pulse placement makes it possible to individually shift each pulse within its sampling period to actively influence the spectral characteristics of the CHB output voltage. A comprehensive analytical treatment of individual pulse behavior is presented in Chapter 4 [71], where a mathematical framework is developed to enable the direct synthesis of gate signals as pulse trains with adjustable positions. According to this formulation, the generic gate signal $x(t)$ is given by (4.16). In this chapter, that mathematical analysis is applied to optimize the harmonic content of the CHB converter output voltage, and consequently its current, under unbalanced cell operation. The objective is to minimize the required output filter size by acting solely on the modulation strategy, without modifying the hardware structure.

5.2.1 PPM-based CHB output voltage expression derivation

The study focuses on a single phase CHB converter composed of three cells. As a result, a total of 6 gate signals are needed to control the converter and generate the desired waveforms (two switching signals per cell). The application of the PPM method requires, as a preliminary step, the computation of the duty-cycle values for each control interval T_c, as determined by the controller. Subsequently, the analytical expression for the CHB converter voltage can be derived. Since the CHB converter consists of a series connection of full-bridge cells, the analysis begins with

the generic expression of the output voltage of the x-th cell, as given in (5.1) [71].

$$\begin{aligned} v_x(t) = {} & m_x \frac{V_{DC}}{2} \sum_{n=1}^{R} (d_{n,x} - d_{180,n,x}) f_0 \\ & + m_x V_{DC} \sum_{n=1}^{R} \sum_{k=1}^{\infty} \frac{i}{2\pi k} e^{-i2\pi k f_0 (n-1) T_c} \\ & \times \left[e^{-i2\pi k f_0 \left(\frac{T_c - d_{n,x}}{2} + p_{n,x} \right)} \left(e^{-i2\pi k f_0 d_{n,x}} - 1 \right) \right. \\ & \left. - e^{-i2\pi k f_0 \left(\frac{T_c - d_{180,n,x}}{2} + p_{180,n,x} \right)} \left(e^{-i2\pi k f_0 d_{180,n,x}} - 1 \right) \right] \\ & \times \cos(2\pi k f_0 t) \end{aligned} \tag{5.1}$$

Here, V_{DC} denotes the DC voltage applied to each cell, assumed to be identical across all cells and phases. The variables $d_{n,x}$ and $d_{180,n,x}$ are arrays containing the duty-cycle values, calculated for each control interval, associated with the two legs of a generic cell. The modulation index m_x characterizes the x-th cell and is defined as the per-unit value of the fundamental component of the output phase voltage waveform with respect to V_{DC} [18]. It is important to note that m_x may vary among cells in scenarios involving unbalanced operation, which is the central focus of this study. Lastly, $p_{n,x}$ and $p_{180,n,x}$ are arrays representing the unknown pulse displacement values, relative to their respective centered positions, for the two legs of the x-th cell. These displacement values are the parameters to be identified. These parameters are clearly illustrated in the upper part of Fig. 5.1, which shows the PPM signal associated with switch S_1. For clarity, only the first four pulses are depicted.

Since the output voltage of a CHB converter is the sum of the voltages generated by its individual cells, the overall phase voltage can be expressed as in (5.2), where N is the number of cells per phase. It is evident that the harmonic content of the CHB output voltage explicitly depends on the pulse displacements of each gate signal, denoted as $p_{n,x}$. Specifically, the unknown parameters are the p_n arrays,

each consisting of R elements corresponding to the positions of the pulses within a fundamental period T_o. For each leg of the three cells, one such array is defined. As a result, a total of 6 p_n arrays must be identified to properly shape the harmonic profile of the CHB output voltage under unbalanced operating conditions, if the considered CHB is made by three cells. Further details on the identification of these parameters for harmonic improvement are provided in the next paragraph.

$$
\begin{aligned}
v_{CHB}(t) = & \sum_{x=1}^{N} m_x \frac{V_{DC}}{2} \sum_{n=1}^{R} (d_{n,x} - d_{180,n,x}) f_0 \\
& + \sum_{x=1}^{N} m_x V_{DC} \sum_{n=1}^{R} \sum_{k=1}^{\infty} \frac{i}{2\pi k} e^{-i2\pi k f_0 (n-1) T_c} \\
& \times \left[e^{-i2\pi k f_0 \left(\frac{T_c - d_{n,x}}{2} + p_{n,x} \right)} \left(e^{-i2\pi k f_0 d_{n,x}} - 1 \right) \right. \\
& \left. - e^{-i2\pi k f_0 \left(\frac{T_c - d_{180,n,x}}{2} + p_{180,n,x} \right)} \left(e^{-i2\pi k f_0 d_{180,n,x}} - 1 \right) \right] \\
& \times \cos(2\pi k f_0 t)
\end{aligned}
\tag{5.2}
$$

5.2.2 Pulse displacements identification procedure in unbalanced CHB

Based on the harmonic expression of the CHB output voltage derived in (5.2), it is crucial to establish a specific optimization target in order to accurately determine the appropriate pulse displacements. As previously introduced, unbalanced operation in CHB inverters results in the appearance of low-order harmonic groups in the output voltage spectrum. This degradation negatively affects the harmonic quality of the current waveform, requiring the use of larger and more complex output filters. To enhance the harmonic performance of the current, it becomes necessary to minimize the voltage WTHD of the CHB output voltage, which leads to the definition of the

following cost function:

$$WTHD = \frac{1}{V_{CHB_1}} \sqrt{\sum_{k=2}^{\infty} \left(\frac{V_{CHB_k}}{k} \right)^2} \tag{5.3}$$

where V_{CHB_k} denotes the k-th harmonic component of the CHB output voltage defined in (5.2), and V_{CHB_1} is the amplitude of the fundamental component. The analysis is limited to harmonics up to the third group in order to enable a proper evaluation. Compared to the classical THD, the WTHD assigns greater weight to low-order harmonics, that most significantly affect current distortion and filter sizing, making it more suitable for evaluating harmonic performance in unbalanced CHB conditions.

An offline optimization process has been carried out using MATLAB's *fmincon* nonlinear programming solver. It is worth noting that any suitable optimization technique could be employed to minimize the WTHD of the voltage waveform; however, the selection or comparison of optimization methods falls outside the scope of this work. As thoroughly explained in Chapter 4, specific constraints are imposed on each displacement value to ensure that every pulse forming the gate signal remains entirely within its respective control interval T_c, preventing any overlap into adjacent intervals. The WTHD is directly influenced by the pulse displacement values, which represent the only unknowns to be determined in order to meet specific harmonic requirements under unbalanced modulation index conditions (m_x). These displacement values are the outputs of the optimization process. As a result, a set of six LUTs has been generated, each containing the corresponding optimal pulse displacements.

5.3 Numerical validation

To assess the effectiveness of the proposed PPM strategy in mitigating harmonic distortion under unbalanced operating conditions in CHB inverters, time-domain simulations have been performed on the single phase configuration depicted in Fig. 5.1. For benchmarking purposes, the results are compared against those obtained using the well-established VPS-PWM technique, demonstrating the superior harmonic performance of PPM in scenarios involving cell imbalance.

In the present analysis, it is postulated that the three submodules constituting the CHB inverter operate under conditions of unequal power sharing. Despite this non-uniform distribution of power among the submodules, the total power transferred by the converter to the load is assumed to remain constant across all operating scenarios. More precisely, the output voltage of the converter is defined as $m_{\text{tot}}\, V_{\text{DC,tot}}$, where m_{tot} denotes the overall modulation index, computed by the control system to ensure that the desired output power is delivered. The term $V_{\text{DC,tot}}$ represents the cumulative DC-link voltage, obtained as the sum of the individual DC voltages of the three submodules. Specifically, in this analysis it is assumed that the required modulation index to be processed is fixed at $m_{\text{tot}} = 0.5$. However, one or more of the three submodules may become compromised due to various operational factors, such as those discussed in the introduction of this chapter. As a consequence, the power processed by each submodule is no longer uniformly distributed. In such cases, the non-compromised submodules must compensate for the degraded ones (for instance, through an active thermal control strategy) in order to ensure that the converter continues to generate the required output voltage, namely $0.5\, V_{\text{DC,tot}}$. Accordingly, four different operating scenarios have been considered, each characterized by a distinct distribution of power among the submodules, while maintaining the total modulation index constant at $m_{\text{tot}} = 0.5$. These scenarios, reported in Table 5.1, have been first investigated numerically and subsequently validated through

experimental testing. The optimization algorithm previously described has been applied to the PPM strategy, yielding a set of 6 optimal displacement arrays. Similarly, VPS-PWM has been implemented by applying the same optimization procedure to determine the phase-shift angles that minimize the same cost function. The resulting values are also listed in Table 5.1.

Table 5.1: Simulation Parameters for the Validation of PPM Performance on Unbalanced CHB

Parameter	**Symbol**	**Value**	**Unit**
Cell voltage	V_{DC}	120	V
Fundamental frequency	f_o	50	Hz
Switching frequency	f_c	1	kHz
Number of cells	N	3	–
Load inductance	L_{load}	6.8	mH
Load resistance	R_{load}	30	Ω
Modulation indices	$[m_1, m_2, m_3]$	Scenario 1: [0.8, 0.5, 0.2]	–
		Scenario 2: [0.4, 0.2, 0.9]	
		Scenario 3: [0.5, 0.3, 0.7]	
		Scenario 4: [0.2, 0.6, 0.7]	
VPS-PWM angles	$[\phi_1, \phi_2, \phi_3]$	Scenario 1: [0, 106.3, 52.6]	°
		Scenario 2: [0, 54.5, 106.1]	
		Scenario 3: [0, 126.8, 68.2]	
		Scenario 4: [0, 126.7, 53.3]	

Based on the simulation parameters summarized in Table 5.1, the output voltage spectra of the CHB inverter are computed and illustrated in Fig. 5.3. Four unbalanced operating scenarios, as defined in Table 5.1, are considered. The corresponding results obtained using VPS-PWM (top) and PPM (bottom) are reported, with both sets of spectra compared against those produced by the conventional PS-PWM method, shown in red.

It is readily observed that, across all four scenarios, the application of the proposed PPM technique results in the complete suppression of the first harmonic

group, which is particularly challenging to filter due to its low-frequency content. In contrast, when VPS-PWM is applied, only a limited number of sideband components within this harmonic group are suppressed, while others remain, preventing full cancellation. This leads to superior harmonic mitigation performance with PPM. In particular, across the four scenarios, the proposed PPM technique achieves voltage WTHD reductions respectively of 67%, 60%, 72%, and 37% with respect to the conventional PS-PWM method. By contrast, the VPS-PWM strategy provides significantly lower improvements, with reductions of only 41.3%, 26.7%, 38%, and 10.5%, respectively.

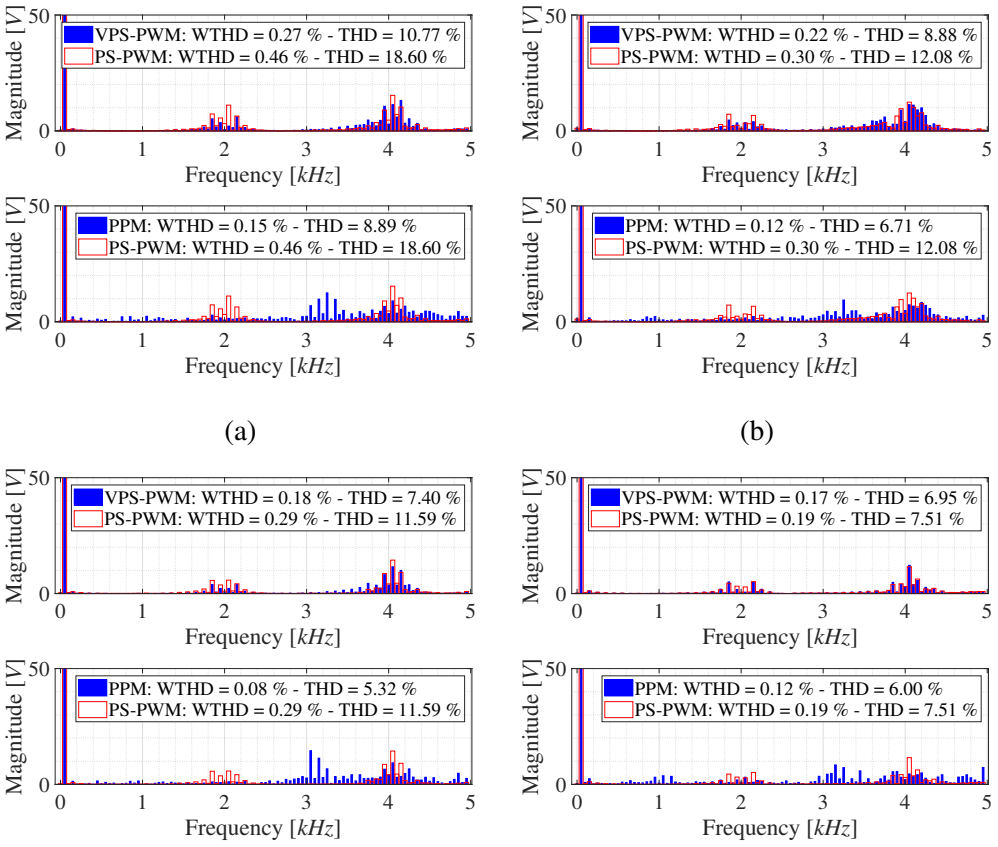


Figure 5.3: Spectra of the CHB inverter output voltage obtained with VPS-PWM (top) and PPM (bottom), in comparison with conventional PS-PWM, for scenarios 1 (a), 2 (b), 3 (c), and 4 (d).

The superior performance of the PPM technique is attributed to its greater num-

ber of degrees of freedom compared to VPS-PWM. In PPM, each switching pulse can be individually repositioned within its corresponding control period T_c to shape the harmonic spectrum as desired. In contrast, VPS-PWM applies a uniform phase shift to all pulses within a cell, determined by a fixed carrier displacement angle, thereby lacking the flexibility to control each pulse independently.

5.4 Experimental validation

The effectiveness of the proposed PPM strategy in mitigating the harmonic issues arising when the CHB operates under unbalanced conditions has been experimentally validated using the setup available at the Power Electronics Laboratory of the Polytechnic University of Bari. Specifically, a single-phase three-cells configuration connected to an R–L load has been tested, operating at a switching frequency of $1kHz$. A control board based on a Xilinx Zynq system-on-chip (SoC) has been employed to manage the converter operation. The parameters used in the experimental tests are the same used for the simulation, listed in Table 5.1, while the experimental setup is depicted in Fig. 5.4.

To demonstrate the effectiveness of the proposed PPM technique in improving the harmonic quality of CHB waveforms, the same comparison presented in the previous section for the simulation results has been carried out experimentally. The proposed strategy has been evaluated against the conventional PS-PWM and the optimized VPS-PWM. The same scenarios described in Table 5.1 and previously analyzed through simulations have been experimentally tested. The corresponding results are reported in Figs. 5.5–5.7, where the output voltage and current waveforms, together with their harmonic spectra, are shown under PS-PWM, VPS-PWM, and PPM operation, respectively. Each figure presents the results for the four different scenarios (a–d).

It is clearly observed that the proposed PPM technique demonstrates superior

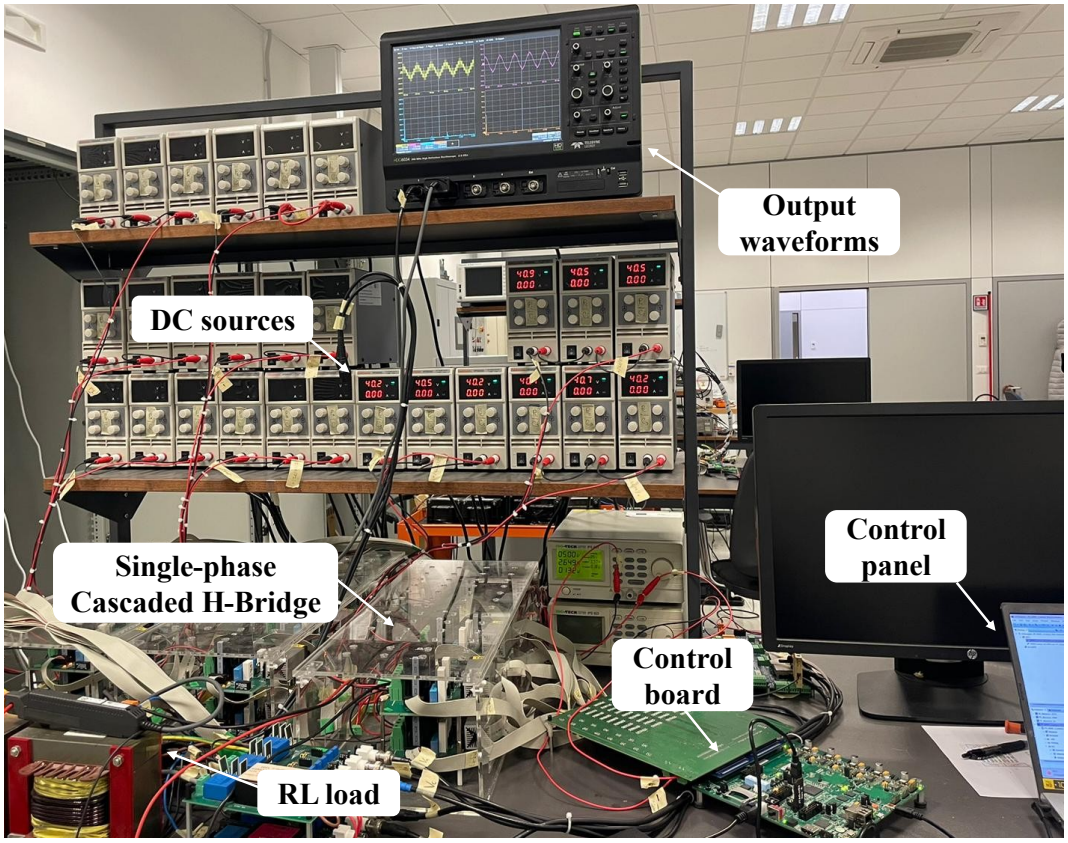


Figure 5.4: Experimental setup of the single-phase 3-cells CHB converter.

performance in mitigating harmonic distortion under unbalanced CHB operating conditions across all investigated scenarios. In particular, the PPM method achieves a complete suppression of the first harmonic group in the low-frequency range, typically the most challenging to filter and, under normal balanced CHB operation, inherently absent. In contrast, the VPS-PWM strategy fails to entirely eliminate this harmonic group, managing instead to attenuate only a limited number of its associated sideband components.

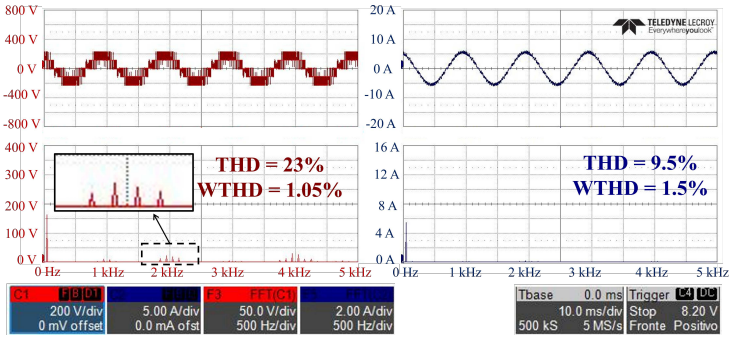
This phenomenon is confirmed by the THD and WTHD values reported in the figures. Among the reference methods, VPS-PWM, identified as the most effective conventional alternative, achieves a voltage WTHD (i.e., the optimized cost function) reduction of 6.7%, 2.3%, 20.8%, and 1.3% for the four scenarios, respectively. In contrast, the proposed PPM technique attains voltage WTHD reductions of 19%, 9.3%, 36%, and 10.5% across the same scenarios, thus significantly outper-

forming VPS-PWM in terms of harmonic improvement. Consequently, the current waveforms also exhibit notable harmonic enhancements, as evidenced by the corresponding THD and WTHD values shown in the figures. These results are in good agreement with the corresponding simulation outcomes discussed in the previous section. Once again, the remarkable advantages of the proposed PPM technique become evident, owing to its increased degrees of freedom and, consequently, its capability to independently position each individual pulse that composes the overall driving signal. These benefits are also clearly observed in multilevel converter topologies such as the CHB.

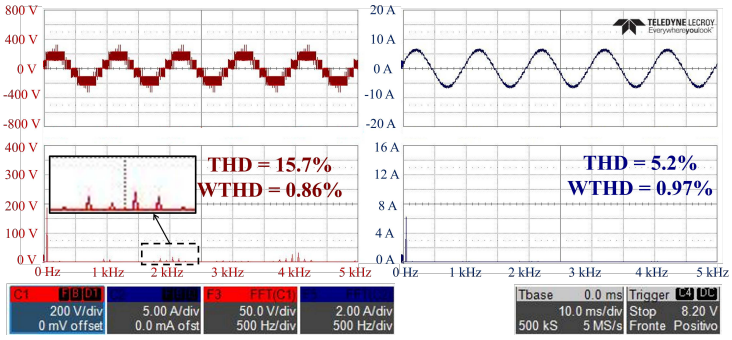
5.5 Key Outcomes

The key findings and contributions discussed throughout this chapter are summarized below, highlighting the effectiveness and validation of the proposed PPM technique through both simulation and experimental analyses:

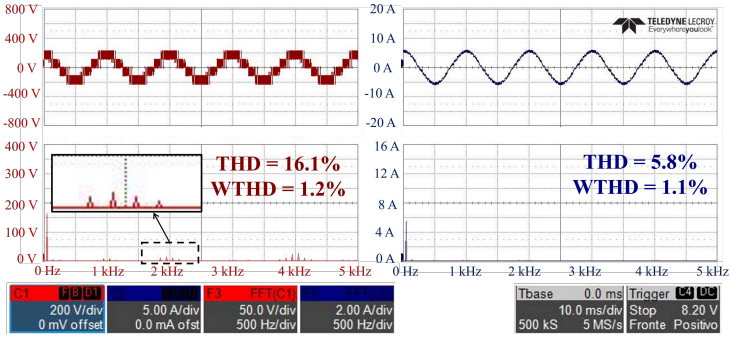
- The proposed PPM technique has been successfully extended and validated on multilevel converter topologies, specifically on the CHB architecture, demonstrating a strong capability to mitigate harmonic distortion under unbalanced operating conditions.
- Both simulation and experimental results confirm that PPM significantly improves the harmonic performance of the CHB output voltage and current compared to conventional PS-PWM and optimized VPS-PWM techniques.
- Overall, the PPM method represents an effective open-loop solution for enhancing harmonic quality in CHB converters, ensuring high power quality even in the presence of unbalanced conditions.



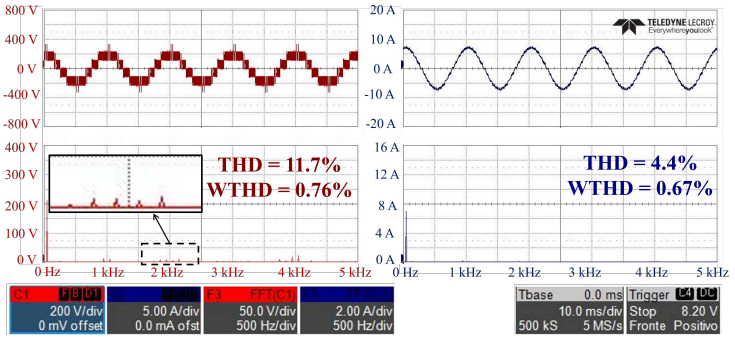
(a)



(b)

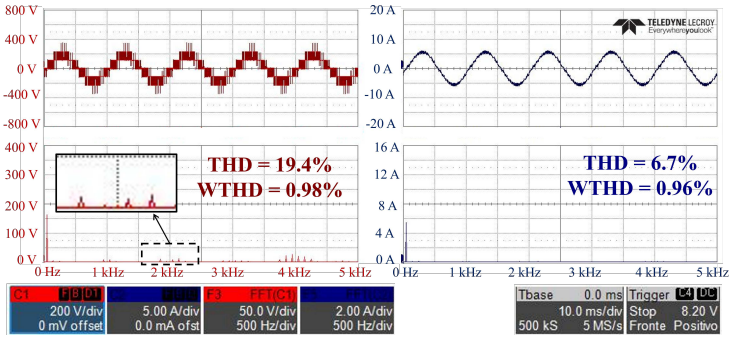


(c)

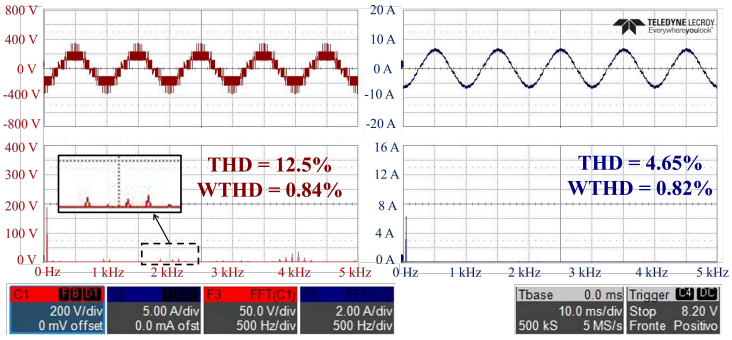


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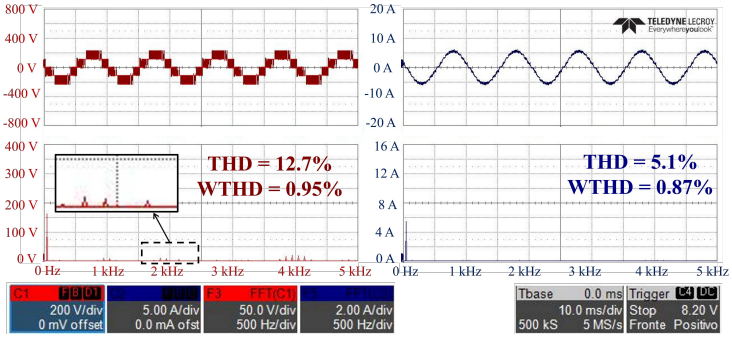
Figure 5.5: Experimental voltage and current waveforms, together with their corresponding harmonic spectra, for Scenarios 1–4 (a–d), respectively, under PS-PWM operation.



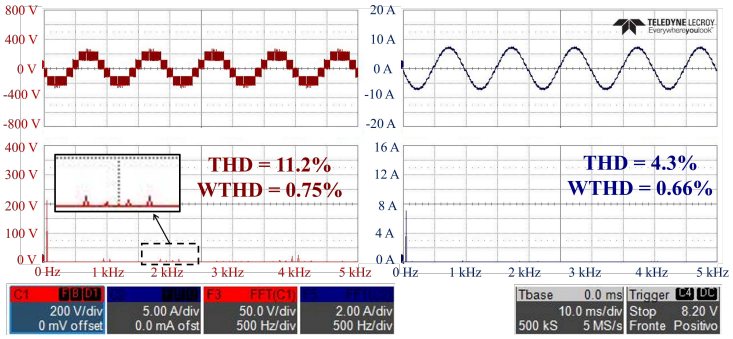
(a)



(b)

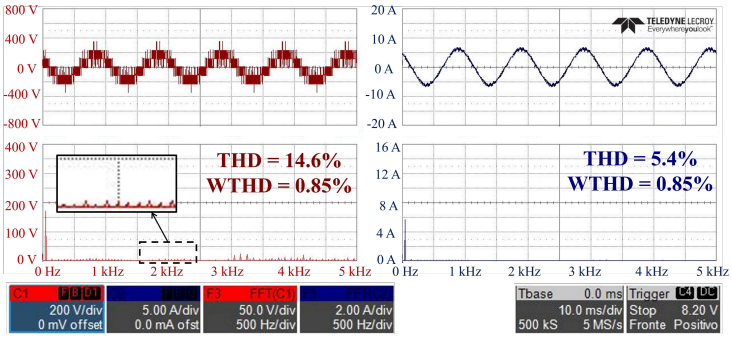


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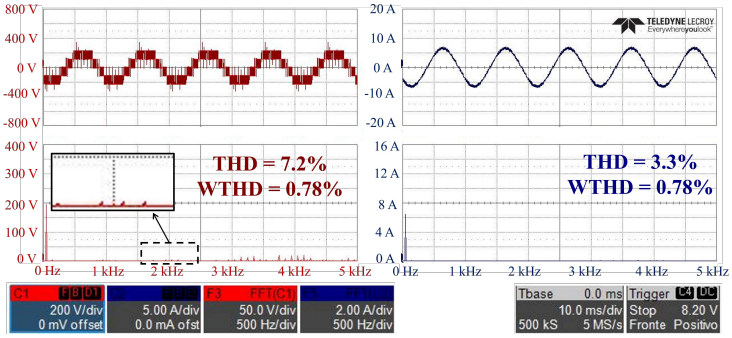


(d)

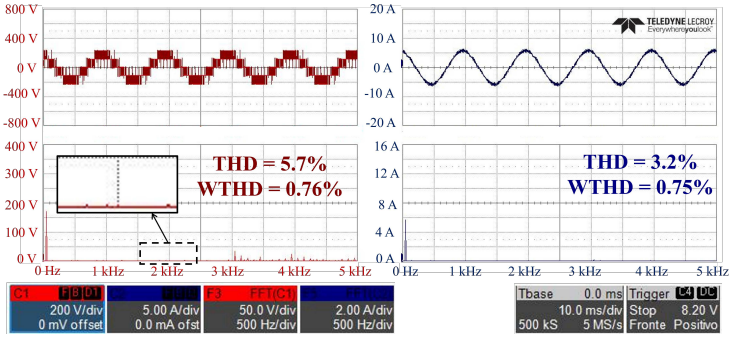
Figure 5.6: Experimental voltage and current waveforms, together with their corresponding harmonic spectra, for Scenarios 1–4 (a–d), respectively, under VPS-PWM operation.



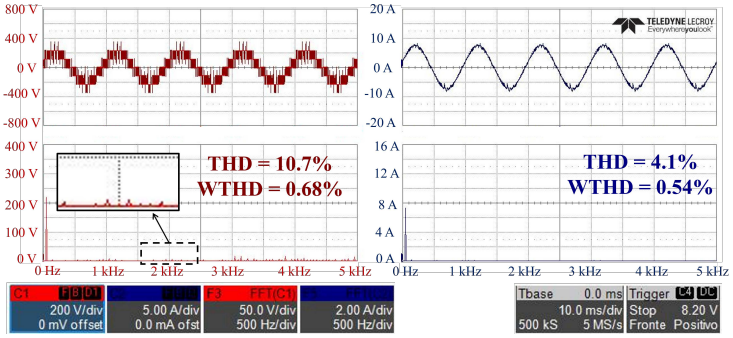
(a)



(b)



(c)



(d)

Figure 5.7: Experimental voltage and current waveforms, together with their corresponding harmonic spectra, for Scenarios 1–4 (a–d), respectively, under PPM operation.

Chapter 6

Cascaded H-Bridge Based on Interleaved Full-Bridge Submodules

In the preceding chapters, this thesis has explored various techniques aimed at the harmonic optimization of waveforms generated by the CHB converter. These strategies have demonstrated the CHB's potential not only as a high-quality waveform generator but also as an active element in improving power quality within electrical systems.

Building upon this foundation, the current chapter introduces and investigates an innovative CHB architecture based on interleaved full-bridge submodules. This configuration offers significantly enhanced current scalability compared to the conventional CHB topology, making it especially suitable for low-voltage, high-power applications. By interleaving multiple submodules, the proposed design can synthetically multiply the number of output voltage levels without increasing the number of hardware units, thereby extending the well-established advantages of the CHB to new application domains.

A dedicated modulation strategy tailored to this interleaved architecture is presented and thoroughly analyzed in terms of its impact on the output waveform's harmonic content and voltage level resolution. A comparative evaluation with the

traditional CHB configuration, under the constraint of a fixed number of submodules, demonstrates the superior harmonic performance of the proposed approach. Experimental validation further confirms the practicality and effectiveness of the interleaved converter and its modulation scheme. Although this study focuses on a single-phase implementation, the proposed methodology can be readily extended to three-phase systems with minimal adjustments.

6.1 Interleaved submodule configurations in CHB converters: literature background

The increasing electrification of key sectors such as renewable energy, electric mobility, and industrial automation has amplified the demand for power converters that combine high efficiency, modularity, and scalability [104]. In this context, multilevel converter technologies have attracted significant interest due to their inherent modular structure, improved waveform quality, and ability to deliver high output power using low-voltage semiconductor devices [2, 105]. Their robustness and fault-tolerance capabilities further contribute to their suitability for demanding applications.

Although the CHB converter has already been introduced in previous chapters for its well-known structural advantages and suitability in grid-connected systems [9, 106, 107], the literature presents a wide variety of derived configurations aimed at enhancing its performance in specific applications. These include renewable energy systems (e.g., PV and wind), motor drives, active power filters, uninterruptible power supplies, smart transformers, and flexible AC transmission systems (FACTS) [108, 109].

Over time, various topological alternatives have been proposed to optimize specific converter characteristics. In particular, different CHB configurations have been

explored [110], as well as novel submodule (SM) topologies such as half-bridge and full-bridge implementations [111]. More advanced solutions include multilevel variants like the H-bridge NPC, ANPC, neutral-point piloted, FC, and clamp-double topologies [56]. These structures aim to address application-specific challenges such as capacitor voltage ripple mitigation and increased voltage level granularity.

Regarding modulation strategies, as deeply described in Chapter 2, several PWM techniques have been developed for CHB-based converters [14, 112]. Among the most widely adopted are PS-PWM and LS-PWM. In systems with a high number of submodules, staircase-based modulation methods also represent a compelling alternative due to their implementation simplicity and reduced switching losses.

A more recent trend in the literature focuses on enhancing the parallelism within converter architectures through interleaved topologies. Interleaving, commonly applied in power electronics to reduce output current ripple and increase current handling capability, has been used in DC-DC and MMC systems to maintain high performance and modularity [113, 114]. Notable examples include an interleaved two-phase quasi-three-level DC-DC MMC with coupled inductors [115], and an interleaved DC-DC MMC for utility-scale PV applications [116]. Additionally, interleaved-stage AC-DC converters have been proposed for railway traction systems operating at medium voltage levels [117].

While most of these works implement interleaving at the system or leg level, recent studies propose a finer-grained approach by integrating interleaving directly within the submodules. For instance, the authors of [118, 119] present an MMC topology based on interleaved submodules, where each SM includes multiple internal converter legs modulated via interleaved carriers. This design not only increases output current without sacrificing modularity, but also improves waveform quality and enables the use of standard, low-current power semiconductors.

Building on these concepts, the present work proposes an interleaved CHB (I-CHB) architecture featuring submodules composed of multiple full-bridge cells

connected in parallel across a shared DC link and coupled on the AC side through interleaving inductors. This configuration enhances current-handling capability while allowing the use of lower-rated, cost-effective IGBTs. Furthermore, the interleaving introduces a level multiplication effect through phase-shifted carrier modulation. The proposed architecture is experimentally validated and benchmarked against the conventional CHB topology, with a focus on output voltage levels and harmonic performance in single-phase configurations.

6.2 Interleaved CHB submodule architecture

6.2.1 Overview of the conventional CHB cell

As deeply described in the previous chapters, the conventional CHB converter architecture is built upon the series connection of N full-bridge submodules (or cells), each powered by an independent DC voltage source V_{DC} [9]. This modular configuration is widely adopted in both single- and three-phase systems for synthesizing multilevel AC output voltages. A schematic of the conventional single-phase implementation is shown in Fig. 6.1. The principal benefits of this structure are its scalability, improved fault tolerance, and the inherent reduction in electrical and thermal stress experienced by individual power components. Each submodule operates as a full-bridge inverter under unipolar modulation, generating three discrete voltage levels: V_{DC}, 0, and $-V_{DC}$. The output AC voltage of the converter is the

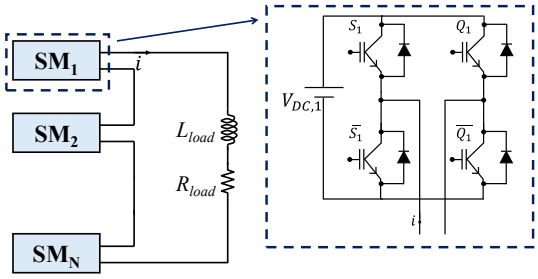


Figure 6.1: Standard CHB configuration with full-bridge submodule.

aggregate of the voltages produced by the individual submodules. To enhance the number of output levels and improve waveform quality, the PS-PWM technique is typically employed. This approach introduces a phase displacement of $T_{\text{sw}}/(2N)$ between the carrier signals of adjacent submodules, where T_{sw} denotes the PWM switching period. As a result, the theoretical maximum number of output voltage levels becomes:

$$\mathcal{L} = 2N + 1 \,. \tag{6.1}$$

However, the effective number of voltage levels also depends on the modulation index m, which is defined as $m = V_{AC}/(NV_{DC})$, where V_{AC} is the amplitude of the desired AC output. The range of achievable levels is constrained by:

$$3 \leq 2\lceil Nm \rceil + 1 \leq \mathcal{L} \,. \tag{6.2}$$

The maximum level count is achieved only when $m > 1 - \frac{1}{N}$.

For clarity, this work focuses solely on sinusoidal PS-PWM modulation. An illustration of this technique using three submodules ($N = 3$) is provided in Fig. 6.2. The use of phase-shifted carriers not only increases the number of available voltage levels, thus improving THD, but also introduces a beneficial frequency multiplication effect, pushing switching harmonics toward higher-order frequencies where they are less detrimental to system performance.

Due to the symmetrical nature of PS-PWM, power delivery is naturally balanced across the submodules and their associated DC sources. This characteristic makes PS-PWM preferable over other level-shifted schemes such as PD, POD, and APOD [120]. Nonetheless, optimal implementation requires a centralized control system capable of maintaining precise carrier phase displacement and dynamically adapting to variations in the number of active submodules. Furthermore, typical closed-loop control systems necessitate current sensing on the AC side (per phase)

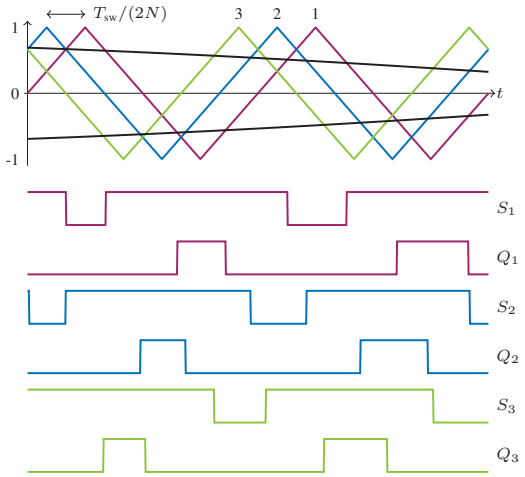


Figure 6.2: PS-PWM carrier-based implementation in case of $N = 3$. Switch nomenclature from the CHB of Fig. 6.1.

and voltage sensing for each individual DC link.

6.2.2 Proposed interleaved CHB submodule

The proposed I-CHB converter architecture introduces an enhanced submodule configuration aimed at increasing the converter's ampacity while preserving modularity and waveform quality. Each submodule in this architecture consists of K full-bridge inverters connected in parallel on the DC side to a common voltage source V_{DC}, and magnetically coupled on the AC side through interleaving inductors L_I. A schematic example for $K = 2$ is depicted in Fig. 6.3. This configuration enables the

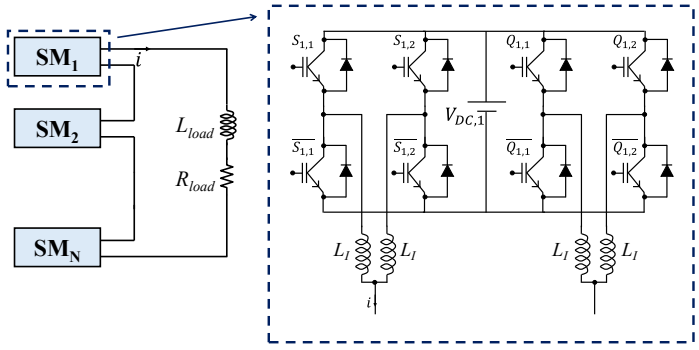


Figure 6.3: Proposed I-CHB configuration with interleaved full-bridge submodule. Example with $K = 2$.

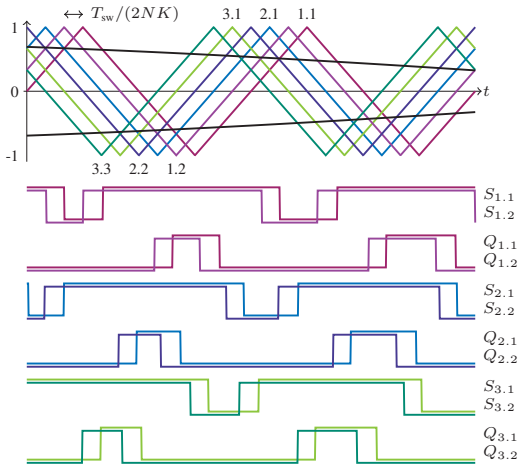


Figure 6.4: PS-PWM carrier-based implementation in case of $N = 3$ and $K = 2$. Switch nomenclature from the I-CHB of Fig. 6.3.

use of lower current-rated IGBTs and improves current handling capability without requiring an increase in the number of isolated DC sources.

To exploit the benefits of interleaving, an internal carrier phase shift of $T_{\text{sw}}/(2NK)$ is introduced among the K full-bridge carriers within each submodule, where T_{sw} denotes the PWM switching period. This modulation strategy, illustrated in Fig. 6.4, results in a level multiplication effect that increases the number of output voltage levels up to:

$$\mathcal{L} = 2NK + 1\,, \tag{6.3}$$

compared to the conventional CHB maximum of $2N + 1$. The effective number of levels remains dependent on the modulation index m, following:

$$3 \leq 2\lceil NKm \rceil + 1 \leq \mathcal{L}\,, \tag{6.4}$$

with $m = V_{AC}/(NV_{DC}) \in [0, 1]$, and V_{AC} the peak AC output voltage. Notably, the expressions (6.3) and (6.4) converge to the conventional CHB limits when $K = 1$.

Moreover, the interleaved and phase-shifted switching pattern applied to the FB cells within each SM effectively increases the equivalent switching frequency

experienced by the load to the value:

$$f_{\text{eq}} = 2KNf_{\text{sw}} \,, \tag{6.5}$$

without increasing the switching stress on individual devices. This emulated high-frequency behavior enhances waveform quality and reduces filtering requirements; increment of f_{eq} leads to a reduction of the WTHD.

6.2.3 Bill of Material: Transducers, Magnetics, and Switches

Despite the added complexity, the proposed architecture maintains the same sensor requirements as the standard CHB. Each submodule shares a common DC source, so no additional DC voltage sensing is needed. Although each submodule contains $2K$ internal switching legs, it is sufficient to sense a single AC current per phase to ensure full observability, as detailed in [119].

Each SM contains $2K$ internal inductors L_I used for interleaving, leading to a total installed inductance in every phase of $L_{\text{tot}} = 2NKL_I$. On the other hand, the load experiences an equivalent inductance:

$$L_{\text{eq}} = \frac{2N}{K} L_I \,. \tag{6.6}$$

At a first glance it might look like that the proposed solution magnetics present larger volume and weight. Although this is certainly true, it should be pointed out that to achieve the same level count and ampacity with conventional CHB with phase/leg interleaving it would be necessary to provide every phase with $S_{\text{dc}} = NK$ isolated DC sources instead of $S_{\text{dc}} = N$ leading to a broader BOM.

Similar considerations can be carried out concerning switch count. In fact, the total number of installed IGBTs in every phase is $Q_{\text{sw}} = 4NK$ meaning K time more power switches than in a conventional CHB; clearly, every switch present

a current rating roughly K time smaller. On the other hand, conventional CHB with phase/leg interleaving present the same amount of switches as the proposed solution. Finally, if compared with CHB arrangements with multilevel submodules like NPC- or FC-based H-bridge, the proposed solution employs roughly the same number of switches (note that NPC presents clamping diodes, FC employs additional capacitors, and both require multiple isolated drivers) and it achieves the same level multiplication effect while increasing converter ampacity. Of course, differently from multilevel submodules, every switch of the proposed I-CHB presents a voltage rating of V_{DC}.

6.3 Comparison and discussion

To validate the operational behavior of the proposed topology, numerical simulation results are subsequently presented comparing the following five relevant CHB arrangements:

- **N3K2f3:** proposed I-CHB considering $N = 3$, $K = 2$, $L_I = 1$ mH, $V_{DC} = 150$ V, and $f_{\text{sw}} = 3$ kHz. In this configuration $L_{\text{eq}} = 1$ mH, $L_{\text{tot}} = 12$ mH, $\mathcal{L} = 13$, $f_{\text{eq}} = 36$ kHz, $Q_{\text{sw}} = 24$, and $S_{\text{dc}} = 3$;
- **N3K2f1.5:** is equivalent to **N3K2f3** with the sole difference of having $f_{\text{sw}} = 1.5$ kHz and therefore $f_{\text{eq}} = 18$ kHz;
- **N6K1f3:** conventional CHB considering $N = 6$, $K = 1$, $V_{DC} = 75$ V, and $f_{\text{sw}} = 3$ kHz. To have the same equivalent inductance as the other cases, an external filter of $L_{\text{F}} = 3$ mH should be considered. Also in this case $\mathcal{L} = 13$, $f_{\text{eq}} = 36$ kHz, and $Q_{\text{sw}} = 24$. However, the number of isolated DC sources is $S_{\text{dc}} = 6$ while $L_{\text{tot}} = 3$ mH;
- **N3Kp2f3:** conventional CHB considering $N = 3$, $K = 1$, $V_{DC} = 150$ V, and $f_{\text{sw}} = 3$ kHz. However, in this case 2 parallel IGBT are considered within

every submodule. Also in this case $Q_{\text{sw}} = 24$, $S_{\text{dc}} = 3$, $L_{\text{F}} = 3\,m\text{H}$, and $L_{\text{tot}} = 3$ mH. However, is evident that $\mathcal{L} = 7$ and $f_{\text{eq}} = 18$ kHz anticipating mediocre harmonic performances;

- **N3Ke2f3:** 2 conventional CHB considering $N = 3$, $K = 1$, $V_{DC} = 150$ V, and $f_{\text{sw}} = 3$ kHz externally coupled in interleaving at the phase level employing $L_E = 6$ mH. Also in this configuration $L_{\text{eq}} = 3$ mH, $L_{\text{tot}} = 12$ mH, $\mathcal{L} = 13$, $f_{\text{eq}} = 36$ kHz, and $Q_{\text{sw}} = 24$. However, likewise **N6K1f3** the number of isolated DC sources is $S_{\text{dc}} = 6$.

All the above parameters have been collected in Table 6.1. Note that inductance and frequency values have been chosen with the sole purpose of enabling a straightforward comparison, and the displayed values are not intended to represent any specific and realistic design. As is visible, designs share common figures of merit and are particularly effective in highlighting the benefits and drawbacks of the proposed I-CHB. Specifically, in all the cases the modulation index is set to 0.9 to ensure the maximum number of levels and the same value of V_{AC} is considered. As a consequence, **N6K1f3** presents a smaller V_{DC} (i.e., 75 V instead of 150 V) in virtue of the larger number of submodules. To enable a fair comparison, in all the cases the same switches count and equivalent inductance is considered.

All the CHB arrangements from Table 6.1 have been simulated on PLECS (Plexim GmbH) and the open circuit output voltage is displayed in Fig. 6.5. All the configurations, with the exclusion of **N3Kp2f3**, present 13 levels with amplitude 75 V and are characterized by the same THD of 11 %. Although visually very similar, **N3K2f1.5** presents the first harmonic cluster around the equivalent switching frequency 18 kHz instead of 36 kHz. Such different harmonic behavior is reflected also on the WTHD which assumes the value 0.024 % instead of 0.012 % and it is motivated by the smaller switching frequency, i.e., 1.5 kHz. It is interesting to notice that the level count although identical is caused by strongly different phenomena.

Table 6.1: CHB arrangements comparative analysis: per phase main parameters

Description	**Symbol**	**N3K2f3**	**N3K2f1.5**	**N6K1f3**	**N3Kp2f3**[†]	**N3Ke2f3**[‡]	**Unit**
Type of CHB	-	I-CHB	I-CHB	CHB	CHB	2×CHB	-
Number of SM in each phase	N	3	3	6	3	3	-
Number of FB in each SM	K	2	2	1	1	1	-
Maximum number of levels	$\mathcal{L}$	13	13	13	7	13	-
IGBTs count	Q_{sw}	24	24	24	24	24	-
Isolated DC sources count	S_{dc}	3	3	6	3	6	-
Switching frequency	f_{sw}	3	1.5	3	3	3	kHz
Equivalent switching frequency	f_{eq}	36	18	36	18	36	kHz
Individual SM voltage	V_{DC}	150	150	75	150	150	V
IGBTs voltage rating	V_{sw}	150	150	75	150	150	V
Modulation index	m	0.9	0.9	0.9	0.9	0.9	-
SB-level interleaving inductor	L_I	1	1	–	–	–	mH
Phase-level filtering inductor	L_F	–	–	3	3	–	mH
Phase-level interleaving inductor	L_E	–	–	–	–	6	mH
Equivalent inductance	L_{eq}	3	3	3	3	3	mH
Total installed inductance	L_{tot}	12	12	3	3	6	mH
Inductors current rating in per unit	I_L	1	1	2	2	1	p.u.
IGBTs current rating in per unit	I_{sw}	1	1	2	1	1	p.u.
Voltage THD	THD	10.54	10.66	10.54	22.24	10.54	%
Voltage WTHD	WTHD	0.01218	0.02439	0.01218	0.05192	0.01228	%

[†] 1 FB per SB but each constituted by 2 parallel IGBTs.
[‡] 2 externally parallelized CHB each constituted by 1 FB per SB.

Configurations **N3K2f3** and **N3K2f1.5** take advantage of the level multiplication guaranteed by the proposed I-CHB and discussed in (6.4). Similarly, conventional CHB in **N3Ke2f3** takes advantage of a level multiplication effect caused by the external interleaving inductors at the phase level. On the other hand, **N6K1f3** generates 13 levels in virtue of the greater amount of submodules N as per (6.2) and it is not characterized by any level multiplication effect.

Configuration **N3Kp2f3** presents the smaller BOM because characterized by only three submodules and a total installed inductance of 3 mH. However it presents the worst harmonic performances characterized by only 7 voltage levels and greater THD and WTHD. Such configuration should be operated with switching frequency to at least 12 kHz in order to reach a WTHD level close to the other counterparts but in any case the THD would not improve. Increasing the switching frequency of parallel IGBTs is not straightforward and it leads to commutation losses at least four times greater, caused by the higher switching event count but also by the smaller gate voltage necessary to keep a positive temperature coefficient [121]. On the other hand, one could install a filtering inductor of about 12 mH to achieve the same current ripple as the other configurations. Clearly the latter statement nullifies all the BOM benefits because it would require the same amount of the total installed inductance (i.e., 12 mH) as the proposed I-CHB aggravated by the greater current rating of such inductors.

Although the proposed configuration **N3K2f3** appears to have the same harmonic performances as the conventional arrangements **N6K1f3** and **N3Ke2f3**, its merit stems from the smaller BOM largely caused by the need for only 3 isolated DC sources rather than 6. This saving is enough to compensate for the larger total installed inductance that characterizes the interleaved submodule here proposed.

In virtue of the above discussion, the I-CHB class of converters appears to be a competitive solution in applications requiring good harmonic performances, relatively small switching frequency, and smaller overall BOM (i.e., accounting also

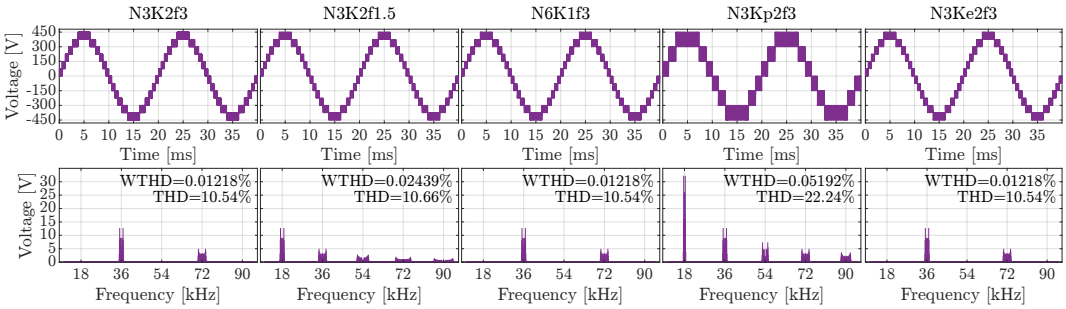


Figure 6.5: Numerical results of the CHB arrangements of Table 6.1. Open circuit output voltage: (top) time domain; (bottom) spectral components.

for the power electronics necessary to create the isolated DC sources).

6.4 Experimental validation

To experimentally validate the performance and benefits of the proposed I-CHB topology, a dedicated laboratory test bench has been developed, faithfully replicating the configuration depicted in Fig. 6.3. The complete experimental setup is shown in Fig. 6.6. The converter was controlled via an FPGA-based platform built around the NI sbRIO-9651 System-on-Module (SoM), which was programmed to implement the modulation strategy under investigation. The I-CHB was connected to a passive R-L load during testing. All relevant system and test parameters are comprehensively listed in Table 6.2.

First, the conventional PS-PWM technique has been implemented without introducing any interleaving between the PWM carriers. This configuration corre-

Table 6.2: Experimental setup parameters

Parameter	**Symbol**	**Value**	**Unit**
Cell voltage	V_{DC}	150	V
Switching frequency	f_{sw}	3	kHz
Fundamental frequency	f_{o}	50	Hz
Interleaving inductor	L_{I}	1	mH
Cell count	N	3	–
Parallel H-bridge count	K	2	–
Load inductance	L_{load}	18	mH
Load resistance	R_{load}	60	Ω

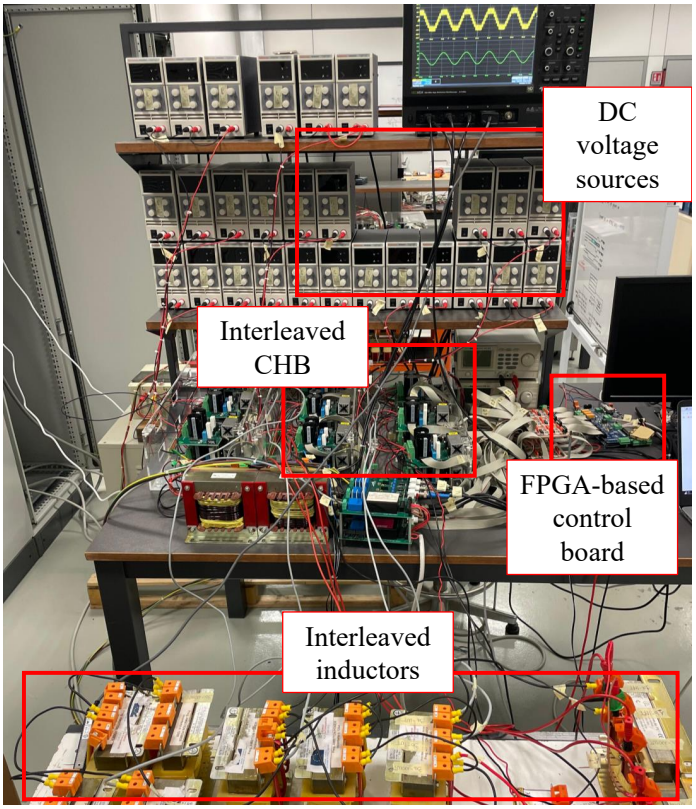


Figure 6.6: Experimental I-CHB setup with $N = 3$ and $K = 2$.

sponds to the standard CHB inverter. Subsequently, the proposed I-CHB has been implemented by introducing the internal phase shift between each carriers. This interleaving aims to enhance the harmonic performance by increasing the number of voltage levels. The corresponding output voltage and current waveforms, along with the voltage spectra, are illustrated in Fig. 6.7, for a set of modulation indexes ranging from 0.1 to 0.9. In particular, Figs. 6.7a and 6.7c show the conventional CHB waveforms for switching frequencies of $f_{sw} = 3$ kHz and $f_{sw} = 1$ kHz, respectively. Conversely, Figs. 6.7b and 6.7d present the corresponding waveforms and spectra for the proposed I-CHB under the same switching frequency conditions. This comparison clearly illustrates the improvements in waveform quality achieved through the application of the modulation technique. The level multiplication effect is particularly evident for all values of the modulation index and coherent with what was anticipated in (6.4). The corresponding values of THD and WTHD

are reported for all the spectra. To enable a fair comparison capable of highlighting different harmonic cluster locations, the WTHD is computed considering only switching harmonics.

In virtue of the parameter selection, it should be pointed out that $m = 0.9$ waveforms displayed in Figs. 6.7a and 6.7b are the experimental counterpart of configurations **N3K2f3** and **N3Kp2f3** respectively; see Fig. 6.5. As clearly visible, there is a one-to-one correspondence between experimental results and numerical case studies. In detail, the numerical THD was anticipated to be 10.54 % and 22.24 % for the I-CHB and the conventional CHB, respectively. The experimental results show comparable levels of THD with 12.53 % and 24.24 %, respectively. Similar considerations retain validity for the WTHD as well.

In all the cases, the first switching harmonic cluster is located as per the analytical discussion reported in (6.5) regardless from the value of modulation index. Specifically, conventional CHB shows the first predominant cluster accumulated around the equivalent switching frequencies $f_{sw} = 18$ kHz and $f_{sw} = 6$ kHz in the case of $f_{sw} = 3$ kHz and $f_{sw} = 1$ kHz, respectively. In a similar fashion, the proposed I-CHB shows the first predominant cluster accumulated around the equivalent switching frequencies $f_{sw} = 36$ kHz and $f_{sw} = 12$ kHz in the case of $f_{sw} = 3$ kHz and $f_{sw} = 1$ kHz, respectively.

As shown in Figs. 6.7a and 6.7b the proposed I-CHB experience about 50 % smaller THD in both switching frequency scenarios. On the other hand, the WTHD shown by the I-CHB is about 3-4 times smaller than the CHB counterpart. Interestingly, I-CHB operated at 1 kHz presents a WTHD comparable with the one of the CHB operated at 3 kHz. In all the cases, current waveform presents a minimal amount of current ripple as anticipated by the good values of WTHD.

Overall, experimental results showcase a clear enhancement in harmonic performances thanks to the adoption of the interleaved configuration across both switching frequency scenarios. This improvement becomes particularly pronounced at a

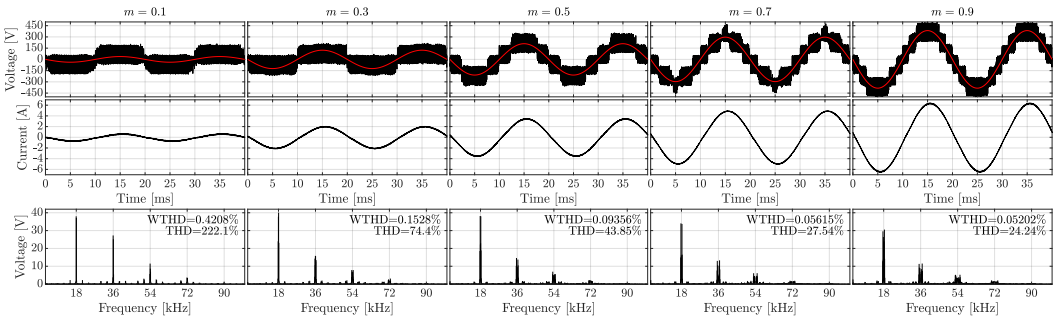
lower switching frequency (i.e., $f_{sw} = 1$ kHz), highlighting the suitability of the I-CHB topology for low-frequency operation. This finding is of particular significance, as it demonstrates that I-CHB not only benefits from the typical advantages of low switching frequency, such as reduced switching losses and diminished requirements for thermal management, but also counteracts the usual drawback of increased harmonic distortion. In fact, I-CHB manages to deliver improved output waveform quality even under conditions where harmonic performance is traditionally compromised.

6.5 Key outcomes

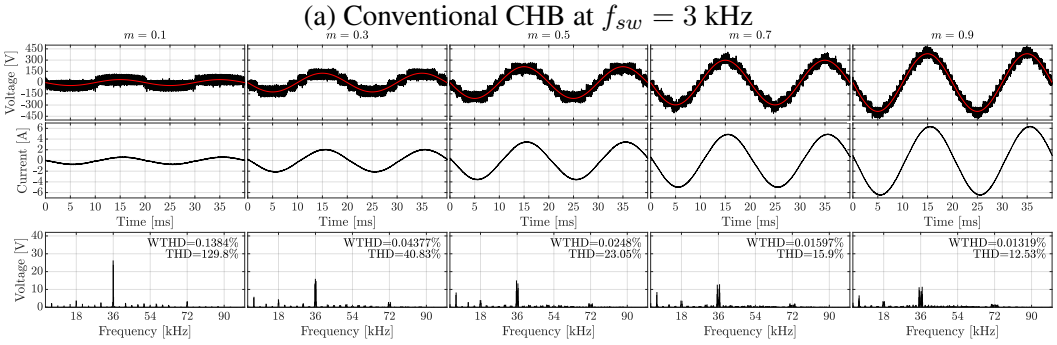
This chapter has introduced and analyzed a novel multilevel converter architecture based on interleaved full-bridge submodules. The proposed solution overcomes several inherent limitations of conventional CHBs in applications demanding both high output current and a large number of voltage levels. The proposed architecture enables new degrees of freedom in converter design, particularly in the horizontal scaling of submodules, and presents an effective compromise between performance, cost, and complexity.

The key contributions and findings can be summarized as follows:

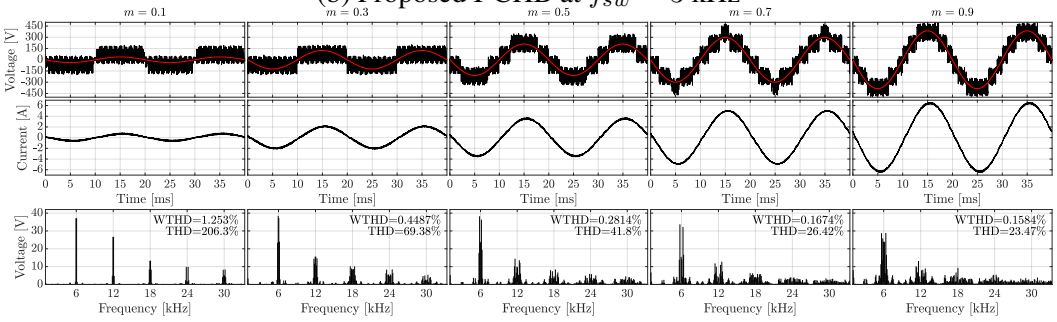
- A new CHB topology based on interleaved full-bridge submodules has been proposed, demonstrating enhanced scalability of current ratings without increasing the number of isolated DC sources.
- The architecture enables the use of lower-current, widely available power devices, improving cost-effectiveness and easing component sourcing compared to conventional high-current solutions.
- The interleaving mechanism synthetically multiplies the available voltage levels, resulting in improved harmonic performance at relatively low switching



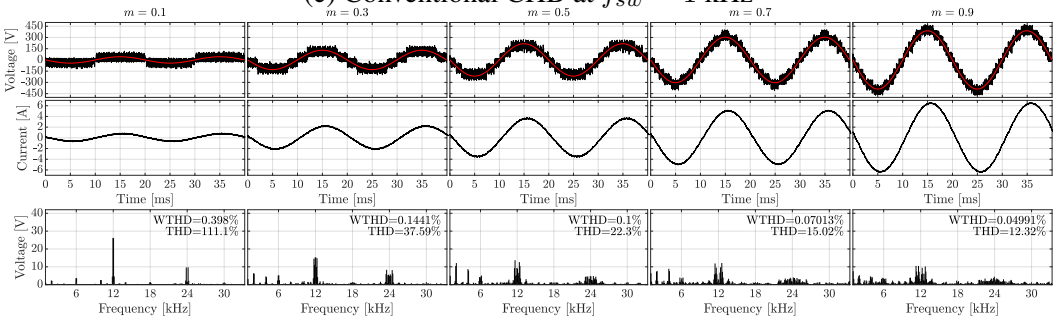
(a) Conventional CHB at $f_{sw} = 3$ kHz



(b) Proposed I-CHB at $f_{sw} = 3$ kHz



(c) Conventional CHB at $f_{sw} = 1$ kHz



(d) Proposed I-CHB at $f_{sw} = 1$ kHz

Figure 6.7: Experimental current and voltage waveforms under various m values for the conventional CHB and the proposed I-CHB.

frequencies.

- A dedicated carrier-based modulation scheme has been developed to fully exploit the interleaved architecture, enabling accurate waveform synthesis and effective phase-shifting among submodules.
- Experimental validation on a laboratory-scale prototype confirms the feasibility of the approach. Results show increased ampacity and significantly reduced THD and WTHD values compared to conventional CHB converters.

Chapter 7

Active Damping with Flying Capacitor Buck Converter: Modeling and Implementation

This chapter describes the research conducted during the six-month research period abroad at Eidgenössische Technische Hochschule (ETH) in Zurich, Switzerland, in the High Power Electronics (HPE) Laboratory. During this period, the research activities focused on the study of a different class of multilevel converters, thereby extending the scope of the general multilevel framework that constitutes the main theme of this PhD thesis. In particular, attention was devoted to the Flying Capacitor Buck Converter (FCBC), with a specific focus on the design and control of its three-level configuration, as depicted in Fig. 7.1. The work concentrates on the development of an active damping (AD) technique, which exploits the flying capacitor as a transient energy buffer to enhance the converter's dynamic performance. This method effectively eliminates the negative input-resistance phenomenon across a wide frequency range, significantly improving the stability of DC systems. Additionally, the proposed approach allows for more compact input filter designs without requiring extra damping components. The chapter includes simulation results

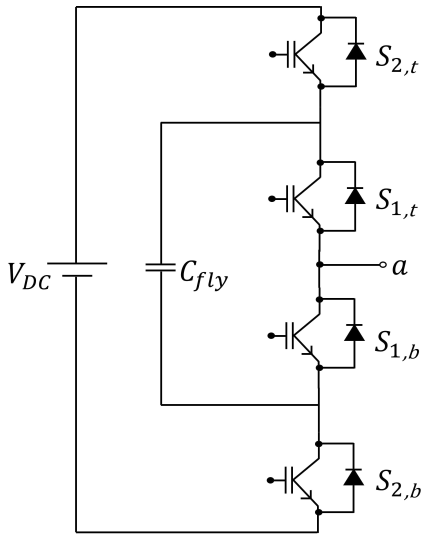


Figure 7.1: Scheme of a single-phase, three-level Flying Capacitor Converter.

demonstrating the improved control performance and input impedance characteristics enabled by this technique.

7.1 Literature background

Buck converters are extensively utilized in applications such as DC microgrids and onboard power systems for electric aircraft and marine vessels [122]. When operated under voltage regulation, the buck converter's control strategy inherently imposes a constant power load (CPL) behavior on its input side. This occurs because the controller continuously adjusts to maintain a stable output voltage by ensuring that the instantaneous input power matches the output power at all times. However, this dynamic leads to the well-known negative input resistance characteristic, which poses considerable challenges to the overall system stability, as documented in prior studies [123–125]. To mitigate these stability issues, passive damping (PD) techniques are frequently applied. Although PD approaches are effective, they tend to increase the number of components, physical size, weight, and introduce additional power losses due to the damping resistors. Moreover, variations in the external grid impedance or the source converter's output impedance cause shifts in the resonance

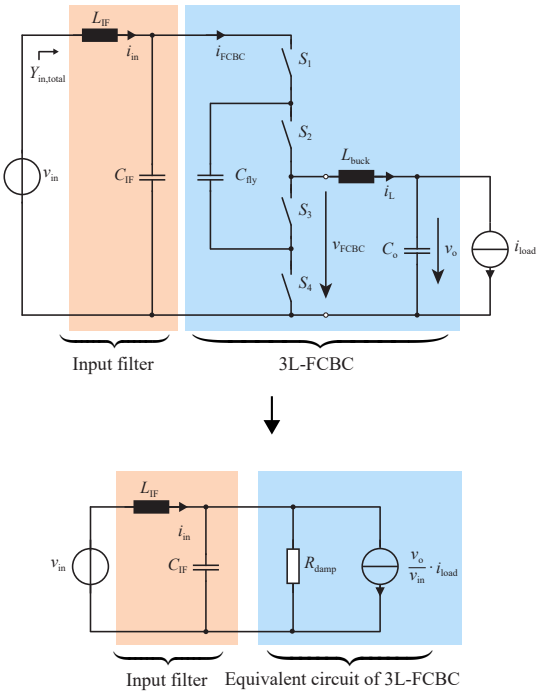


Figure 7.2: Considered buck converter with 3-level flying capacitor buck converter and its equivalent circuit with the proposed active damping controller.

frequency and the required damping level for the input filter, thereby limiting the robustness and adaptability of passive damping solutions.

While active damping strategies have been explored for conventional two-level buck converters, they often result in degraded output voltage regulation performance [122]. This limitation arises because traditional methods rely solely on the inductor current fluctuations for implementing damping, due to the absence of additional energy storage elements. In contrast, three-level FCBCs provide an additional degree of freedom through the flying capacitor voltage, enabling effective active damping without compromising voltage regulation. This chapter investigates how the flying capacitor can be utilized as a transient energy buffer to decouple the input and output power flows, thereby mitigating the negative input resistance phenomenon over an extended frequency range, as illustrated in Fig. 7.2.

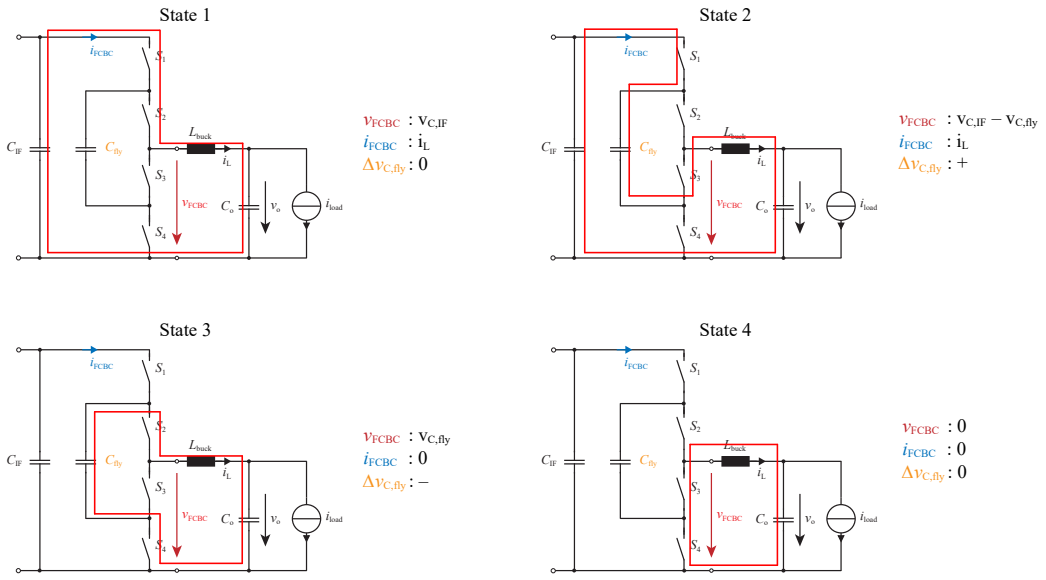


Figure 7.3: Four switching states of 3-level FCBC and their voltage/current characteristics.

7.2 3-level FCBC operation

7.2.1 Limitations of conventional operation

The three-level FCBC operates through four distinct switching states, as illustrated in Fig. 7.3. For each switching state, the output voltage v_{FCBC}, the current drawn from the input filter capacitor i_{FCBC}, and the voltage variation ($\Delta v_{C,fly}$) across the flying capacitor $v_{\text{C,fly}}$ are depicted in the figure. To regulate the flying capacitor voltage at a desired operating point, the controller typically balances the durations of switching states 2 and 3 during both transient and steady-state conditions. As a consequence, the output voltage v_{FCBC} and the input current i_{FCBC} become strongly coupled, resembling the behavior of a conventional two-level buck converter.

An illustrative example of this operation is shown in Fig. 7.4, where the normalized voltage reference signal is defined as $D_v = \frac{v_{\text{FCBC}}}{v_{\text{C,IF}}} = 0.6$. During the interval $0 < t < \frac{1}{f_{\text{sw}}}$ in the first half of Fig. 7.4, switching states 1, 2, and 3 are employed to synthesize the desired output voltage using phase-shift modulation, as described in [126]. This results in a current ratio $D_i = \frac{i_{\text{FCBC}}}{i_L} = D_v$, indicating a strong cou-

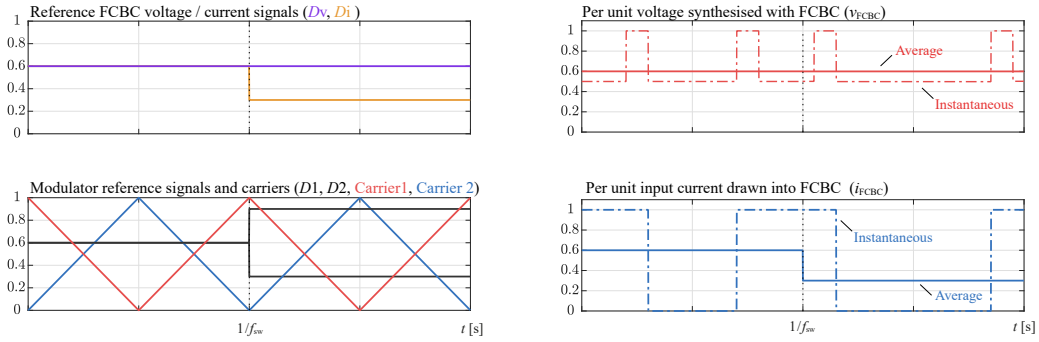


Figure 7.4: Conventional and proposed modulation of 3-level FCBC.

pling between the voltage and current. This coupling is the fundamental cause of the negative input resistance behavior observed in buck-type converters. When the input voltage drops, D_v increases to maintain v_{FCBC} constant in order to shape the required inductor current i_L. As D_v increases, both i_{FCBC} and the current ratio D_i also increase. In essence, the converter draws more current as the input voltage decreases, and less as it increases, leading to the well-known negative resistance characteristic.

7.2.2 Proposed operation with transient power decoupling

By leveraging the dynamic variations in the flying capacitor voltage, the FCBC topology enables transient power decoupling between the input and output ports of the converter. This feature introduces an additional degree of freedom in the system's operation, which can be strategically exploited for active damping purposes.

An illustrative case is presented in the second half of Fig. 7.4, corresponding to the interval $\frac{1}{f_{\text{sw}}} < t < \frac{2}{f_{\text{sw}}}$, where the FCBC operates with a normalized voltage reference $D_v = 0.6$ and a normalized current ratio $D_i = 0.3$. During this interval, the output voltage v_{FCBC} remains regulated, ensuring output performance equivalent to that of a conventional control scheme. However, due to the additional control flexibility offered by the flying capacitor, the input current i_{FCBC} drawn from the input filter capacitor can be modulated independently. This transient decoupling of volt-

age and current allows for the synthesis of a controlled damping current, which mitigates the negative input resistance effect over an extended frequency range. Moreover, it enables the suppression of oscillatory behavior in the input filter network.

In the following, the details of the proposed modulation strategy, which explicitly incorporates the flying capacitor voltage dynamics during transients to realize this enhanced control capability, are presented.

7.3 Proposed modulator

In conventional modulation schemes, the objective is limited to synthesizing the desired output voltage v_{FCBC} using a single reference signal D_v. In contrast, the proposed modulation strategy aims to regulate both the output voltage v_{FCBC} and the input current i_{FCBC} simultaneously. This dual-objective control introduces an additional layer of complexity, as both targets may not always be simultaneously achievable under all operating conditions. Since maintaining accurate output voltage regulation remains the primary control objective, the proposed modulator prioritizes tracking the voltage reference D_v. The current reference D_i is then shaped accordingly to ensure tight control of the inductor current, but only within the limits imposed by the voltage tracking constraint.

Under ideal conditions, specifically when the flying capacitor voltage equals half of the input filter capacitor voltage, the relationship between the achievable values of D_v and D_i can be analytically simplified. In this idealized scenario, switching states 1, 2, and 3 (as depicted in Fig. 7.3) are utilized when $D_v \geq 0.5$, whereas states 2, 3, and 4 are employed when $D_v \leq 0.5$.

In both cases, the durations of switching states 1 and 4 are fixed to satisfy the required output voltage D_v. The modulation of the current reference D_i is therefore realized solely by adjusting the relative durations of states 2 and 3. Consequently,

the achievable range of D_i is inherently dependent on the selected value of D_v. This dependency can be summarized as follows:

$$\begin{cases} 0 \leq D_v \leq 0.5 & : \quad 0 \leq D_i \leq 2D_v \\ 0.5 < D_v \leq 1 & : \quad (2D_v - 1) \leq D_i \leq 1 \end{cases} \tag{7.1}$$

When the flying capacitor is utilized as a transient energy buffer, its voltage deviates from the nominal value, typically half of the input filter capacitor voltage. This deviation must be taken into account in the modulation strategy to ensure accurate synthesis of both the desired output voltage ratio D_v and the input current ratio D_i. To achieve this, the duration of each switching state (D_{ST}) must be dynamically adjusted based on the instantaneous value of the flying capacitor voltage. These durations can be determined by formulating a linear system of equations subject to duration constraints, as presented below:

$$\begin{bmatrix} 1 & V_{C,\text{fly}}/V_{C,\text{IF}} & 1 - V_{C,\text{fly}}/V_{C,\text{IF}} \\ 1 & 1 & 0 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} D_{\text{ST1}} \\ D_{\text{ST2}} \\ D_{\text{ST3}} \end{bmatrix} = \begin{bmatrix} D_v \\ D_i \\ 1 \end{bmatrix} \tag{7.2}$$

The linear system can be solved analytically and the modulator reference signals (D_1,D_2) as shown in the left down side of Fig. 7.4 can be calculated as follows:

$$D_1 = D_i, \quad D_2 = (D_v - D_i)\frac{V_{C,\text{IF}}}{V_{C,\text{fly}}} + D_i \tag{7.3}$$

If the computed value of D_2 lies outside the permissible range $[0, 1]$, it must be saturated to the nearest boundary. In such cases, D_1 must be recalculated accordingly to ensure that the desired output voltage ratio D_v is still synthesized, while attempting to follow the input current reference D_i as closely as possible within the constraints of the system. The resulting saturated conditions lead to the following expressions

for the reference signals:

$$\begin{cases} \text{if } D_2 \leq 0 \quad : \quad D_1 = D_v \dfrac{V_{C,\text{IF}}}{V_{C,\text{IF}} - V_{C,\text{fly}}}, \quad D_2 = 0 \\ \\ \text{if } D_2 \geq 1 \quad : \quad D_1 = \dfrac{V_{C,\text{fly}} - V_{C,\text{IF}} D_v}{V_{C,\text{fly}} - V_{C,\text{IF}}}, \quad D_2 = 1 \end{cases} \tag{7.4}$$

In the following, a comprehensive control framework that generates the necessary D_v and D_i references is described. This approach ensures the output voltage regulation matches that of the conventional controller, while simultaneously achieving active damping of the input filter.

7.4 Control structure

The complete control architecture of the proposed strategy is depicted in Fig. 7.5. In this configuration, a conventional cascaded controller is employed to regulate the output voltage by accurately shaping the buck inductor current. This controller generates the reference voltage signal D_v. To enhance system performance, an additional control layer is introduced to compute the required damping current contribution. The overall reference signal D_i is then obtained by summing the damping current component with D_v. The switching sequences are ultimately synthesized by the novel modulation technique described in the previous paragraph, which simultaneously considers both D_v and D_i inputs.

Various techniques are available for determining the damping currents necessary to stabilize input filters [127]. Among these, model predictive control (MPC) offers a viable approach by optimizing the damping action based on the dynamic behavior of the input filter [128]. Nevertheless, to maintain simplicity and implementation practicality, this work adopts a damping current formulation that emulates the behavior of RC_d-based passive damping, as outlined in [129]. In general, pas-

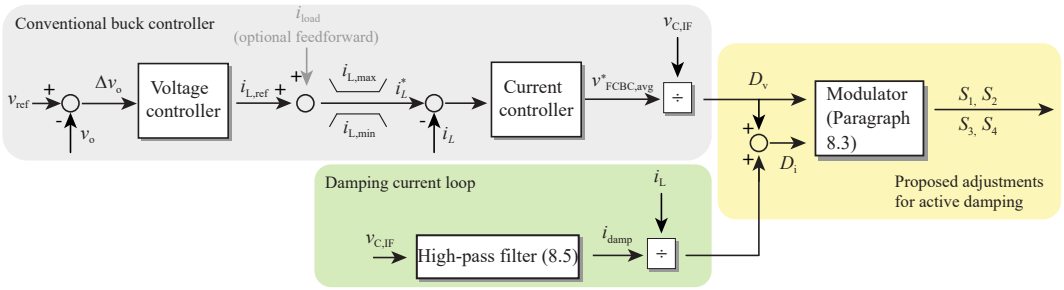


Figure 7.5: Proposed control diagram for achieving active damping (AD) with the FCBC approach. If AD is not implemented, the required damping current i_{damp} becomes zero, resulting in $D_v = D_i$, which corresponds to the behavior of a conventional controller.

sive damping strategies such as RL_d-parallel and RC_d-parallel configurations can be replicated through appropriate filtering of the input filter current $i_{L,\text{IF}}$ and the input filter capacitor voltage $v_{C,\text{IF}}$, respectively, as detailed in the following expressions:

$$i_{\text{damp}} = \begin{cases} \dfrac{L_f s}{L_d s + R_d}\, i_{L,\text{IF}} & \text{with } RL_d\text{-parallel} \\ \\ \dfrac{C_d s}{C_d s + R_d}\, v_{C,\text{IF}} & \text{with } RC_d\text{-parallel} \end{cases} \tag{7.5}$$

Traditional PD components are generally designed under strict constraints related to physical size and economic cost, as they involve the integration of additional hardware elements into the system. In contrast, AD leverages virtual components, thereby offering the flexibility to select component values purely based on desired system performance, independent of physical limitations. In this study, a relatively large value for C_d is deliberately selected to enhance damping performance. This choice allows for effective mitigation of the negative resistance effect over a wider frequency spectrum, by cancelling out the parallel negative input-resistance behavior of buck converter.

Table 7.1: System parameters of 3-level FCBC and input filter

Parameter	Symbol	Value	Unit
Rated power	P_{rated}	2	kW
Input voltage	v_{in}	400	V
Buck inductance	L_{buck}	128	μH
Input filter inductance	L_{IF}	1.27	mH
Flying capacitor capacitance	C_{fly}	20.83	μF
Switching frequency	f_{sw}	50	kHz
Output voltage	v_{out}	240	V
Output capacitance	C_{out}	20	μF
Input filter capacitance	C_{IF}	19.89	μF

7.5 Numerical validation

In the following, the performance of the proposed control strategy is assessed through detailed simulation studies. The effectiveness of the method is benchmarked against conventional control schemes by evaluating both time-domain responses under load transients and frequency-domain characteristics via input admittance analysis. Additionally, the system's large-signal transient stability is examined, and a more in-depth investigation is provided regarding power decoupling mechanisms and the inherent limitations in synthesizing the damping current with AD. The simulation setup is based on a three-level FCBC integrated with an input filter. The parameters employed for both the FCBC and the input filter are summarized in Table 7.1. The converter design follows the methodology outlined in [130], while the input filter is designed according to the specifications in [125], aiming to achieve an attenuation of 70 dB at the converter's switching frequency.

7.5.1 Time-domain load transient comparison

The simulation outcomes for three different control strategies are illustrated in Fig. 7.6. The first strategy adopts a conventional cascaded control architecture combined with passive damping to ensure system stability. This controller is implemented following the methodology in [131], utilizing PI controllers for both the voltage

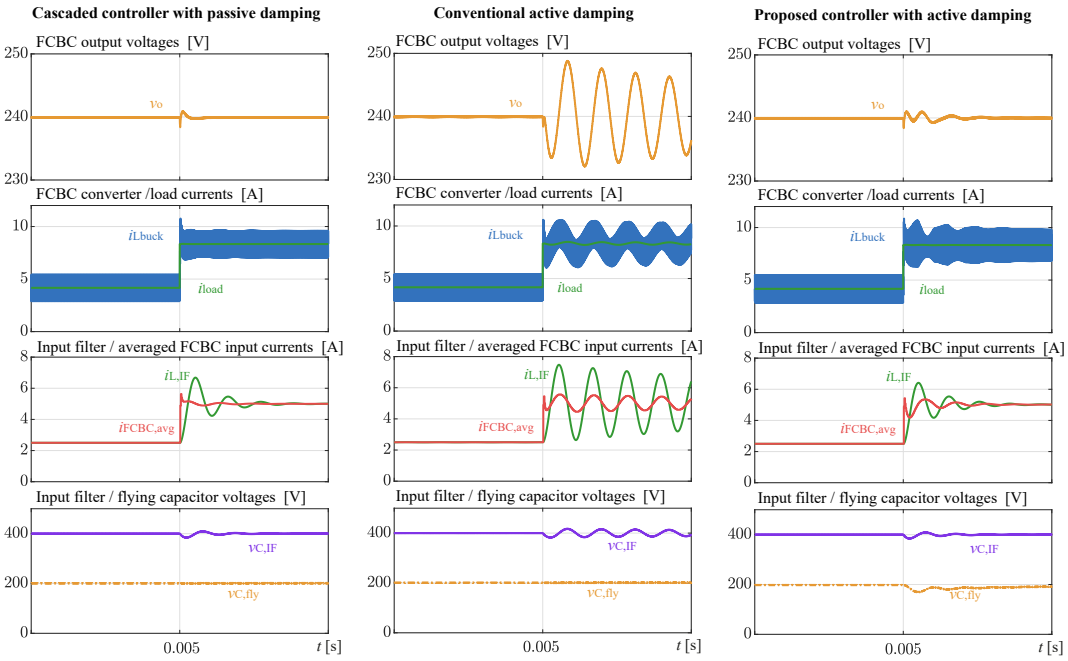


Figure 7.6: Comparisons of output voltage, damping current, and flying capacitor voltage results between control schemes.

and current regulation loops.

The second strategy eliminates passive damping components and instead embeds active damping directly into the current control loop, as proposed in [122]. Although this conventional active damping technique can mitigate oscillations, it introduces pronounced fluctuations in the buck inductor current and, consequently, in the output voltage. Its limited damping capability compromises output voltage regulation performance. The passive damping approach, on the other hand, delivers excellent output voltage control by precisely regulating the inductor current to compensate for voltage deviations during load transients. However, the achieved damping effect depends entirely on the inclusion of dedicated passive hardware components.

In contrast, the proposed active damping technique provides output voltage regulation performance that is comparable to the passive damping case. Moreover, the input filter current profiles are nearly identical for both methods, as the virtual damping resistance in the proposed method is designed to emulate the physical

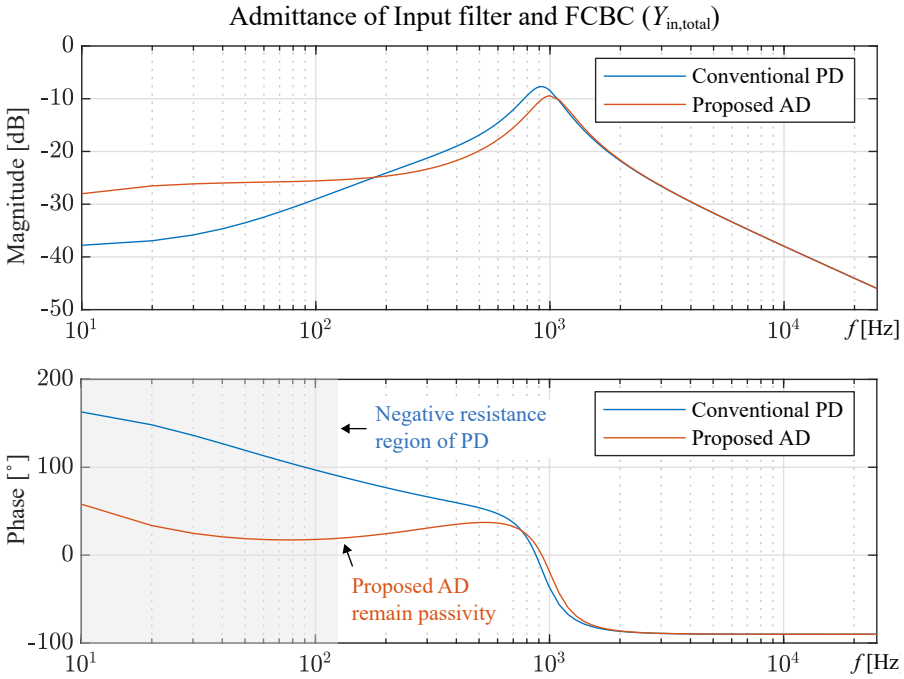


Figure 7.7: Comparisons of system admittance between PD and the proposed AD.

damping resistor used in the passive approach. A fundamental difference, however, lies in the behavior of the flying capacitor voltage. In the proposed method, noticeable fluctuations occur during load transients due to the use of the flying capacitor as an energy buffer in the active damping process.

7.5.2 Input admittance comparison

The passive damping technique is effective in attenuating resonant phenomena caused by the negative impedance characteristics of the converter, but only within the specific resonance frequency range for which the input filter is designed. Despite its localized effectiveness, this method does not fully address instability issues at lower frequencies, where the system input admittance continues to exhibit negative resistance behavior, as shown in Fig. 7.7. Such behavior may pose risks to system stability, particularly when interacting with external grid inductance or the output impedance of upstream converters.

In contrast, the proposed active damping strategy successfully suppresses the negative resistance effect across a broader frequency spectrum. This results in a system that maintains passive behavior over an extended frequency range, thereby substantially improving overall stability margins.

7.5.3 Power decoupling and limitation of damping current synthesis

Enlarged load step transient responses from no-load to half of the rated load is shown in Fig. 7.8. The resistive input impedance characteristic of the FCBC under the proposed control scheme is illustrated by the waveforms of $v_{C,\mathrm{IF}}$ and $i_{\mathrm{FCBC,avg}}$ shown in the first and second rows, respectively. As the load increases and $v_{C,\mathrm{IF}}$ drops, a corresponding decrease in $i_{\mathrm{FCBC,avg}}$ is observed, confirming the expected resistive behavior. However, in the blue-shaded region, a deviation from ideal damping current synthesis becomes evident. Ideally, $i_{\mathrm{FCBC,avg}}$ should follow the shape of $v_{C,\mathrm{IF}}$, scaled by the virtual damping resistor. Instead, an opposite curvature is seen, indicating a temporary limitation in synthesizing the required damping current. This occurs because the elaborated damping component, and hence D_i, becomes excessively large compared to the required D_v. Under such conditions, the modulator prioritizes the generation of D_v, which leads to a temporary increase in the effective damping resistance. This limitation is influenced by the load condition, since lighter loads demand larger D_i to achieve the same damping effect, which may exceed the modulator's feasible control region. Nonetheless, the system continues to exhibit resistive characteristics, and once D_i returns within the modulator's operational range, the correct damping current synthesis resumes, as seen immediately after the highlighted region.

The ability to generate damping currents relies on the flying capacitor, which acts as a temporary energy buffer during transients. As illustrated in the fourth row

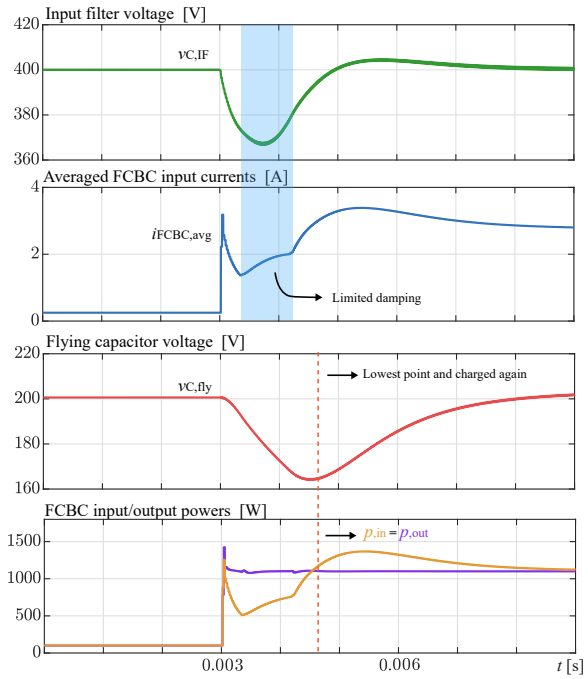


Figure 7.8: Limitation of damping current synthesis and relationship between the flying capacitor voltage and power decoupling. FCBC input power is $p_{\text{in}} = v_{C,\text{IF}} \cdot i_{\text{FCBC,avg}}$ and output power is $p_{\text{out}} = v_o \cdot i_{\text{buck,avg}}$.

of Fig. 7.8, this mechanism enables decoupling between input and output power during dynamic events. When the output power exceeds the input power, the flying capacitor voltage drops, indicating energy discharge. This behavior is consistent with a system exhibiting positive input resistance. The capacitor is then recharged to restore its nominal voltage once power balance is recovered. In steady-state conditions, input and output power converge, and the flying capacitor ceases to act as a buffer. In contrast, with conventional passive damping, the FCBC maintains continuous power flow balance at all times, keeping the flying capacitor voltage constant and equal to its nominal reference.

7.5.4 Large-signal transient stability against external grid inductance

The mechanism leading to instability in the proposed control method differs fundamentally from that observed in conventional approaches. In traditional schemes, instability primarily originates from the negative resistance behavior of the converter, making the full-load condition, where such negative resistance effects are most pronounced, the critical operating point for stability analysis. Under these circumstances, system input admittance plays a central role in evaluating small-signal stability.

In contrast, the proposed method effectively suppresses small-signal instabilities associated with negative impedance but introduces a different limitation: it does not inherently guarantee large-signal stability. This stems from the fact that the flying capacitor is not specifically dimensioned to handle significant energy exchange during transient power imbalances. During dynamic events, the flying capacitor must act as an energy buffer (either sourcing or sinking power temporarily) which places a demand on its energy-handling capacity. As a result, voltage stability of the flying capacitor can become a limiting factor. This issue is exacerbated in the presence of external grid inductance upstream of the input filter. The added inductance slows the dynamic response of the input filter current, thereby prolonging the period of power imbalance and increasing the energy burden on the flying capacitor.

Fig. 7.9 presents a comparative simulation that highlights system behavior with and without external grid inductance. When the inductance is present, the input filter current takes linger time to be increased, resulting in a longer power imbalance period. Consequently, the flying capacitor voltage exhibits a deeper drop, leading to noticeable degradation in output voltage regulation. Further increases in grid inductance may lead to complete system instability. It is worth noting, however, that the FCBC continues to exhibit resistive input impedance characteristics even

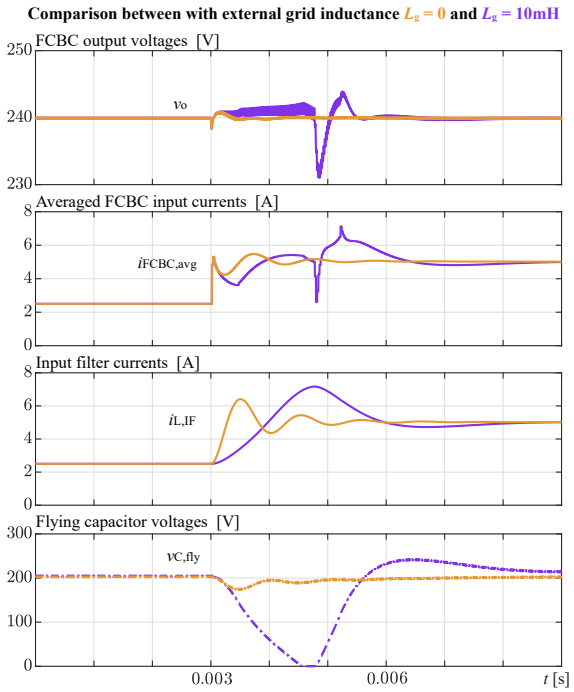


Figure 7.9: Comparative simulation results with and without external grid inductance for large-signal stability.

when external grid impedance is present. Therefore, no small-signal oscillations are observed under these conditions.

7.5.5 Large-signal transient stability against Flying Capacitor capacitance

Since the energy storage capacity of the flying capacitor represents the primary limitation to large-signal stability in the proposed control strategy, increasing its capacitance can significantly improve system robustness. This effect is demonstrated in Fig. 7.10, which presents a comparative simulation using a larger flying capacitor. Despite the presence of the same external grid inductance, the system remains stable, as the flying capacitor voltage stays close to its nominal value and the damping current is fully synthesized as intended.

It is important to note that the flying capacitor typically operates at approximately half the input voltage, whereas the damping capacitor C_d in passive damping

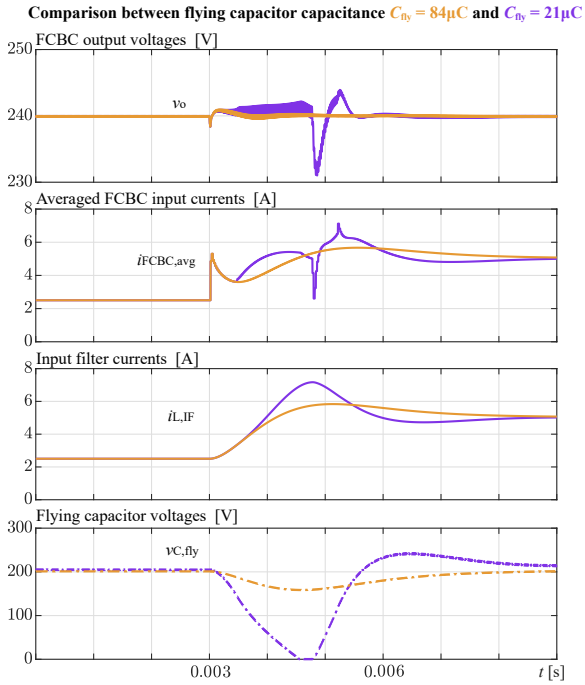


Figure 7.10: Comparative simulation results with basic and larger flying capacitor capacitance for large-signal stability. The external grid inductance $L_g = 10mH$ exists and the purple colored results are same as the results shown in Fig. 7.9.

schemes operates closer to the full input voltage. As a result, for the same capacitance value, the energy storage requirement, and consequently the physical volume of the flying capacitor is approximately 1/4 that of C_d. This needs to be considered if a system optimization for comparison is performed.

7.6 Key outcomes

This chapter presents and evaluates a novel active damping strategy for three-level FCBCs, aimed at improving stability and reducing filter size by using the flying capacitor as a dynamic energy buffer. The main insights and contributions are outlined below:

- A novel AD strategy for three-level FCBC is proposed, leveraging the flying capacitor as a transient energy buffer. The proposed AD method enables the

design of more compact and lightweight input filters by eliminating the need for additional passive damping components.

- The implemented control strategy ensures robust performance under varying external impedance conditions, which is particularly relevant for applications such as DC microgrids and on-board DC distribution systems.

- To ensure large-signal stability during power transients, proper sizing of the flying capacitor is essential in order to accommodate temporary power imbalances.

Chapter 8

Conclusions and Discussion

This thesis has presented a comprehensive investigation into advanced control and modulation strategies for multilevel power converters, encompassing both theoretical developments and extensive experimental validation. The work has demonstrated that modulation is not merely an auxiliary control layer but rather a core functional component that fundamentally determines the efficiency, reliability, and harmonic behavior of power electronic systems. Starting from the analysis of conventional PWM-based schemes, the research systematically identified their intrinsic limitations, particularly the impossibility of controlling each switching pulse independently, and subsequently developed an entirely new modulation paradigm capable of overcoming such constraint, named PPM.

The proposed PPM technique represents a significant contribution to the state of the art in converter control. By defining gate signals as the superposition of individually optimized pulses whose positions can vary within each control period, PPM introduces additional degrees of freedom that allow for finer harmonic shaping, lower switching losses, and enhanced dynamic response. Its effectiveness has been experimentally verified across multiple converter configurations, from single full-bridge modules to multilevel CHB systems, confirming its superior capability to suppress common-mode voltages, minimize leakage currents, and mitigate un-

balanced harmonic conditions. The resulting improvements in power quality and device lifetime underscore the practical relevance of the approach in both grid-connected and drive-oriented applications.

In parallel, the investigation into an interleaved CHB topology has demonstrated how architectural innovation, combined with dedicated modulation, can yield tangible improvements in scalability and efficiency. The proposed configuration successfully reduces the current stress on individual semiconductor devices and optimizes the use of available switching resources, thereby lowering system cost while maintaining high performance. These results reaffirm the essential interdependence between converter topology and modulation, emphasizing that meaningful progress in power electronics arises from their concurrent optimization.

The final contribution of this work, focused on the Flying Capacitor Buck Converter, extends the modulation-based approach beyond traditional AC–DC or DC–AC conversion contexts. By leveraging the flying capacitor as an active energy buffer, the proposed control and modulation strategies enhance the dynamic stability of DC systems and eliminates the need for bulky passive components. This outcome further validates the versatility of advanced modulation and control strategies as a key enabler for improving system performance, compactness, and sustainability.

In conclusion, the doctoral research presented herein provides both conceptual and practical advancements in the field of control and modulation for power electronic converters. The newly introduced PPM method, the modulation framework for interleaved CHB architectures, and the control strategy for the Flying Capacitor Buck Converter collectively form a coherent set of contributions that advance the understanding and practical implementation of efficient, reliable, and grid-compliant power conversion. The results open several promising directions for future developments, that will aim to further exploit the flexibility of PPM to enhance grid power quality through selective harmonic cancellation, active compensation of distortion components, and improved fault-tolerant operation under

abnormal or unbalanced conditions, thereby reinforcing its role as a versatile and resilient modulation framework for next-generation power conversion systems.

From an implementation point of view, the adoption of the proposed modulation strategies, particularly PPM and the EMA-based optimization, in real-time industrial controllers raises relevant challenges related to online computational effort, memory usage, deterministic execution, and achievable pulse-timing resolution. In addition, controller latency and switching frequency constraints may limit the direct applicability of optimization techniques in time-critical environments. These aspects suggest the extension of the experimental platform toward real-time validation on industrial digital signal processors under realistic operating conditions. Furthermore, the experimental setups considered in this work, including conventional inverter, CHB, I-CHB, and FCBC, capture a wide range of structural and operational characteristics commonly found in industrial power conversion systems, such as modularity, multi-level operation, power sharing, and voltage balancing. While not exhaustive, this set of configurations provides a representative and scalable validation framework, which can be further extended in future research to higher power levels, hardware-in-the-loop testing, and long-term operation scenarios typical of industrial applications.

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