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Results from CHIPIX-FE0, a Small-Scale Prototype of a New Generation Pixel Readout ASIC in 65 nm CMOS for HL-LHC

L. Pacher*, **E. Monteil, L. Demaria, A. Rivetti, M. Da Rocha Rolo, G. Dellacasa, G. Mazza, F. Rotondo, R. Wheadon**

INFN Sezione di Torino, Torino, Italy

A. Paternò, S. Panati

Politecnico di Torino and INFN Sezione di Torino, Torino, Italy

F. Loddo, F. Licciulli

INFN Sezione di Bari, Bari, Italy

F. Ciciriello, C. Marzocca

Politecnico di Bari and INFN Sezione di Bari, Bari, Italy

L. Gaioni, G. Traversi, V. Re

Università di Bergamo and INFN Sezione di Pavia, Bergamo, Italy

F. De Canio, L. Ratti

Università di Pavia and INFN Sezione di Pavia, Pavia, Italy

S. Marconi, P. Placidi

Università di Perugia and INFN Sezione di Perugia, Perugia, Italy

G. Magazzù

INFN Sezione di Pisa, Pisa, Italy

A. Stabile

Università di Milano and INFN Sezione di Milano, Milano, Italy

S. Mattiazzo

Università di Padova, Italy

Abstract - A prototype of a new-generation readout ASIC targeting High-Luminosity (HL) LHC pixel detector upgrades has been designed and fabricated as part of the Italian INFN CHIPIX65 project using a commercial 65 nm CMOS technology. This demonstrator, hereinafter referred to as CHIPIX-FE0, is composed of a matrix of 64 $\times$ 64 pixels with 50 μm $\times$ 50 μm pixel size embedding two different architectures of analog front-ends working in parallel. The final layout of the chip was submitted and accepted for fabrication on July 2016. Chips were received back from the foundry on October 2016 and successfully characterized. Several irradiation campaigns with X-rays have been accomplished during 2017 at Padova INFN and CERN EP/ESE facilities under different uniformity and temperature conditions up to 630 Mrad Total Ionizing Dose (TID). First sample chips have been also bump-bonded to 3D sensors provided by Trento FBK and preliminary characterizations with laser and radioactive sources have started. This paper briefly summarizes most important pre- and post-irradiation results, along with preliminary results obtained from chips bump-bonded to 3D sensors. Selected components of the CHIPIX demonstrator have been finally integrated into the large-scale RD53A prototype submitted at the end of summer 2017 by the CERN RD53 international collaboration on 65 nm CMOS technology.

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*Speaker.

1. Introduction

CHIPIX-FE0 is a small-scale ASIC demonstrator fabricated in a commercial 65 nm CMOS technology and addressing all key requirements expected for HL-LHC pixel detectors upgrades. It was designed in the framework of the INFN CHIPIX65 project and in close synergy with the CERN RD53 international collaboration on 65 nm CMOS, providing a fundamental intermediate step towards the implementation of the large-scale RD53A prototype [1].
The chip is composed of an array of 64 $\times$ 64 cells with 50 μm $\times$ 50 μm pixel size and integrates two different architectures of analog front-ends working in parallel, one synchronous [2] and one asynchronous [3]. An innovative region-based digital Centralized Buffering Architecture (CBA) grouping 4 $\times$ 4 pixels has been implemented in order to withstand 3 GHz/cm^2 hit rate and extended trigger latencies foreseen at HL-LHC [4].
A more exhaustive description of prototype implementation details can be found in [5]. In the following, a concise summary of latest experimental results is reported.

2. Summary of pre-irradiation and post-irradiation results

The test-setup is composed of a custom PCB hosting the chip under test. A dedicated firmware implemented on a Xilinx evaluation board supports all chip operations. It provides also a robust custom implementation of the Ethernet/UDP protocol for data-acquisition, which is handled by a NI/LabView user interface. Off-line data analyses are then performed using a set of Python/ROOT macros. Extensive pre-irradiation electrical tests validated expected chip functionalities [6].
All global DACs and the monitoring ADC placed at the chip periphery exhibit excellent linearity in agreement with simulations, providing reliable bias conditions and charge-injection characteristic for analog front-ends characterizations.
Analog front-ends performance have been assessed by means of S-curves obtained through charge and threshold scans. On the one hand, the synchronous front-end can reach a minimum threshold as low as 250 e^- with an Equivalent Noise Charge (ENC) of about 90 e^-. The measured threshold dispersion with autozeroing is about 100 e^- RMS, in agreement with the simulated latch dynamic offset. Low-noise performance have been therefore demonstrated despite continuous latch and region-logic digital switching activity. Additionally, fast ToT counting up to 320 MHz has been validated for a 5 ke^- injected charge. On the other hand, tests on the asynchronous front-end confirmed an expected minimum threshold of about 500 e^- with a noise level of about 80 e^-. The measured threshold dispersion is about 400 e^- RMS before digital trimming in agreement with simulations, reduced to 45 e^- RMS after per-pixel tuning.
Several irradiation campaigns have been performed on the CHIPIX-FE0 demonstrator with X-rays under different conditions at Padova INFN and CERN EP/ESE facilities: a non-uniform irradiation at room temperature up to 230 Mrad, a uniform cold irradiation at -20 °C up to 600 Mrad and a uniform irradiation at room temperature up to 630 Mrad. Samples were always biased at nominal operating conditions with continuous monitoring of proper chip configuration and data readout. Irradiated chips demonstrated to be fully-functional up to 600 Mrad TID, whereas after 630 Mrad the ASIC completely recovered its electrical functionality after one-week annealing at room temperature. Post-irradiation threshold and charge scans confirmed for both analog front-end architectures negligible degradation of low-noise and low-threshold performance.

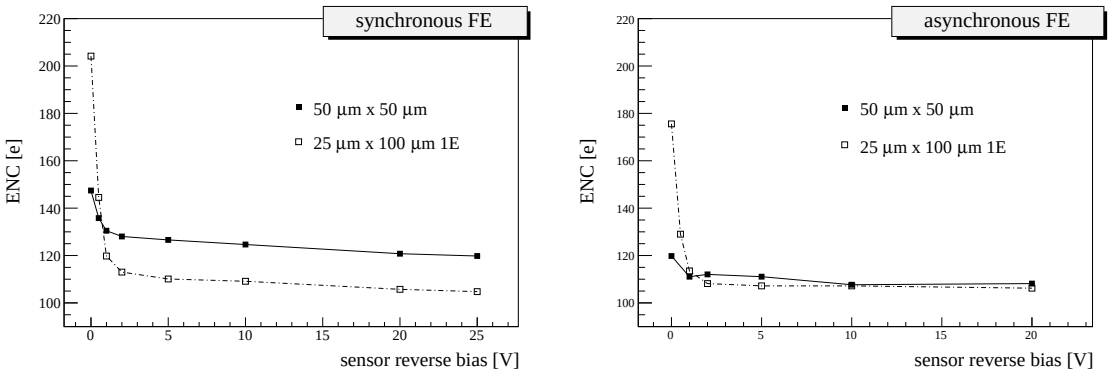

Figure 1: Preliminary results obtained with CHIPIX-FE0 demonstrator bump-bonded to 50 μm $\times$ 50 μm and 25 μm $\times$ 100 μm 1E 3D sensors designed and fabricated by Trento FBK. Measured ENC as a function of the sensor reverse bias for both synchronous (left) and asynchronous (right) front-end architectures.

3. Preliminary results with 3D sensors

Selected prototypes have been bump-bondend to 3D pixel sensors designed and fabricated by Trento FBK [7]. Bump deposition and flip-chip were performed at SLAC with both 50 μm $\times$ 50 μm and 25 μm $\times$ 100 μm 1E sensors. Chips were received back for characterization at the beginning of September 2017. This represented a major milestone for the entire CHIPIX65 INFN project, offering to the pixel community the first example of a complete readout chip in 65 nm CMOS technology coupled to such a kind of silicon detectors.
Proper sensors electrical connectivity with the chips have been validated by measuring the noise increase in analog front-ends connected to sensitive cells, revealing a high-quality bump-bonding despite the small chip size. A preliminary measure of the average ENC as a function of the sensor reverse bias is presented in Figure 1. Very promising and comparable results were obtained for both front-end architectures. Extensive characterizations using laser and radioactive sources have started.

4. Conclusions

Latest results from CHIPIX-FE0 have been shortly summarized. This small-scale prototype of a new-generation pixel readout ASIC in 65 nm CMOS represented a fundamental milestone towards the implementation of final chips that will be employed for pixel detector upgrades at HL-LHC.
Encouraging results were collected from all pre- and post-irradiation tests. Irradiation campaings performed with X-rays at -20 °C demonstrated that chips are fully-functional up to 600 Mrad. Low-noise and low-threshold performance satisfying all design specifications have been validated for both synchronous and asynchronous front-end architectures, certifying negligible degradation of analog key parameters after irradiation.

First samples have been bump-bonded to 50 μm $\times$ 50 μm and 25 μm $\times$ 100 μm 1E 3D sensors from FBK and characterizations are ongoing.
Improved versions of both front-end flavors and of the centralized region digital architecture have been included into RD53A prototype, along with additional selected analog blocks such as biasing DACs and bandgap voltage reference.
A new version of the prototype containing further improvements in analog front-ends has been re-submitted as part of the shared RD53A engineering run. Bump-bonding with planar sensors and characterizations of CHIPIX65 components that were embedded into the RD53A prototype are foreseen at the end of 2017.

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