A Modulator-less Beam Steering Transmitter based on a revised DDS-PLL Phase Shifter Architecture

G. D'Amato, G. Avitabile, G. Coviello and C. Talarico

***Abstract*—This paper details the design and implementation of a modulator-less beam steering transmitter based on a revised DDS-PLL phase shifter architecture. The proposed topology targets low data rate communications for Internet-of-Things systems, and has been demonstrated using an FPGA evaluation board and a custom PCB with four PLLs centered at 2.453-GHz. Measured system performance for an experimental 32-kbps data rate achieved through a 16-PSK modulation scheme are discussed. The proposed architecture is frequency independent, can be used in multi-band devices and has the potential for being integrated as an RF System-on-Chip.**

***Keywords*—direct digital synthesizer (DDS); phase-locked loop (PLL); modulator-less; beam steering; polar transmitter; low data rate communications; Internet-of-Things (IoT).**

I. INTRODUCTION

For a given spectrum, spatial multiplexing techniques are a key opportunity to allocate the ever-growing number of wireless communications between Internet-of-Things (IoT) devices. An effective strategy to achieve spatial multiplexing is the use of phased arrays. Phased arrays are antennas made up of at least two stationary elements and whose radiation pattern can be shaped and directed, through the phenomenon of constructive and destructive interference of electromagnetic waves, by assigning a convenient phase and amplitude relation to the currents fed to each of its radiators. The electronic control of phase and amplitude allows to implement directional radiation patterns that can be steered without the need for moving parts, even when starting from omnidirectional and non-moving individual elements. Electronic steering provides dramatic improvements both in radar and wireless communication applications. In radar applications, this is because electronic steering is not affected by inertia, as it happens with mechanical scanning.

In wireless communication systems, electronic steering allows to enhance directivity, so the consequent boosting in gain and spatial selectivity results in a significantly better energy efficiency. Compared to single element antennas, in most cases, the benefits coming from the use of phased arrays prevail over any cost and complexity consideration. In addition, for many critical applications phased arrays represent the only feasible option to meet gain or radiation pattern requirements. Spatial selectivity is the capability to implement radiation patterns that are characterized by a steerable main lobe. This means that, at the receiver end, undesired signals (a.k.a. interferers) that fall outside the width of the main lobe are significantly attenuated, whereas at the transmitter end, only a reduced amount of power is transmitted towards undesired directions, leaving the field free for other communications.

In literature, many solutions have been proposed to implement circuits that drive electronically scanning arrays. Among the solutions proposed there are extensive differences both in terms of complexity and cost. This depends on the strategy used to implement phase shifts, which is related to the region of the overall system architecture where the phase shifts are generated, a choice that typically depends on the bandwidth requirement for the phased array. Phased array architectures can be partitioned into three distinct categories, depending on the circuit path (RF, LO or IF) where phase shifters are located. Traditionally, RF phase shifting architectures are the ones that have been used most frequently. These architectures use only one mixer, and are characterized by just one LO distribution point. For these reasons, RF phase shifting architectures are the best at filtering strong interferers. This is because contributions coming from the various antenna are combined before the overall signal goes into the mixer stage, which is where interferers may cause the saturation of the input dynamic range. Working in the RF path means that the phase shifting devices operate at high frequencies, where parasitic effects are significant, and for this reason they typically require large on chip area. A common technique to implement RF phase shifters is that of using switched transmission lines. In [1], Maloratsky reviews many common PIN diodes-based phase shifting solutions. In [2], Sharma et al. proposes a 6-bit phase shifter targeting high-power airborne IFF applications that works in the 1030-1090 MHz range and is based on the loaded line topology. In [3], Karabey et al. propose a continuously tunable loaded line phase shifter for

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microwave applications based on liquid crystals as a tunable dielectric. In [4], Miyaguchi et al. propose a 5-bit phase shifter MMIC using series/parallel LC circuits working from 6- to 18-GHz. In [5], Kim et al. propose a monolithic TTD network, based on direct metal-to-metal contact RF MEMS switches, capable of operating from DC to 40-GHz. In [6], Jiang et al. propose a microwave photonic phase shifter, based on an optical phase modulator and a fiber Bragg grating, capable of providing continuous phase shifts from 20- to 30-GHz. In [7], Burla et al. propose a CMOS-compatible optical delay line for Ku-band satellite communications, based on four optical ring resonators.

LO and IF phase shifting architectures are based on the observation that the phase of an RF signal can also be changed indirectly. It is possible to change the phase of an RF signal intervening on any of the stages forming the RF signal. In IF phase shifting architectures, phase shifting is performed before up-conversion or after down-conversion. Phase shifters operating in the IF path operate at a much lower frequency than the ones operating in the RF or in the LO path, and thus their requirements are much more relaxed. However, IF phase shifting architectures require that each antenna is equipped with a phase shifter and a mixer. Moreover, these architectures are the worst at filtering strong interferers. This is because they perform the filtering after the received signal has gone through the mixer stage. In [8], Digdarsini et al. reported the realization of a FPGA-based digital beam forming (DBF) system capable to drive a phased array receiver made up of 16 elements. In LO phase shifting architectures, the LO is the only component that is phase shifted to perform beam steering. One of the main advantages of the architectures working in the LO path is that they do not interfere with the circuit topology of the signal path. For this reason, typical performance degradations (e.g. losses, non-linearity and noise) due to the insertion of phase shifters in the signal path can be neglected. Moreover, the bandwidth requirement for the phase shifting devices are more relaxed when compared to the requirements needed for devices operating in the RF path. Unfortunately, LO phase shifting architectures suffer from the same drawback of the IF phase shifting architectures, namely they require that each antenna is equipped with a phase shifter and a mixer. It must be noted that LO phase shifting architectures implement an approximation of the time delays that are required to drive the phased array. In fact, rather than actual time delays they introduce constant phase offsets. In [9], Lu et al. propose an LO-phase shifting receiver front-end, where a tunable transmission line loaded with switched capacitors is used to implement fine grained phase shifts in the first down-conversion stage. In [10], Hashemi et al. propose a fully integrated 24-GHz LO-phase shifting receiver for phased arrays, based on a 19.2-GHz CMOS ring VCO. TABLE I provides a summary of phase shifting architectures present in the literature. By comparing the existing architectures, it becomes clear that the LO phase shifting approach is the most promising for fully integrated phased arrays based solutions, and among other alternatives, carrier frequency independent topologies such as the ones based on the DDS-PLL architecture are the most suited for multi-band and agile devices.

Since typical IoT applications are characterized by low data rate communication needs, the DDS-PLL architecture (and its known variants) is a well-suited choice to embody the benefits of spatial selectivity into these devices. Moreover, the DDS-PLL architecture can also be used to implement communications based on the PSK modulation scheme without the need for additional hardware. This work investigates this opportunity, through the evaluation of an actual prototype capable of transmitting data up to 32-kbps by using a 16-PSK modulation scheme.

The rest of this paper is organized as follows. Section II introduces the standard DDS-PLL architecture as well as its known variants. Section III describes the implemented Beam Steering Unit (BSU) prototype as well as the theory of its operation as a modulator-less polar transmitter. Section IV presents the measurement setup and the experimental results obtained with the above hardware.

TABLE I
SUMMARY OF THE CITED PHASE SHIFTING ARCHITECTURES

Reference	Technique	Technology	Resolution	Frequency
[1]	RF path	Discrete PIN diodes	-	-
[2]	RF path	Discrete PIN diodes	6-bit	1030- to 1090-MHz
[3]	RF path	Liquid crystals	Continuous	12-GHz
[4]	RF path	Monolithic LC circuits	5-bit	6- to 18-GHz
[5]	RF path	Monolithic MEMS	4-bit	DC to 40-GHz
[6]	RF path	Fiber-based photonic circuit	Continuous	20- to 30-GHz
[7]	RF path	Integrated optics	Continuous	10.7- to 12.75-GHz
[8]	IF path	FPGA-based hybrid circuit	-	-
[9]	LO path	Monolithic 40-nm CMOS	6-bit	44- to 54-GHz
[10]	LO path	Monolithic 0.18-μm SiGe BiCMOS	4- to 5-bit	24-GHz

II. DDS-PLL Phase Shifter Architecture

The DDS-PLL architecture allows to combine the high frequency performance of PLL synthesizers with some of the unmatched characteristics of DDSs for the generation of agile LO signals. DDSs can achieve extraordinary frequency and phase resolutions (e.g. up to 10^{-6}-Hz), have an output frequency that can span over a range that can exceed 40 octaves (e.g. from 1-μHz to 150-MHz), can make extremely fast output frequency changes (even thousands of times faster than PLLs), can be synchronized to implement multiple DDS architectures and can be used to implement high-speed digital modulations. However, for certain applications, DDSs can also show substantial limitations, such as the impossibility to implement, under certain circumstances, exact frequencies and phases due to the quantization error inherent with their digital operation nature. Conversely, although continuous time PLLs can perform phase and frequency locking to the input reference that allows extremely precise synthesis of equally spaced frequencies at speeds that can be up to three order of magnitude faster than what DDSs are capable of, continuous PLLs are not designed to change their frequency instantaneously and their frequency resolution is far from the sub-Hz steps achievable through DDSs.

In literature, three main techniques have been proposed to implement DDS-driven PLLs, whose differences reside in the role that the DDS plays inside the loop [11]. One option is to put the DDS in the feedback path of the PLL, acting as a fractional divide-by-N stage. Another option is to employ the DDS as an offset frequency generator in an offset-PLL, that is a PLL where an analog mixer is inserted in the feedback path. Finally, the last option is to employ the DDS as the reference signal generator for the PLL. This last option is the simplest DDS-PLL architecture that can be implemented. In [12], Bonifanti et al. implemented a DDS-based PLL for a 2.4-GHz frequency synthesis that relies on the above discussed offset scheme. The authors reported a detailed analysis of the power consumption of the overall DDS-PLL solution, and noted that the largest contribution to power consumption was due to the DDS-DAC block. Since then, many revised topologies have been proposed to further reduce the complexity and power consumption of the original topology. In [13], Avitabile et al. proposed a revised DDS-PLL phase shifter (Fig. 1) based on accumulator registers, comparators (Fig. 2) and integer-N PLLs. In the work, the DDS subsystem is replaced by an all-digital circuit that, without any degradation of the PLL performance, feeds square waves rather than sine waves to the PFD input of the PLL. This is because in modern PFDs the phase and frequency mismatch detection is eventually operated by converting the input signals into square waves, and then working on their rising edges. For this reason, the proposed architecture gets rid of the unnecessary digital-to-analog transformation at the DDS output and manages to significantly reduce the complexity of the circuit topology. To understand the operation of the revised DDS-PLL proposed in [13] it is crucial to derive the formulation of the phase shift resolution at its output. Considering the duration of one period of the clock signal (T_{CLK}) assigned to the accumulator register

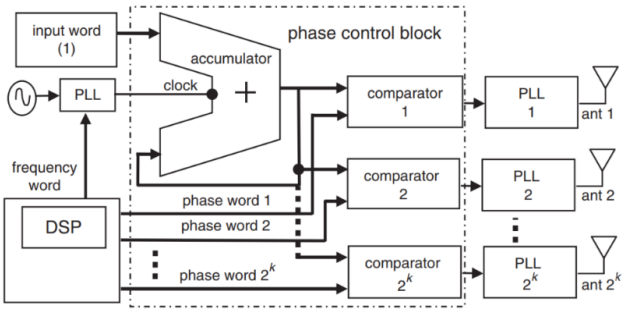

Fig. 1. Block diagram of the improved DDS-PLL architecture in [12]

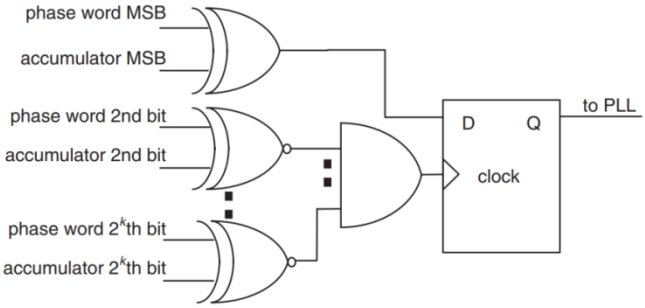

Fig. 2. Circuit diagram of the implemented comparators

and the duration of one period of the reference signal (T_{REF}) assigned to the PLLs, the minimum phase shift that can be assigned to the reference signals ($\Delta\varphi_{REF}$) in the above architecture is:

$$\Delta\varphi_{REF} = \frac{T_{CLK}}{T_{REF}} 2\pi \tag{1}$$

The corresponding phase shift $\Delta\varphi_{OUT}$ at the PLL outputs is:

$$\Delta\varphi_{OUT} = \frac{T_{CLK}}{T_{OUT}} 2\pi = N \frac{T_{CLK}}{T_{REF}} 2\pi = N \cdot \Delta\varphi_{REF} \tag{2}$$

where T_{OUT} is the duration of one period of the PLLs output sine waves. The above equations show that $\Delta\varphi_{OUT}$ is greater than $\Delta\varphi_{REF}$, and its magnitude depends on N, that is the ratio between the input and output frequency of the signals at the PLLs. However, due to the periodicity of sine waves:

$$\Delta\varphi = \Delta\varphi + m \cdot 2\pi \tag{3}$$

where m is an integer number. As long as the following ratio applies:

$$\frac{T_{REF}}{T_{CLK}} = 2^k \tag{4}$$

and the following relation holds true:

$$\Delta\varphi_{OUT} = \Delta\varphi_{REF} + m \cdot 2\pi = N \cdot \Delta\varphi_{REF} \tag{5}$$

it is possible to use an N divider in the feedback path without decreasing the resolution of the phase shifter, and thus:

$$N = 1 + m \cdot 2\pi \cdot \frac{1}{\Delta\varphi_{REF}} = 1 + m \cdot 2^k \tag{6}$$

The above relationship states that the output phase resolution

is preserved if N is an odd number. Even if the above derivation explains how to preserve the number of phases at the output of the phase control block, phases at the outputs of the PLLs are scrambled, and therefore we must derive the theoretical relationship that relates these output phases to the phase words assigned to comparators. From the above derivations, we find that:

$$\Delta\varphi_{OUT} = (PTW \cdot \Delta\varphi_{REF})\ mod\ 2\pi \tag{7}$$

where PTW is the phase words assigned to comparators. Any assigned PTW maps to a $\widehat{PTW}$ that quantifies the actual phase implemented at the output of the PLL through the following equation:

$$\widehat{PTW} = (PTW \cdot n)\ mod\ 2^k \tag{8}$$

where $n = M\ mod\ 2^k$. A lookup table (LUT) can used to store the 2^k correspondences, or real-time calculations can be carried out by inverting the above equation. The inverted relationship needed for carrying out real-time calculations is:

$$PTW = (\widehat{PTW} \cdot \hat{n})\ mod\ 2^k \tag{9}$$

where $\hat{n}$ is an integer number in the range $(0;\ 2^k - 1)$ and it is obtained by imposing the following condition:

$$(\hat{n} \cdot n)\ mod\ 2^k = 1 \tag{10}$$

Another revised circuit topology to implement DDS-PLL phase shifters has been proposed in [14]. In [14] synchronous delay lines (SDLs) with programmable lengths are used to implement the Phase Control Unit (PCU), namely the replacement for the DDS subsystem. The above architecture is capable of synchronously implementing a set of delays at its outputs. The principle behind the above architecture involves the management of just two signal paths: i) the signal to be delayed; ii) the system clock assigned to the flip-flops. The SDL circuit topology at the basis of the proposed phase shifter (Fig. 3) is a sequential logic circuit that consists of 2^n flip-flops, and n 2x1 multiplexers (where n is the desired phase shift resolution in bits). The 2^n flip-flops are arranged into n shift registers of 2^k flip-flops, where k is the position that each delay block covers into the SDL. The n multiplexers are assigned to each delay block to route, at its output, the logic level either at the input or at the output of its shift register, thus allowing programming the overall chain length based on a Phase Tuning Word (PTW) stored into the tuning register. Since the block in the highest k position merely implements a 180° phase shift, an XOR gate (acting as a controlled inverter) can be used in its place. The output of each SDL is fed to a pipeline flip-flop, to mitigate phase errors related to the physical routing of signal paths assigned to each PTW. Each flip-flop delays the reference clock signal at the input of the SDLs of one period of the clock signal (T_{CLK}). To synthesize phase shifts in the [0°; 360°) range, T_{CLK} must be related to the period of the reference clock signal (T_{REF}) as follows:

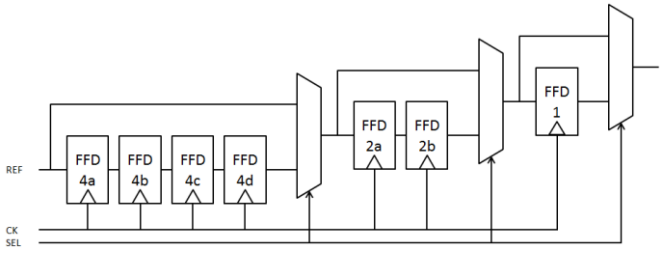

Fig. 3. A cascade of three delay blocks implementing the synchronous delay-line

$$T_{CLK} = \frac{T_{REF}}{2^n} \tag{11}$$

Using an SDL to drive the reference input of a PLL allows to set its phase in the same way the accumulator based variants do. This means that the PCU needs one SDL for each PLL it must drive, that is the number of channels that the BSU must be designed for.

III. BSU Prototype and Modulator-Less Polar Transmitter Theory of Operation

The implemented BSU prototype illustrated by this work (Fig. 4) has been presented for the first time in [15]. It is made up of three distinct subsystems, namely a Micro Controller Unit (MCU), a PCU and a Frequency Scaling Unit (FSU).

The MCU and the PCU have been synthesized on an FPGA whereas the FSU has been implemented as a custom daughter card specifically designed for the FPGA evaluation board. The MCU is an instance of the open source 8051 IP-Core from Oregano Systems. The PCU is made up of 4 SDLs with programmable lengths, designed to provide a phase shift resolution of 8-bits (corresponding to a phase tuning step as low as 1.40625°). The target FPGA device was the Altera EP4CE225F29C7 (114,480 logic elements) on the DE2-115 development board. The synthesis has been performed in Quartus II 14.1. The FPGA usage, in terms of Logic Elements (LEs), reported in the compilation report is less than 1%. Fig. 5 depicts the RTL netlist view of the synthesized PCU. The prototype has been configured to work with f_{CLK} and f_{REF}

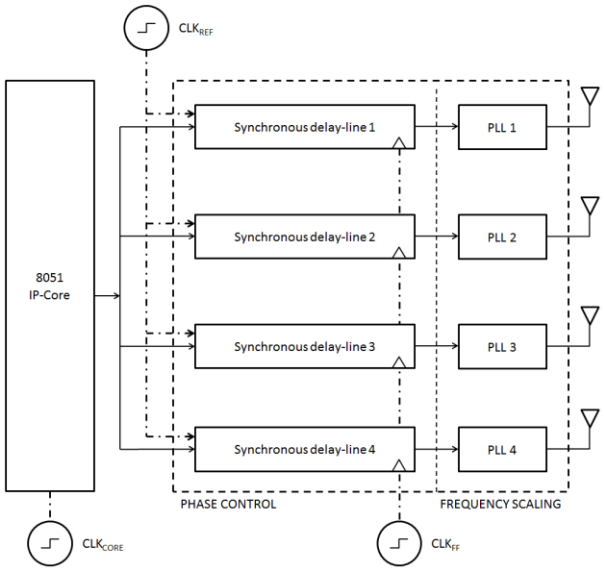

Fig. 4. BSU architecture implemented in this work

frequencies respectively equal to 256-MHz and 1-MHz (among other possible configurations). The full-digital portion of the above architecture, composed by the 8051 IP core and the PCU, is compatible with both FPGA and ASIC design flows. Instead of using a vendor-specific microprocessor IP cores, we have preferred the use of a processor that is distributed openly and freely in plain VHDL under the "GNU Lesser General Public License" (LGPL). A VLSI implementation of the selected 8051 IP core has been reported in [16] by Chu et al. The reported TSMC 0.18μm technology implementation occupies a die area of 1.96-mm^2.

The FSU subsystem is made up of 4 PLLs responsible for synthesizing the phase shifted LOs starting from the delayed reference signals generated by the PCU. In this prototype, the FSU is centered at 2.453-GHz. The PLLs are based on the ADF4118 from Analog Devices and the VCO190-2453TY from Sirenza. The PFD frequency has been set to 1-MHz. Being the ADF4118 an Integer-N PLL chip, with the above PFD frequency configuration, this prototype can synthesize sine waves equally spaced in the frequency domain, that are 1-MHz apart from one another. The loop bandwidth (LBW) has been set to 100-kHz through a passive second-order loop filter, a choice that will be further discussed in the next section. Fig. 6 is a photograph of the FSU hardware that has been fabricated for this work. The prototype has been implemented in the form of a custom daughter card for the DE2-115 evaluation board, and can be stacked to its expansion header. The FSU hardware accepts the reference signals for its PLLs from the expansion header of the host development board or from SMA connectors. The prototype size is 240-mm x 100-mm and its thickness is 0.8-mm. The distance between outputs is equal to 6.115-cm, namely $\frac{\lambda}{2}$ (where λ is the wavelength of the LO frequency, that is 2.453-MHz, in free space). This has been done to allow implementing the phased array by just connecting the antennas to the outputs.

Given that a beam synthesis and steering solution based on the evidence that the output phase of a PLL can be changed through a convenient delay of its reference signal has already been proposed in literature [17], in this work we focus on a modulator-less polar transmitter. If one of the PLL output phases is considered as a reference phase, φ_0, it can be said that some of its other output phases (related to an equal number of reference signal delays) can be interpreted as the symbols of a PSK constellation. In fact, each output phase shift from φ_0 can be interpreted as a rotation of the vector that represents the synthesized PLL output in the IQ plane. If a Look-Up Table (LUT) exists that can map this transformation (and it exists, since it is the same one constructed for the mutual phase shifts among PLLs), a modulator can be implemented exploiting the above BSU hardware; all it is needed is an operator that sums the phase rotation assigned to the PSK symbol α, to the phase shift β assigned to the beam steering (Fig. 7). The α angle changes with a frequency that is defined by the symbol rate of the communication, thus the transient response of the PLLs at each transition must extinguish in a fraction of the symbol time duration, a specification that ultimately depends on the loop bandwidth. The angle β can be interpreted as a phase offset that changes with a much slower frequency (its variation is only needed to reshape the radiation pattern). The phase rotations α, due to the transmission of the PSK symbols, do not affect beam steering. In fact, beam steering is related to mutual phase shifts at the BSU outputs, that only depend on β (α is equal for all outputs).

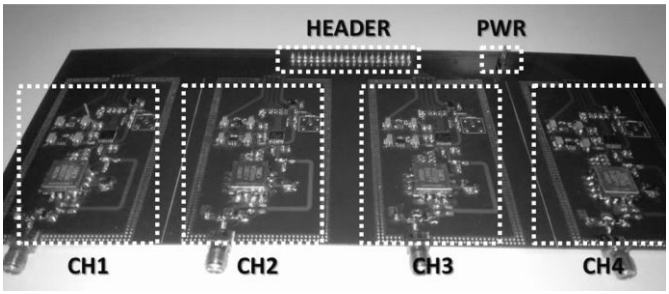

Fig. 6. Custom daughter card for the DE2-115 FPGA evaluation board implementing the FSU

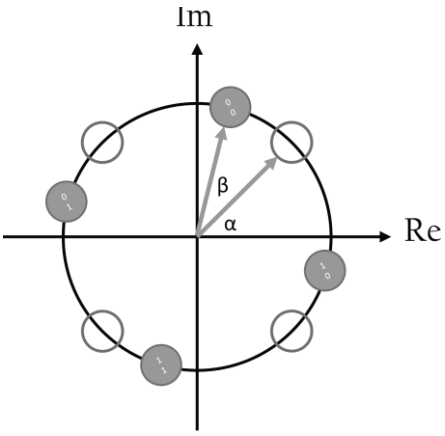

Fig. 7 – IQ plane representation of α and β

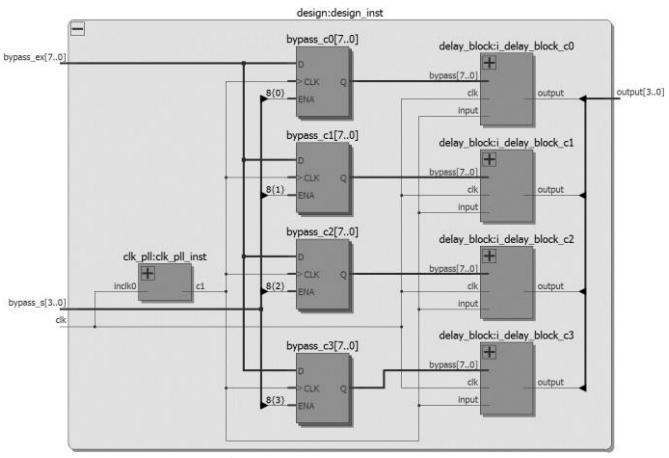

Fig. 5. RTL netlist view of the PCU entity

illustrating how the proposed BSU architecture can operate as

Being $B = [\beta_0, \beta_1, \beta_2, \beta_3]$ the vector of phase shifts to synthesize the desired radiation pattern, and α the phase

rotation assigned to the PSK symbol being transmitted, the resultant phase state vector for the array is $B' = [\alpha + \beta_0, \alpha + \beta_1, \alpha + \beta_2, \alpha + \beta_3]$. Thus, the configuration vector for the delay lines is $C = [\chi(\alpha + \beta_0), \chi(\alpha + \beta_1), \chi(\alpha + \beta_2), \chi(\alpha + \beta_3)]$ where χ is the transformation, operated through the LUT, that maps output phases to binary Phase Tuning Words (PTWs) in the PCU. The transformation is operated by finding the LUT pointer (*PTR*) that returns the PTW needed to obtain the $\alpha + \beta_i$ output phase, and then reading from that address the matching PTW. For a LUT where the PTWs are stored in memory for increasing output phases, the desired *PTR* is:

$$PTR = \text{round}\left(\frac{(\alpha + \beta_i) \bmod 360}{360} \cdot 2^8\right) \tag{12}$$

where PTR ∈ [0, 1, … 255], that is PTR is an 8-bit unsigned integer.

It must be noted that PTR can also be computed as follows:

$$PTR = a_1 + a_2 = \text{round}\left(\frac{\beta_i \cdot 2^8}{360}\right) + \frac{\alpha \cdot 2^8}{360} \tag{13}$$

where both addenda $a_{1,2} \in [0, 1, \ldots 255]$, that is the addenda are two 8-bit unsigned integers. In fact, $\beta_i \in [0°; 360°)$, and for any 2^n-PSK constellation ($n \in [1, 2, \ldots 8]$):

$$\alpha = m \cdot \frac{360}{2^n} \tag{14}$$

where $m \in [0, 1, \ldots 2^n - 1]$. This allows to lower the number of instructions needed to find the PTW, since no modulus operation is needed to compute the *PTR*.

IV. Measurement Setup and Experimental Results

The purpose of this section is to present the measurement setup and the experimental results obtained during the performance evaluation of the discussed BSU architecture. All measurements are taken at the outputs of the PCU and the FSU prototypes. The experimental results presented also include the evaluation of the architecture when it operates as a modulator-less beam steering transmitter. The qualification of the PCU and FSU output channels has been conducted using semi-rigid coaxial cables. The PCU output signals are square waves, characterized by a frequency of 1-MHz, a peak-to-peak amplitude of 3-V and a mean amplitude of 1.5-V. Fig. 8 depicts the block diagram of the measurement setup. The FSU outputs are high-frequency tones, characterized by a frequency of 2.453-GHz, and a typical output power level of 3-dBm on matched 50-Ω loads.

Fig. 9 depicts the block diagram of the measurement setup. The measurements were taken using a 4 GHz oscilloscope (a LeCroy WavePro 7300A) configured for 20-GSPS sampling rate. The clock signal assigned to the PCU was generated from an external clock jitter cleaner circuit based on the LMK04806B by Texas Instruments. Actual phase shifts as well as related phase errors have been quantified on the digitized output signals.

The following experimental results have also been used to perform a calibration of the LUT that inverts the PTW vs. phase shift relation needed to descramble the PLLs output phases. This has been done through a sorting routine that outputs a monotonically growing series of phases based on the theoretical formulation presented in Section II. To better match the correspondence between PTWs and PLLs output phases, for some of the PTWs values the LUT based on the theoretical formulation has been corrected. When working with the real hardware, the following relationship applies:

$$\Delta\varphi_{OUT} = \left(\frac{(\Delta t_{IN} + \delta) \cdot 360}{T_{REF}} \cdot M\right) \bmod 360 \tag{15}$$

where Δt_{IN} is, the expected delay applied to the reference signal and δ is an unknown delay error that depends on the desired phase output. This allows to overcome the need to quantify a-priori the value of δ. The value of parameter δ represents a deterministic phase error. Measurements were automated by using a MATLAB script assisted by an ad-hoc firmware executed on the MCU.

Fig. 10 depicts the PTW vs. output phase trans-characteristic at the PCU outputs whereas Fig. 11 depicts the PTW to output

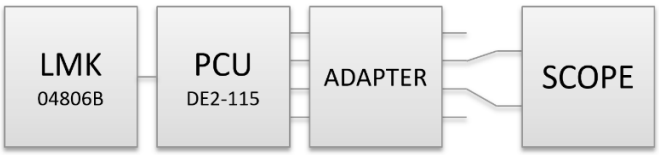

Fig. 8. Measurement setup employed during the qualification of the PCU outputs

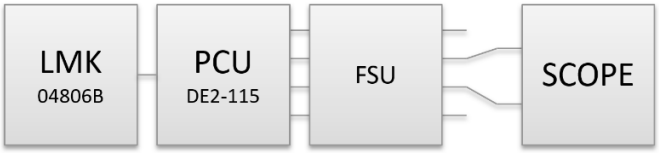

Fig. 9. Measurement setup employed during the qualification of the FSU outputs

phase error. Phase difference measurements have been averaged over 1000 samples. During the tests, one channel was used as the trigger source (and thus as the zero-phase reference signal), whereas the phase of the signal connected to the second channel was swept across the 256 PTWs. The following measurements were conducted over a time span of about 4.3 hours. The mean phase error across PTWs is extremely close to 0, and the mean standard deviation in the acquired phase difference samples is less than 0.0025°. The phase error is contained within the range [-0.01°; +0.01°]. Fig. 12 depicts the LUT address vs. the output phase trans-characteristic at the FSU outputs whereas Fig. 13 depicts the LUT address vs. the output phase error. Measurements have been performed following the same technique described before. The mean phase error across LUT addresses is very close to 0, and the mean standard deviation in the acquired phase difference samples is less than 0.01°. The phase error is contained within the range [-0.9°; +0.9°].

The qualification of the BSU architecture when it is acting as a modulator-less beam steering transmitter has then been also conducted. The prototype has been configured to transmit data according to a 16-PSK modulation scheme (4-bits per symbol). The symbol rate of the communication has been fixed to 8-kbaud (that is the symbol duration time for data transmission, a.k.a. UI, is 125 μs). Thus, the data transmission rate is:

$$R_b = 8\frac{\text{Kbaud}}{\text{s}} \cdot 4\frac{\text{bits}}{\text{baud}} = 32\text{kbps} \tag{16}$$

The baud rate of the communication is constrained by the loop bandwidth that, as reported in TABLE II, fixes the worst-case Time-To-Lock (TTL) at 1°. For the prototype presented in this work, the loop bandwidth is 100-kHz, thus the worst case TTL during a symbol transition is 24.5μs (in other terms the transient response of the loop is less than 19.6% of the UI). The measurement setup includes a direct-conversion receiver based on a TRF371125 IQ demodulator and the LO was tuned to match carrier frequency and phase.

During the measurements, the receiver was connected to the RF outputs of the BSU through a 4-way passive combiner and four semi-rigid coaxial cables with matched lengths (Fig. 14). This allowed to simulate the position of the receiver with respect to the transmitter as if it was broadside and in the far-field. The BSU was configured to transmit towards the receiver, with β_1, β_2, β_3 and β_4 set to the same value. A random sequence of bits was used to validate the transmission. Fig. 15 shows the received IQ signals before filtering. Fig. 16 shows the transient response of the PLLs at a symbol transition. The worst transient response measured was less than 19.6% of the UI and the transmitted symbols were correctly interpreted at the receiver end. Typically, the symbol transitions were much shorter than the worst-case percentage measured, so the change in the PLLs output phase did not lead to lose the "lock" condition. The BSU steering vector has then been swept across all the 2^8 implementable angles to prove its spatial selectivity. This was done by assigning vectors of phase shifts that verify the following condition:

$$B = [0, \Delta\varphi, 2 \cdot \Delta\varphi, 3 \cdot \Delta\varphi] \tag{17}$$

TABLE I
FREQUENCY AND PHASE TIME TO LOCK

Loop BW	TTL at 10-Hz	TTL at 1°	% of UI
10-kHz	377μs	333μs	266.4%
50-kHz	78.2μs	55μs	44%
100-kHz	36.7μs	24.5μs	19.6%

with:

$$\Delta\varphi = w \cdot \frac{2\pi}{2^8} \tag{18}$$

and $w \in [0, 1, \ldots 2^8 - 1]$. The measurement setup includes a 9-kHz to 26.5-GHz Vector Signal Analyzer (VSA, Agilent N9010A) and is shown in Fig. 17. Fig. 18 shows the normalized peak power at the VSA for each phase shift at adjacent outputs. The curve is expected to exhibit a zero when a 180° phase shift is assigned to adjacent outputs of the FSU. In this working condition, the received signal attenuation exceeded 50-dB. The received signal attenuation, with respect to the broadside working condition, is better than 8-dB at the

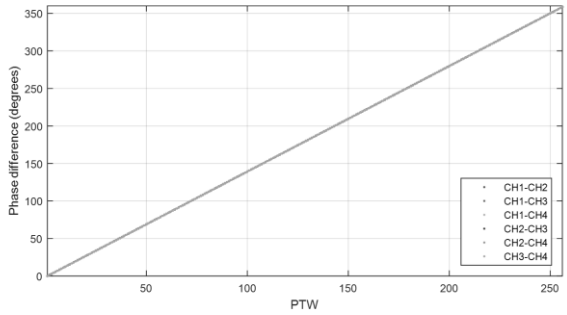

Fig. 10. PTW vs. phase difference trans-characteristic (PCU outputs)

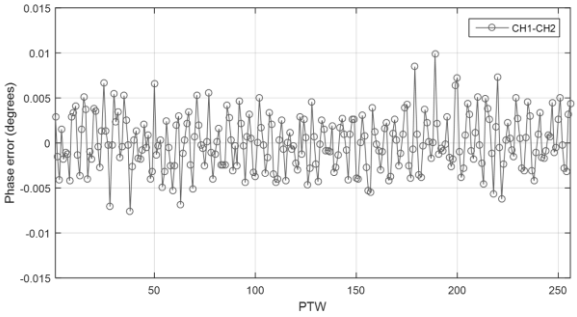

Fig. 11. PTW vs. phase error (PCU outputs, CH1-CH2)

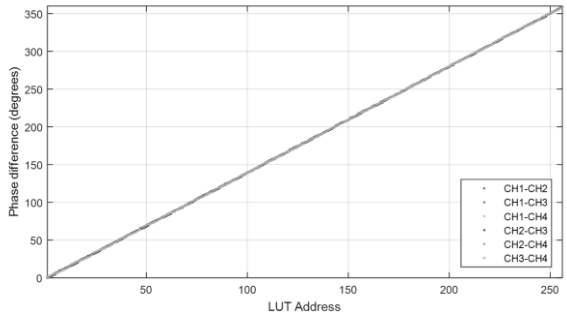

Fig. 12. LUT address vs. phase difference trans-characteristic (FSU outputs)

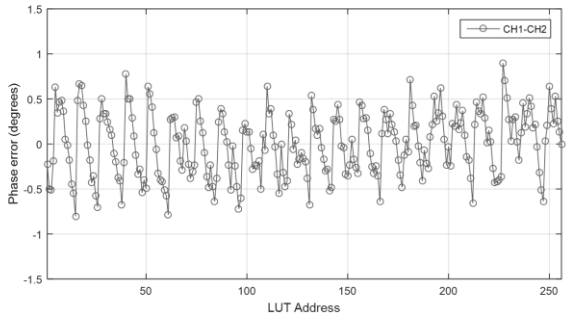

Fig. 13. LUT address vs. phase error (FSU outputs, CH1-CH2)

Fig. 14. Measurement setup employed during the qualification of the BSU architecture acting as a transmitter

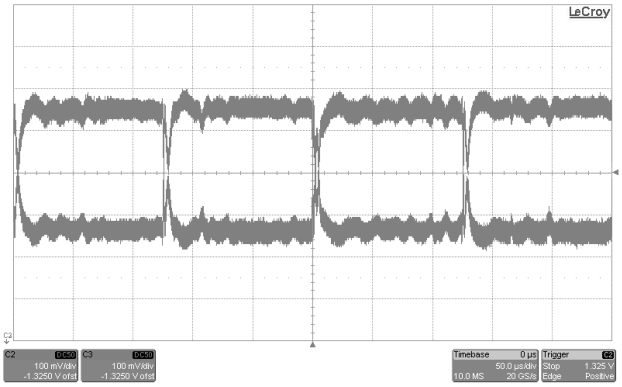

Fig. 15. Received IQ signals measured in time domain

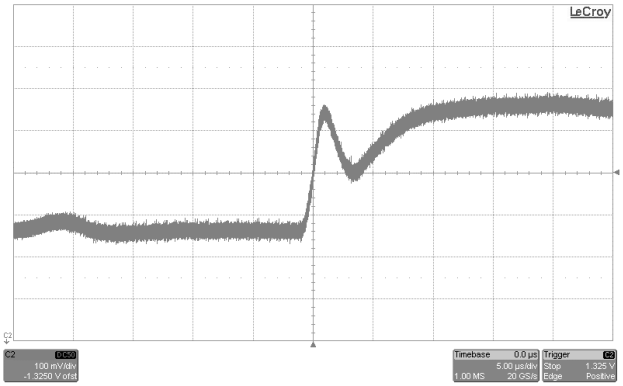

Fig. 16 – Transient response measured in time domain

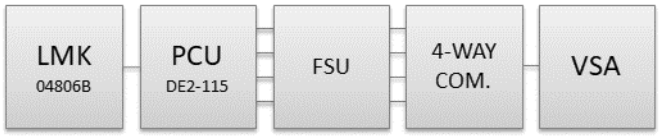

Fig. 17. Measurement setup employed during the qualification of the steering performance of the BSU

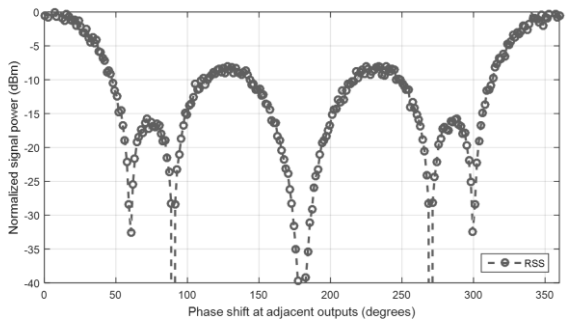

Fig. 18. Phase shift at adjacent outputs vs. normalized peak power at the spectrum analyzer

first relative maxima, and it is better than 16-dB at second relative maxima.

V. Conclusions and Future Work

This work presented the design and implementation of a modulator-less beam steering transmitter based on a revised DDS-PLL phase shifter architecture. The proposed topology targets low data rate communications for Internet-of-Things systems, and has been demonstrated using an FPGA evaluation board and a custom PCB with four PLLs centered at 2.453-GHz. Measured system performance for an experimental 32-kbps data rate achieved through a 16-PSK modulation scheme have been discussed. At the PCU outputs, the mean phase error across PTWs, measured among pairs of outputs, is close to 0, and the mean standard deviation in the acquired phase difference samples is less than 0.0025°. The PCU phase error is contained within the range [-0.01°; +0.01°]. At the FSU outputs, the mean phase error across LUT addresses is close to 0, and the mean standard deviation in the acquired phase difference samples is less than 0.01°. The FSU phase error, measured among pairs of outputs, is contained within the range [-0.9°; +0.9°]. The BSU has been configured to transmit data according to a 16-PSK modulation scheme with a symbol rate fixed at 8-kbaud. Measurements have been conducted through a 4-way passive combiner and four semi-rigid coaxial cables, simulating that the position of the receiver, with respect to the transmitter, was broadside and far away. When a 180° phase shift is assigned to adjacent outputs of the FSU, the received signal attenuation exceeded 50-dB.

The proposed architecture is carrier frequency independent, so it can be used in multi-band devices and has the potential for being integrated as an RF System-on-Chip. The integration of the microprocessor and the low-complexity phase shifter gives a self-contained architecture providing a desirable solution for a wide class of applications that requires firmware execution and enhanced connectivity through a phased array. Future research effort will focus on: i) measuring system performance in free space; ii) implementing hardware and firmware IPs for built-in calibration procedures; iii) implementing a beam steering receiver based on DDS-PLLs; iv) integrating the proposed design into an ASIC developed in a BiCMOS technology. This perspective is supported by the cost effectiveness of many mixed-signal processes on the market, the promise of the measured results and the vigorous research efforts that are currently taking place in the field of phased arrays.

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