

Article

# Innovative Strategy for Mixer Design Optimization Based on $g_m/I_D$ Methodology

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**Abstract:** This work introduces a process to optimize the design of a down-conversion mixer using an innovative strategy based on the  $g_m/I_D$  methodology. The proposed process relies on a set of technology-oriented lookup tables to optimize the trade-off between gain, power dissipation, noise, and distortion. The design is implemented using a 0.13  $\mu\text{m}$  CMOS technology, and to the best of our knowledge, it possesses the best (post-layout simulation) figure of merit (FOM) among the works presented in literature. The FOM is defined as the product of gain and third-order intercept divided the product between average noise figure and power dissipation. Finally, the core of the mixer takes only 31  $\mu\text{m}$  by 28  $\mu\text{m}$  and it draws a current of 1 mA from the 1.5 V DC supply.

**Keywords:** mixer; Gilbert's cell;  $g_m$  over  $I_D$ ; optimized design strategy

## 1. Introduction

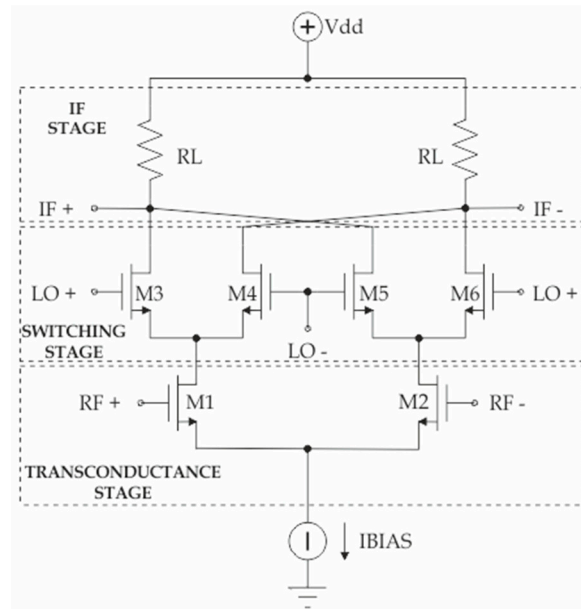
The down-conversion mixer is a critical block in the design of systems based on the software-defined radio (SDR) architecture. Due to technology limits of the analog to digital converters (ADC), the RF signals at high frequency cannot be directly sampled. The mixer is, thus, a key component to perform the down-conversion of the antenna signal at intermediate frequencies compatible with commercial ADCs.

In literature, several approaches were introduced to maximize the mixer performance. For example, Wei et al. [1] use a folded topology to diminish the transistors stacked on top of each other. With a folded structure, the circuit can employ a lower supply voltage, however, it requires an extra current source that has the negative effect of reducing both gain and bandwidth. MacEachern et al. [2] propose a topology that relies on the charge injection method. Their approach allows to improve both gain and linearity, however, it has the drawback that requires a significantly higher bias current and hence it worsens power consumption. Seo et al. [3] exploit a switched biasing technique for the tail current source that results in a substantial reduction of the noise figure. Unfortunately, this benefit comes at the expenses of a significantly larger supply voltage and power dissipation than the traditional Gilbert's cell. Hence, these approaches utilize very complicated hardware solutions to maximize the performance of the mixer. This work presents the design approach followed to optimize the circuit of a conventional double-balanced Gilbert mixer cell (Figure 1).

This architecture is very common in homodyne (also known as direct-conversion) receivers because it exhibits a favorable port-to-port isolation factor and negligible even harmonic distortion [4]. Unfortunately, the presence of three MOS transistor pairs on top of each other calls for a relatively large supply voltage to keep them operating in saturation.

As illustrated in Figure 1, the RF voltage is fed into the stage consisting of the transistors M1 and M2. The transistors M3–M6, perform RF voltage-to-current conversion and switch the polarity of the RF inputs at the LO frequency rate. In theory, given the symmetry of the circuit, any common-mode RF and LO frequency component at the output should be zero.

This paper aims to extend the Jespers and Murmann  $g_m/I_D$ -based approach [5,6] to optimize the design of a double-balanced mixer based on the Gilbert cell. A new set of lookup tables were computed to take into account the performance of the mixer in the three MOSFET inversion regions. With these new set of lookup tables, the designer is able to maximize the overall performance of the basic cell without introducing complex circuit solutions. The reported mixer was used in the design of the positioning system reported in [6–9].



**Figure 1.** Double-balanced Gilbert cell mixer.

The rest of the paper is arranged as follow. Section 2 introduces the methodology we applied to overcome the inaccuracies associated with the traditional square law model of the MOSFET devices. Section 3 describes the design methodology introduced to maximize the performance of the Gilbert cell. Section 4 presents the results achieved and compares them with other works presented in the literature. Finally, Section 5 provides a set of conclusions and closes the paper.

## 2. Theoretical Background

The traditional approach to design analog circuits is based on modeling the drain current  $I_D$  of MOSFET devices in saturation region with the following square law Equation (1)

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \equiv I_{D,sat} \quad (1)$$

where  $\mu$  is the mobility of the carriers in the inversion layer channel,  $C_{ox}$  is the gate oxide capacitance,  $W/L$  is the ratio between the width and the channel length of the MOSFET,  $V_{GS}$  is the gate-source voltage and, finally,  $V_{TH}$  is the MOSFET threshold voltage. Given the continuous shrinking of the channel length of the MOSFETs employed in today's integrated circuits, Equation (1) becomes grossly inaccurate. With the current nanometer channel lengths, several second-order effects are no longer negligible and must be considered [10].

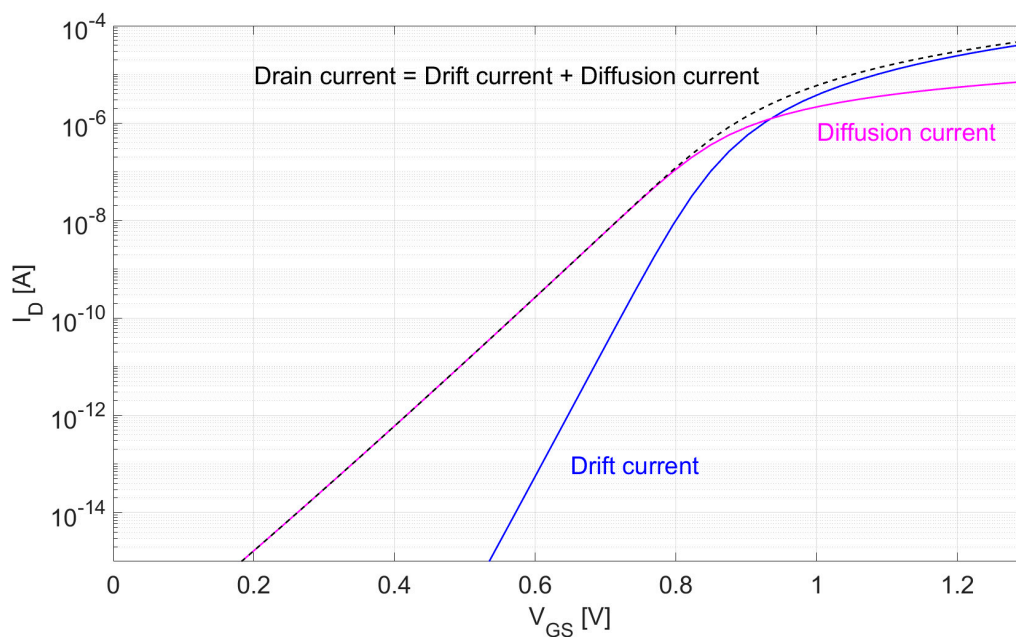
The typical models used for describing the behavior of nanoscale MOSFETs includes several hundred parameters, thus, it is too complicated to come up with a simple analytical abstraction that would be suitable for analog circuit design. When  $V_{GS} \leq V_{TH}$  (sub-threshold operation) the drain current does not go to zero as predicted by the square-law equation. The current in and near sub-threshold takes an exponential form. This is because the MOSFET acts as if it was a lateral BJT. In sub-threshold (also known as weak inversion) the current is mainly dominated by its diffusion

component (rather than its drift component) and as a result, it has an expression that resembles closely the current equation of a BJT [11] (Figure 2):

$$I_D = I_0 e^{\frac{q(V_{GS}-V_{TH})}{m k T}} \left(1 - e^{-\frac{q V_{DS}}{k T}}\right) \quad (2)$$

$$I_0 \triangleq \mu C_{ox} \frac{W}{L} (m-1) \left(\frac{k T}{q}\right)^2$$

where  $k$  is the Boltzman constant,  $q$  is the electronic charge measured in Coulomb,  $T$  is the temperature, and  $m$  is a coefficient accounting for how the body effect at the drain end of the channel affects the control of the charge in the channel. The coefficient  $m$  (also known as the subthreshold factor) is process dependent and it typically varies between 1.3 and 1.7. [12].



**Figure 2.** Drain current with the drift and diffusion contribution. The drift current dominates in strong inversion, diffusion current in weak inversion.

In weak inversion, the current available to drive any capacitive load is quite small so the MOSFET consumes very little power, but it can be quite slow. In addition, the definition of  $V_{TH}$  is problematic. On the contrary, if the transistor operates in strong inversion it consumes more power but exhibits the best performance in terms of speed. The operation between strong and weak inversion is called moderate inversion and due to the growing demand for low supply voltage applications, it has become more and more attractive. In moderate inversion, the MOSFET achieves the best tradeoff between speed and DC-power consumption. Unfortunately, no simple analytical equation exists for the drain current of a MOSFET in moderate inversion. The EKV model [13], the BSIM model [14], the ACM model [15], and the PSP model [16] on which most simulation tools rely are too complicated for hand analysis.

Using a table-based procedure like the  $g_m/I_D$  methodology is more effective. It allows the ability to achieve accurate results with a very limited number of design iterations. This method consists of generating a set of lookup tables starting from the DC-analysis of the transistor. Each table computes a different width-independent figure of merit (FOM), closely linked to the design specifications (e.g., transit frequency, intrinsic gain, transconductance efficiency, current density, and relative capacitances). The design process consists in choosing the inversion level of the MOSFETs so that the figures of merit extracted, and the  $W/L$  ratios associated with each transistor are able to meet the required design specifications [6,10]. The  $g_m/I_D$  ratio, also known as the transconductance efficiency or gain-power

efficiency, is a proxy for the inversion level the transistor. Using, for simplicity, the square-law model, for a MOSFET operating in saturation region, the transconductance  $g_m$  is defined as:

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) = \frac{2I_D}{(V_{GS} - V_{TH})}. \quad (3)$$

Hence the  $g_m$  over  $I_D$  ratio depends only on the overdrive voltage  $V_{OV} = V_{GS} - V_{TH}$ .

$$\frac{g_m}{I_D} = \frac{2}{V_{OV}}. \quad (4)$$

In other words, setting the  $g_m/I_D$  ratio is equivalent to setting the operating region of the MOSFET. For values of  $g_m/I_D$  between 5 S/A and 8 S/A the MOSFET is in strong inversion. For  $g_m/I_D$  in the range between 20 S/A and 25 S/A the MOSFET is in weak inversion. The choice of the inversion level is essentially determined by the trade-off between speed (transit frequency,  $f_T = g_m/C_{GG}$ ), intrinsic gain ( $g_m/g_{DS}$ ), and gain-power efficiency ( $g_m/I_D$ ) and it depends on the target application.

The key feature that makes the table-based design approach suggested so effective is that all FOMs are width independent. If for sake of simplicity we resort again to the square-law, we note that:

$$\begin{aligned} f_T &= \frac{g_m}{C_{GG}} \approx \frac{3}{2} \frac{\mu V_{OV}}{L^2} \\ \frac{g_m}{g_{DS}} &\approx \frac{2}{\lambda V_{OV}} \\ \frac{I_D}{W} &= \frac{\mu C_{ox}}{2L} V_{OV}^2. \end{aligned} \quad (5)$$

In strong inversion (low  $g_m/I_D$  ratio) the transistor exhibits higher speed than in weak inversion, but the intrinsic gain is lower, and the power dissipation is higher (to obtain a given value of  $g_m$  the drain current required is higher than in weak inversion). In weak inversion, that is, for a large  $g_m/I_D$  ratio, the intrinsic gain increases, while the  $f_T$  decreases. This is due to the corresponding increase of the width of the transistor its total intrinsic capacitances. Finally, the drain current decreases for increasing values of  $g_m/I_D$ , which means that the DC power consumption drops. The region in the middle between strong and weak inversion is called moderate inversion and usually gives a good compromise in terms of speed, gain, and power consumption.

Figure 3 shows the graphs for transit frequency, intrinsic gain and current density versus  $g_m/I_D$  for the NMOS transistor from the IHP (Innovate for High-Performance Microelectronics) process [17–22] used for implementing the mixer. The curves are sketched for the minimum channel lengths ( $L =$  and for a drain-source voltage,  $V_{DS}$ , equal to half the DC-power supply,  $V_{DD}$ ). The  $g_m/I_D$  design method is both scalable and easily adaptable to the design of different target systems. These charts represent the starting point for implementing the design. The design flow proposed provides the designer with the flexibility to start by choosing any of the tabulated figures of merit as his primary objective and then proceed by systematically extracting all other features depending on the specific performances to be optimized.

### 3. Design Optimization

For Gilbert's cell (Figure 1), given the desired value of the load resistance,  $R_L$ , the mixer gain ( $A_v$ ) is determined by the transconductance value ( $g_m$ ) of the transistors M1 and M2:

$$A_v \cong \left(\frac{2}{\pi}\right) g_m R_L. \quad (6)$$

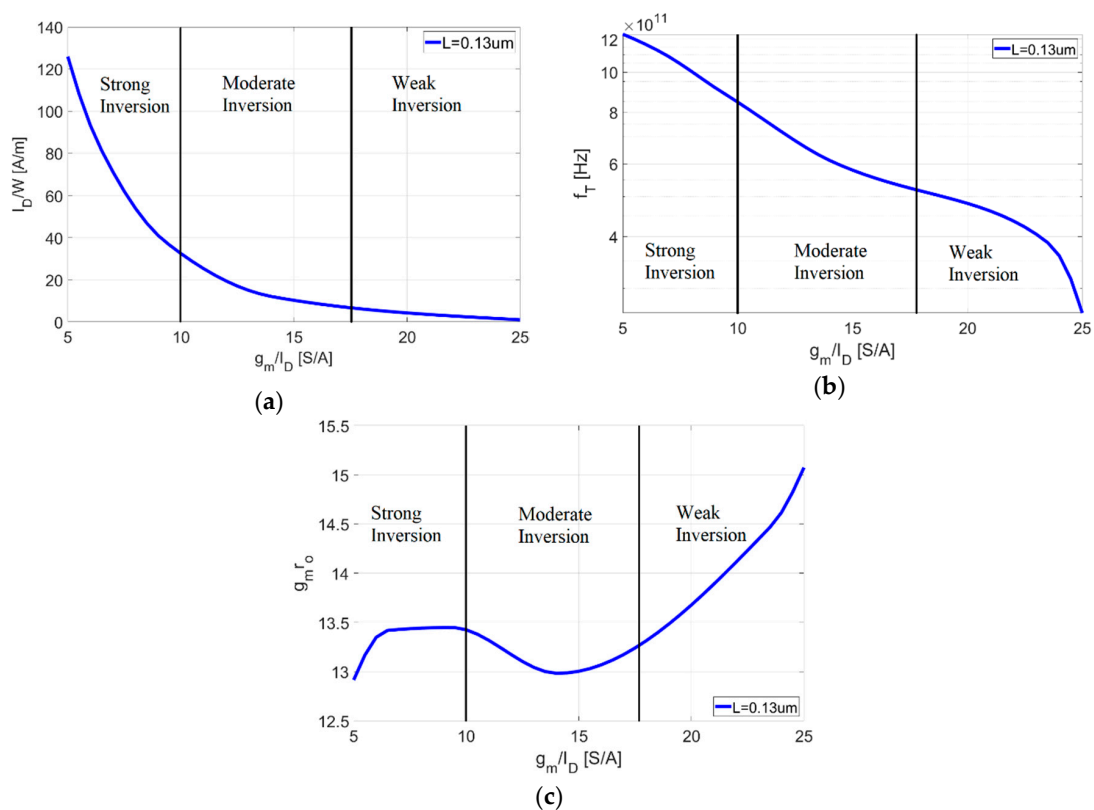
The traditional design approach starts from Equation (6) by first computing the  $g_m$  necessary to obtain the desired gain and then choosing the width  $W$  and channel length  $L$  of the MOSFETs using the square law Equation (7):

$$g_m = \sqrt{\frac{2\mu C_{ox} W I_D}{L}}, \quad (7)$$

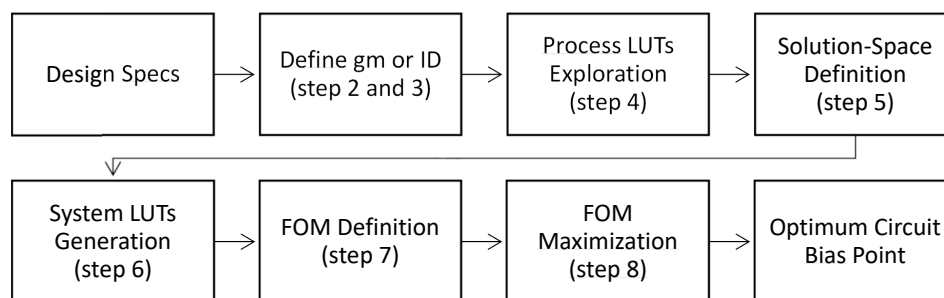
where  $C_{ox}$  is the oxide capacitance of the MOSFET and the  $\mu$  the mobility of the carriers. The bias current supplied by the tail current source ( $I_{BIAS}$ ) is split equally among the transistors in the transconductance stage (TS). Similarly, the current flowing through M1 and M2 is evenly split between the transistors in the switching stage (SS):

$$I_{BIAS} = 2 \times I_{D(TS)}, \quad I_{D(SS)} = 2 \times I_{D(TS)}. \quad (8)$$

Unfortunately, in today’s nanometer integrated circuits, the behavior of the MOS transistors does not follow the square-law model. For this reason, in the approach we advocate, the W/L ratio of the transistors is chosen using  $g_m/I_D$ -based lookup tables. The algorithm used to optimize the sizing of the transistors considers the devices in the switching stage and the transconductance stage separately. The algorithm allows exploring a larger solution space to find the optimal bias point that meets design specifications, by separately sweeping the  $g_m/I_D$  of the two stages. The proposed algorithm is composed of the eight steps represented in Figure 4.



**Figure 3.** IHP 0.13  $\mu\text{m}$  process lookup tables (a) current density  $I_D/W$  vs.  $g_m/I_D$ ; (b) transit frequency  $f_T$  vs.  $g_m/I_D$ ; and (c) intrinsic gain  $g_m/g_{DS}$  vs.  $g_m/I_D$ .



**Figure 4.** The design framework.

Step 1. To be able to run the framework, we must, first of all, generate Jespers and Murmann's lookup tables (LUTs) for the MOS transistors of the 0.13  $\mu\text{m}$  process used to design the circuit (these LUTs are denoted in Figure 4 with the name "process LUTs"). A graphical view of these lookup tables is provided in Figure 3.

Step 2. Given the desired design specs. (i.e., gain and load resistance), Equation (6) can be used to derive the value of  $g_m$ .

Step 3. Once the value of  $g_m$  is found, the algorithm sweeps  $g_m/I_D$  in the whole feasible range (i.e., from 5 S/A to 25 S/A) and computes the associated currents  $I_{D(SS)}$  and  $I_{D(TS)}$ .

Step 4. Given Jesper and Murmann's lookup table of the current density ( $I_D/W$  vs.  $g_m/I_D$ ) the algorithm extracts  $W_{(SS)}$  and  $W_{(TS)}$  for all values of  $g_m/I_D$  explored. To maximize the speed of the mixer the length  $L$  of all transistors is set to the minimum value (130 nm) allowed by the technology used to implement the circuit [20,21].

Step 5. The algorithm performs a systematic analysis of the mixer's performances. For each bias point it computes the DC-power consumption, it checks that all transistors operate in saturation and it prunes any unfeasible solution.

Step 6. For each point that represents a feasible solution, the algorithm computes the gain of the mixer and then discards any point that exhibits a gain that does not meet the specifications. This procedure is repeated for the noise figure and the third-order intercept of the mixer. The system performance metrics computed in this step are captured and stored in the form of lookup tables (these LUTs are denoted in Figure 4 with the name "system LUTs").

Step 7. Given the solution space computed in the last step, to compute the best bias point of the circuit, an overall figure of merit (FOM) is introduced.

Step 8. The algorithm returns the best circuit bias point to be used to design the down-conversion mixer, by looking up the solution (i.e., the value of  $g_m/I_D$ ) corresponding the maximum value of the FOM.

Several performance metrics can be used to define the FOM of the circuit. The designer can choose the one he prefers without performing any software modification. In fact, the algorithm computes the FOM value by simply exploring the lookup tables related to the system performance (conversion gain, noise figure, and so on). In our design, to obtain the best balance between the various parameters specified, we defined the following figure of merit (FOM):

$$FOM = \frac{G_{[dB]} \cdot IIP3_{[mW]}}{NF_{[dB]} P_{DC[mW]}} \quad (9)$$

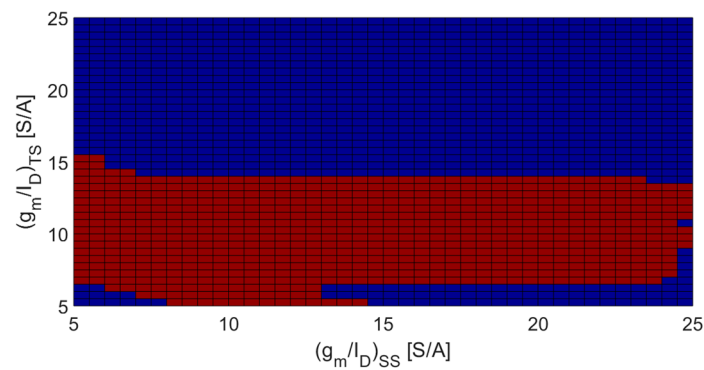
where  $G$  is the gain,  $IIP3$  is the input third-order intercept,  $NF$  is the average noise figure and  $P_{DC}$  is the power dissipation. The definition of the FOM is up to the designer and it is based on the target application of the mixer. Once the lookup tables for the performance metrics of the system (gain, noise figure, etc.) are generated the designer selects the figure of merit as a function of the relative importance of the various performance metrics.

#### 4. Results

The supply current drained by the mixer should be of less than 2 mA with a 1.5 V voltage. The desired gain had to be greater than 10 dB with a load of 500 Ohms, and the  $IIP3$  had to be better than  $-5$  dB. The circuit performances were validated for a LO sine wave with a frequency of 5.7 GHz and a maximum power of 0 dBm.

Figure 5 summarizes the feasible solutions (red color) obtained by the algorithm. From this figure, it is possible to observe that the transistors in the transconductance stage (TS) should be biased with a  $g_m/I_D$  between 5 S/A and 13 S/A while the transistors in the switching stage (SS) can be biased at any  $g_m/I_D$  level.





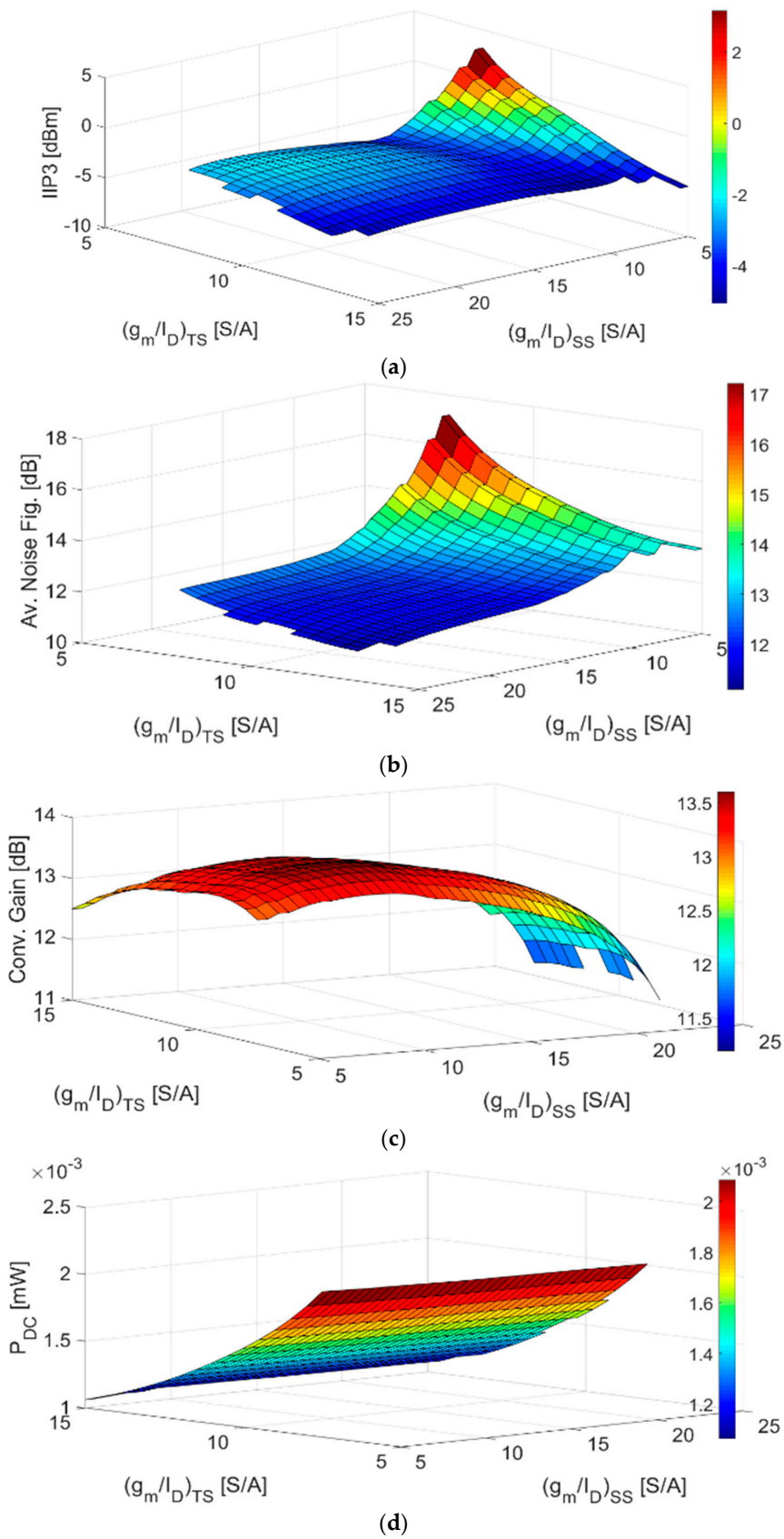
**Figure 5.** Solution space versus  $g_m/I_{D(TS)}$  and  $g_m/I_{D(SS)}$  ratios.

Figure 6a provides the curve characterizing the input third-order intercept of the mixer. Given that the MOSFETs in the switching state must be biased with a  $g_m/I_D$  in the range between 5 S/A and 10 S/A, we note that as the bias point of the transistors in the transconductance stage passes from strong to weak inversion, the IIP3 decays linearly. Moreover, we note that biasing the transistors of the switching stage in weak inversion, the IIP3 behavior can be approximated by a parabolic function with a local maximum for  $g_m/I_{D(SS)}$  of 20 S/A. The IIP3 curve has been computed using two tones, one at 5.8 GHz and the other one at 5.85 GHz. Figure 6b sketches the curve characterizing the average noise figure of the mixer. The average is taken over the ultra-wide bandwidth (UWB) frequencies range (3.1 ÷ 10.6 GHz). Imposing that the SS transistors are biased in strong inversion, we note that as the transistors in the TS pass from strong to moderate inversion the noise figure decreases exponentially and approaches a value that is less than 12 dB. The curve illustrating the mixer gain is reported in Figure 6c. The gain in the mixer can be approximated by a parabolic function in both  $g_m/I_D$  directions. Biasing the transistors of both stages in moderate inversion, the mixer exhibits an absolute maximum gain of 13.5 dB. Figure 6d shows the mixer's power consumption. As expected from the circuit analysis of the mixer [4], the power dissipation of the transconductance stage is dominant over the power dissipation of the switching stage. From Figure 6, we note that the power is approximately constant along the SS axis, while along the TS axis it exhibits an exponential roll-off as  $g_m/I_D$  increases.

Finally, the FOM as a function of  $g_m/I_{D(TS)}$  and  $g_m/I_{D(SS)}$  ratios is presented in Figure 7. Note that the FOM presents a local maximum when biasing the TS in moderate inversion and the SS between moderate and weak inversion.

The algorithm returns as an optimal solution the FOM corresponding to  $g_m/I_{D(SS)} = 18$  S/A and  $g_m/I_{D(TS)} = 10.5$  S/A. The jittery nature of the FOM curve is a result of the irregular behavior of both the IIP3 and the noise figure. To avoid this problem, the FOM can be re-defined introducing weighting coefficients in the formula. The introduction of weighting coefficients also allows the designer to drive the optimization process to favor one or more performances based on the target application. For example, in the case of the mobile market, power consumption is more critical than IIP3 and so it is possible to introduce a coefficient in the FOM expression that induces the algorithm to maximize power performance more than other performances.

Figure 8 reports the post layout performances of the double-balanced mixer designed with the proposed method. With a LO power of 0 dBm, the post-layout mixer gain is about 11 dB. This corresponds to a loss of about 2 dB compared with the theoretical gain expected. The main reason lies in the parasitics introduced by the bias current source physical implementation. Similarly, the post-layout IIP3 is  $-3.1$  dBm lower than the ideal value of 2.8 dBm. In terms of power dissipation, with a voltage supply of 1.5V, the mixer-core consumes only 2.1 mW. Although the performance in post-layout simulations are worse than the theoretical values expected, they still exceed the design specification and therefore validate the proposed design approach.



**Figure 6.** (a) Mixer IIP3 vs.  $g_m/I_{D(TS)}$  and  $g_m/I_{D(SS)}$  ratios. (b) Average noise figure vs.  $g_m/I_{D(TS)}$  and  $g_m/I_{D(SS)}$  ratios. (c) Mixer conversion gain vs.  $g_m/I_{D(TS)}$  and  $g_m/I_{D(SS)}$  ratios. (d) Mixer power dissipation vs.  $g_m/I_{D(TS)}$  and  $g_m/I_{D(SS)}$  ratios.



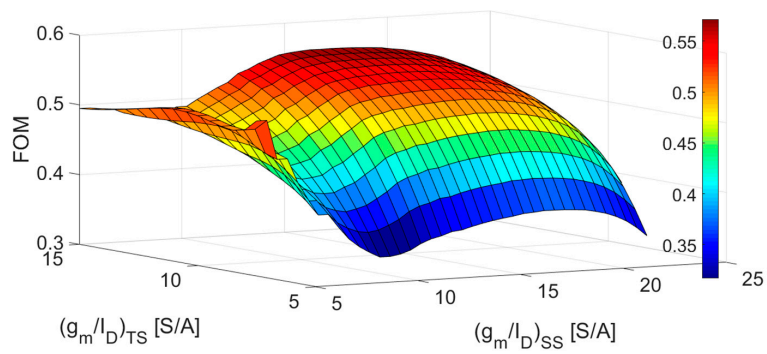
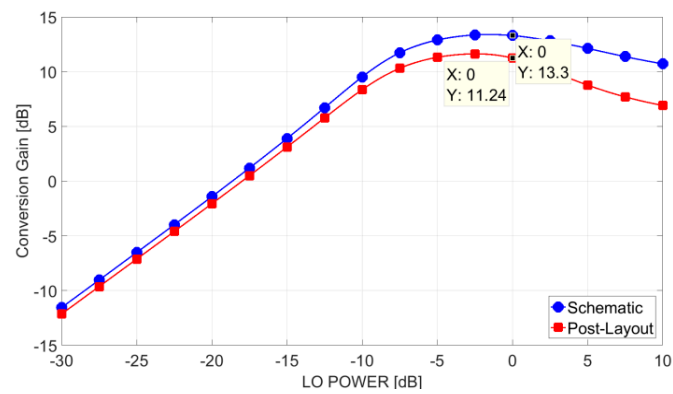
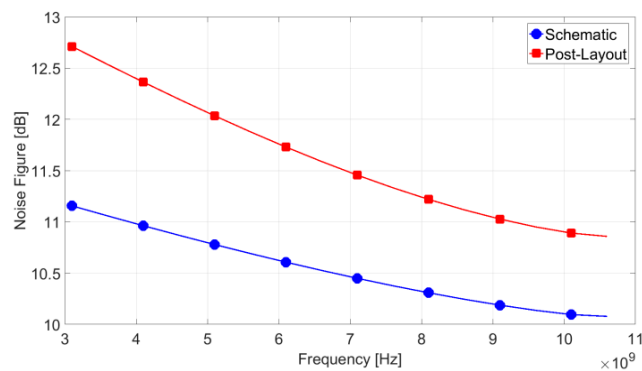


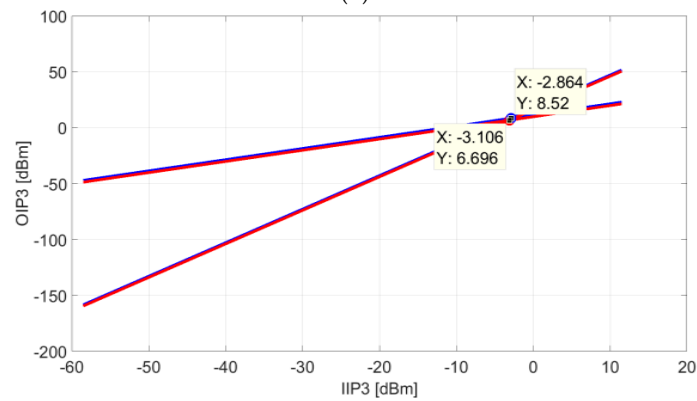
Figure 7. Figure of merit (FOM) versus  $g_m/I_{D(TS)}$  and  $g_m/I_{D(SS)}$  ratios.



(a)



(b)



(c)

Figure 8. Post-Layout Simulation (a) Mixer Conversion Gain vs. LO power (b) Mixer NF vs frequency (c) Mixer OIP3.

To assess the quality of our design we compared its performances with the performances of other CMOS Gilbert mixers found in literature. Using the proposed approach (see Table 1) our mixer achieves the best (post-layout simulation) FOM. Unfortunately, since not all references state unequivocally whether their figures come from measurements or simulation, a fair comparison is problematic. This result is obtained using a traditional double-balanced circuit architecture and did not require the introduction of any of the dedicated topological improvements that can be found in literature. Nevertheless, the proposed approach is completely general and if desired it can be easily extended to other circuit architectures that have the potential to improve a mixer performance. The final layout of the mixer's core is sketched in Figure 9. The mixer-core measures less than 21  $\mu\text{m}$  by 31  $\mu\text{m}$  (bonding pads and baluns excluded).

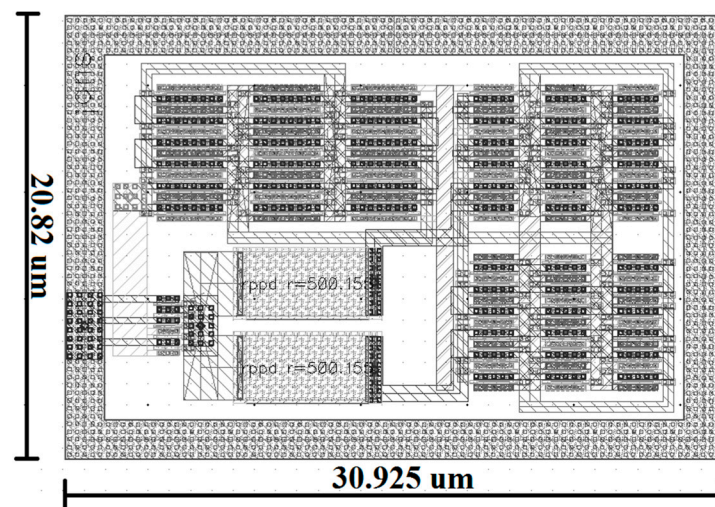


Figure 9. The mixer layout.

Table 1. Comparison of the Gilbert cell mixers performance.

Reference	Technology	Gain [dB]	IIP3 [dBm]	NF avg [dB]	$P_{DC}$ [mW]	FOM
[3]	0.13 $\mu\text{m}$	8	-3	11.2	5.57	0.12
[23]	0.18 $\mu\text{m}$	10	4	10	10	0.16
[24]	0.13 $\mu\text{m}$	8.95	-2.2	11.4	3.7	0.16
[25]	0.13 $\mu\text{m}$	21	-1.8	15.7	18.3	0.06
[26]	0.18 $\mu\text{m}$	13.5	-3.25	21.22	7.2	0.06
[27]	0.18 $\mu\text{m}$	20.4	-4.6	12.2	5.44	0.11
[28]	0.13 $\mu\text{m}$	13.4	-	-	52	-
This Work	0.13 $\mu\text{m}$	11.24	-3.1	11.6	2.1	0.32

## 5. Conclusions

A new optimization approach is introduced and applied to the design of a down-conversion mixer based on the Gilbert cell. The algorithm implemented allows reducing the iteration time required to optimize the design of the circuit by providing a series of lookup tables that can be explored to obtain the best circuit bias point meeting the specification. The main advantage of the proposed methodology is that if the design specifications vary, only the FOM needs to be changed. As a result, redesigning the mixer takes a significantly shorter amount of time. In fact, the lookup tables are generated only the first time and can be subsequently re-used for any different set of design specifications.

The results demonstrate that the mixer designed with the proposed framework is able to achieve the best tradeoff in overall performance without the need for using any complex ad-hoc circuit

topologies present in literature. However, if desired the method can be extended also to more complex circuits to possibly allow to further improve the overall performance of mixers.

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