

Article

Analytical and Simulation Fair Comparison of Three Level Si IGBT Based NPC Topologies and Two Level SiC MOSFET Based Topology for High Speed Drives

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Abstract: Wide bandgap (WBG) power devices such as silicon carbide (SiC) can viably supply high speed electrical drives, due to their capability to increase efficiency and reduce the size of the power converters. On the other hand, high frequency operation of the SiC devices emphasizes the effect of parasitics, which generates reflected wave transient overvoltage on motor terminals, reducing the life time and the reliability of electric drives. In this paper, a SiC metal-oxide-semiconductor field-effect transistor (MOSFET) based two level (2L) inverter is systematically studied and compared to the performance of Si insulated-gate bipolar transistor (IGBT) based three level (3L) neutral point clamped (NPC) inverter topologies, for high speed AC motor loads, in terms of efficiency, overvoltages, heat sink design, and cost. A fair comparison was introduced for the first time, having the same output voltage capabilities, output current total harmonic distortion (THD), and overvoltages for the three systems. The analysis indicated the convenience of using the SiC MOSFET based 2L inverter for lower output power. In the case of the maximum output power, the heat sink volume was found to be 20% higher for the 2L SiC based inverter when compared to 3L NPC topologies. Simulations were carried out by realistic dynamic models of power switch modules obtained from the manufacturer's experimental tests and verified both in the LTspice and PLECS simulation packages.

Keywords: SiC devices; Si devices; three level NPC inverter; three level T-NPC inverter; two level SiC MOSFET inverter; overvoltages; heat sink volume

1. Introduction

Wide bandgap semiconductor devices, such as silicon carbide (SiC), offer many benefits due to their superior material properties, among which are increased junction operating temperature, low specific on resistance, high switching speed capability, low switching losses, etc. Consequently, motor drives supplied by a SiC based voltage source inverter (VSI) can provide lower losses, higher efficiency, and a smaller size when compared with their silicon (Si) counterparts [1,2]. All these features contribute to these devices generating interest in applications for electric traction systems, where a long life time is important, and by reducing the losses in such applications, the life time can be extended [3,4].

Even though the modern switching devices offer many benefits, they still experience many problems mainly connected to the fast switching such as high dv/dt -rates, also in combination with impedance mismatch (machine against cabling and surge), high di/dt , crosstalk [5], etc. Moreover, the fast switching leads to transient overvoltage which increases the strain for the machine's insulation and accelerated aging [4,6]. This, together with the fact that often, the power cable between the inverter and the motor is long, leads to significant voltage overshoot due to reflected wave phenomenon. All of these problems resulting from the high dv/dt spikes could degrade the reliability and efficiency of motor drive systems [7–9]. In some cases, motor transient peak voltages can be even up to 3–4-times the DC bus voltage [10]. Moreover, besides the effects of the overvoltages on a whole winding, also the stress on the inter-turn insulation of the motor windings must be considered, especially as the rise time becomes shorter. This can result in relevant voltage drops across one turn, going beyond the inter-turn insulation design limit considered under sinusoidal operation [6,7].

Currently, insulated-gate bipolar transistor (IGBT) based two level (2L) VSI, and three level (3L) neutral point clamped (NPC) and T-type neutral point clamped (T-NPC) inverters are commercially available and widely used by industry. However, in some cases, the application of 2L inverters is limited due to several drawbacks. They are usually connected with increased losses (in the case of higher fundamental frequencies (1 kHz); at the same time, they typically commute large motor currents with a high switching frequency) and the generation of the high frequency ripple currents at the input DC-bus due to device switching (leading to the usage of oversized capacitors) [11]. Alternatively, 3L NPC and T-NPC inverters feature the following benefits: (1) lower switching losses; voltage across the device is half of the DC-link voltage; and (2) lower output current distortion. Furthermore, the T-NPC inverters incorporate additional advantages such as lower conduction losses when compared with the NPC inverter, being the better choice for low voltage applications [12,13].

Most of the state-of-the-art comparisons between the SiC metal-oxide-semiconductor field-effect transistor (MOSFET) and Si IGBT based inverters are done on the device level or in 2L VSIs [14,15] or hybrid topologies such as the H8 inverter [16]. Recently, also some multilevel Si IGBT based, SiC MOSFET based, or gallium nitride (GaN) based topologies have been compared, such as the single phase T-type inverter [17,18], advanced inverter topologies [19], or the single phase two stage decoupled active neutral point clamped (NPC) converter [20]. Generally, inverters with GaN and SiC MOSFET devices have shown benefits when compared to their Si counterparts such as lower losses, high efficiency at high frequency applications, reduced volume of the heat sink and output filter, etc.

A similar comparison was introduced in [21], where the 2L SiC inverter was compared with the 3L NPC inverter in terms of overvoltages and power losses, having the same output current total harmonic distortion (THD) and the same output voltage capabilities. This paper, following a similar principle, gives the comparative analysis of the 2L and 3L topologies mainly used by industry, introducing a fair comparison.

In this paper, a comparison between the 2L SiC MOSFET based VSI and 3L IGBT based NPC and T-NPC VSI is made, being widely used in industrial applications and offering additional advantages [22]. The three systems consider low voltage high speed electric drive applications with long power cables. The main contribution is the conducted fair comparison that has not been published yet in the literature, and that is based on the fact that the output voltages of the inverters are set in such a way to produce along the cable and at the motor terminals the same overvoltage for the three systems. The overvoltages are known to be the main causes of the partial discharge occurring in the stator winding, greatly influencing its life time and the reliability of the electric drive. In particular, in order to have a fair comparison, the three inverters have the same output voltage capabilities and the same output current THD. Moreover, the overvoltage dv/dt is set the same for the three inverters, by changing the gate resistance. The main idea is to analyze the three inverters in the same working condition. It is crucial in order to understand which topology is better and in which conditions. Even though the 2L SiC based inverters might seem a better solution for an electric drive application, having generally less losses and high switching operation, they still experience problems connected to the

high switching speed, i.e., high overvoltages. On the other hand, 3L NPC inverters are widely used by industry, are considered reliable enough, and can be a good competitor of the 2L SiC MOSFET based solution. The high frequency equivalent circuit of the inverter-cable-motor system is introduced for the simulation modeling and transient analysis. The comparison includes the power loss difference of the three systems, as well as the heat sink design and total cost. The analysis is done on the power modules' real dynamic models obtained from the manufacturer's experimental test in the LTspice simulation tool (for the transient analysis of the overvoltages on the high frequency equivalent circuit, but also switching loss analysis with double pulse tests) and the PLECS simulation package for the loss and heat sink comparison, the access to the steady state being facilitated.

2. Inverter Topologies

Generally speaking, when considering the comparison of 2L and 3L inverter topologies, the 2L inverter features advantages such as the simple configuration, reliability, easy control, and lower cost. However, when it comes to the increase in the switching frequency, it is limited due to the switching losses. Moreover, the magnitude of the switching voltage over each device in the 2L inverter is the same as the entire DC-link voltage, bringing large harmonics in the inverter output. On the other hand, the 3L inverters offer several advantages such as: half the DC-link voltage across each device, lower harmonics, lower switching losses and electromagnetic interference (EMI).

In Figure 1, the three topologies considered for the comparison in this paper are represented. Figure 1a shows the 2L inverter with SiC MOSFET power switches, while Figure 1b,c show the 3L NPC and 3L T-NPC topology with IGBT devices, respectively. When compared to the 2L inverter, the 3L NPC has a more complex structure and control due to the voltage imbalance problem between the two DC-link capacitors caused by the parameter mismatch of non-ideal components. Currently, this problem is solved by the use of more advanced modulation schemes [23]. Historically, the 3L NPC topology was developed for medium voltage applications, because the available devices had limited voltage blocking capability, and there was a need to connect devices in series. The eventual increase in the conduction losses has been outperformed by the gain in voltage handling capability. In the case of low voltage applications, this was not necessary since the available devices have sufficient voltage ratings and fast switching speeds. For this reason, the T-type topology is the better choice for low voltage applications, since there is no series connection of devices that has to block the whole DC-link voltage [12,24].

The T-type inverter on Figure 1c, a member of the NPC inverter topologies, offers three output voltage levels. Switches that are forming one phase leg (S_1 and S_4) in Figure 1c are rated at V_{DC} and bidirectional switches S_2 and S_3 are rated at $V_{DC}/2$. For this reason, the two middle switches (S_2 and S_3) have very low switching and conduction losses. When compared to the 3L NPC topology, the T-type inverter has several benefits. Due to the fact that there is no series connection of the devices that has to block the whole DC-link voltage, the uneven share of the voltage to be blocked in the case when IGBTs in series turn off at the same time cannot occur [12]. Another benefit can be seen in the usage of a single device to block the full DC-link voltage instead of two devices in series, leading to reduced conduction losses, if bipolar devices are considered.

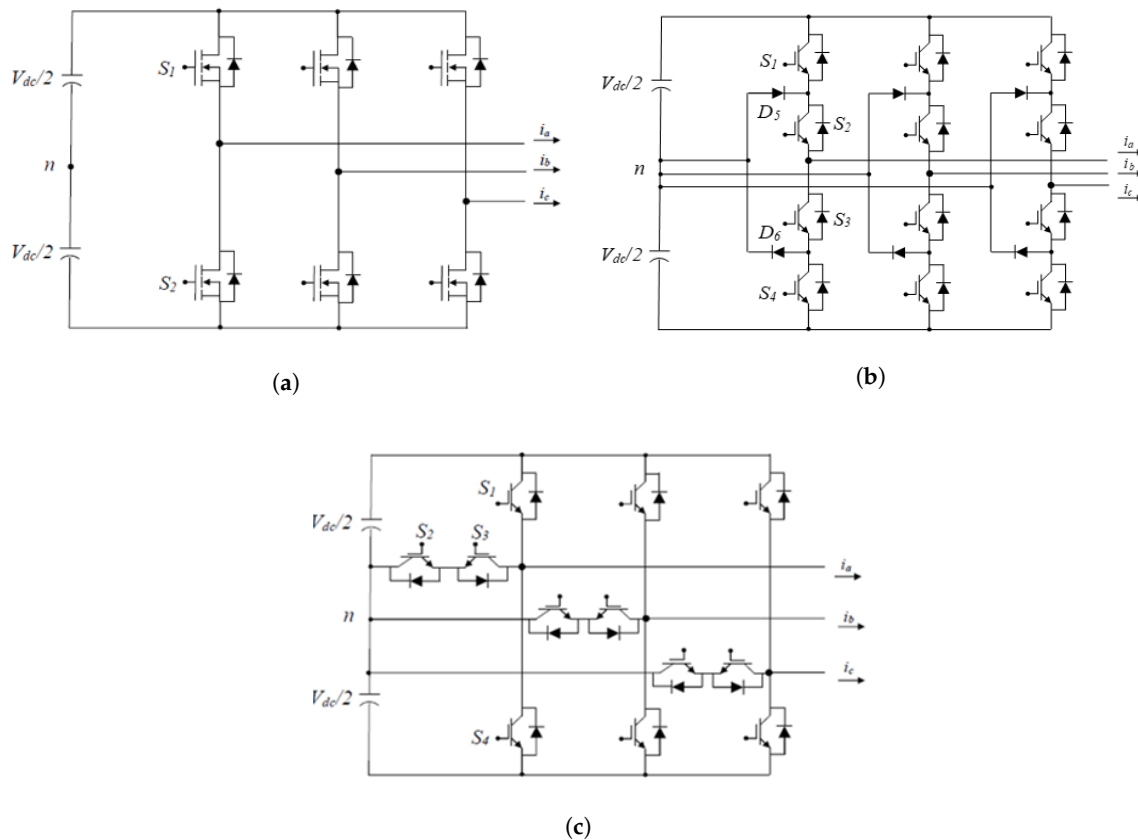


Figure 1. Inverter topologies in a motor drive application: (a) 2L SiC MOSFET, (b) 3L IGBT NPC, and (c) 3L IGBT T-NPC.

3. System Description and Overvoltage Comparison

For the overvoltage comparison, the three systems were analyzed using the simulation package LTspice. To have the same output voltage capabilities, the three inverters were supplied by total DC voltage $V_{DC} = 600$ V. The power modules' real models from the main producers were used for this analysis, i.e., the 1200 V SiC module SCT3080KLHR Rohm with the SiC Schottky anti-parallel diode SCS220KG Rohm for the 2L SiC based inverter, the 600 V IGBT module RGCL80TK60D Rohm for the 3L NPC IGBT based inverter, and the 1200 V RGS50TSX2DHR (leg switches) and 600 V RGCL80TK60D (middle switches) Rohm for the 3L T-NPC IGBT based inverter, with the main characteristics listed in Table 1. The reference was made to carrier based (CB) pulse width modulation (PWM) for the 2L inverter and phase disposition (PD) CB-PWM for the 3L inverter. The sizing of the inverters was done based on high speed drive requirements, considering the future application the high speed AC motor of 5 kW rated power and 48,000 rpm rated speed.

To have a fair comparison, the THD of the output current was set at the same value for the three systems, having in this way different switching frequencies, 60 kHz for the SiC based 2L inverter and 30 kHz for the 3L NPC and T-NPC inverter, while the fundamental frequency was set to 1.6 kHz. It was verified from the manufacturer's tests that two IGBTs can switch at a 30 kHz switching frequency for the maximum considered collector current.

For the overvoltage analysis, the transient analysis was introduced in LTspice, having the three inverter configurations supplying the high frequency (HF) motor model [25], as shown in Figure 2. The parameters of the model used for the simulation shown in Table 1 (motor and cable parameters) were obtained from the genetic algorithm, as explained in [25], and measurements on the real experimental setup, containing the SiC MOSFET based inverter, a 30 meter long cable, and a 0.37 kW induction motor, as explained in [7]. This system was used only to extract the high frequency motor circuit model parameters, which can approximately represent also other loads.

Table 1. Simulation parameters.

Device Parameters			
Parameters	Rohm SiC MOSFET SCT3080KLHR	Rohm Si IGBT RGCL80TK60D	Rohm Si IGBT RGS50TSX2DHR
V_{ds}	1200 V	600 V	1200 V
I_{ds} (25 °C)	31 A	35 A	50 A
I_{ds} (100 °C)	22 A	21 A	25 A
$R_{DS(on)}$ (25 °C)	80 m Ω	N/A	N/A
V_{CE-sat} (25 °C)	N/A	1.4 V	1.7 V
Q_g	60nC@18 V	98nC@15 V	67nC@15 V
V_{th}	2.7 V	5.5 V	6 V
V_{gs}	−4 to +22 V	± 30 V	± 30 V
T_j	175 °C	175 °C	175 °C
P_{diss} (25 °C)	165 W	57 W	395 W
r_{jc}	0.7 °C/W	2.62 °C/W	0.38 °C/W
Motor parameters			
Parameter (unit)	Value		
R_{p1} (k Ω)	7.13		
C_1 (pF)	761.02		
R_{c1} (Ω)	63.47		
L_1 (mH)	3.33		
R_{l1} (Ω)	679.43		
R_{p2} (M Ω)	55.55		
C_2 (nF)	5.31		
R_{c2} (k Ω)	21.04		
L_2 (mH)	16.80		
R_{l2} (Ω)	718.36		
C_g (pF)	231.51		
R_g (Ω)	2.56		
Cable parameters			
Parameter (unit)	Value		
R_{cable} (m Ω /m)	195.87		
L_{cable} (μ H/m)	0.63		
C_{cable} (pF/m)	63.33		

In particular, the three phase equivalent circuit in Figure 2 was used to model the cable lumped impedance (R_{cable} , L_{cable} , and C_{cable}) and the motor impedance. Each phase contained three resonators: the two external ones (accounting for the terminal part of the windings) and the central resonator (for the active part of the winding). Each resonator was made by the parallel connection of three branches: two resistances R_{p1} and R_{p2} took into account the eddy current HF path; the capacitive branch with C_1 or C_2 modeled the HF current path due to the turn-to-turn parasitic capacitance; and the inductive branch with L_1 or L_2 described the low frequency machine behavior. Moreover, two shunt capacitive branches were connected between the resonators and the ground, taking into account the parasitic coupling with the motor case.

Figures 3–5 show the terminal voltage of the AC motor (V_{mot_ab} , with the peak of the total voltage rise ΔV_{mot}) of the 2L SiC MOSFET based and 3L NPC and T-NPC IGBT based inverters, respectively. The transient analysis with the inverters supplying a high frequency motor load circuit was considered. The figures include a comparison when different power cable lengths are used, i.e., 3 m, 5 m, and 10 m (Figures 3a, 4a and 5a), and the case when gate resistance R_g is changed (Figures 3b, 4b and 5b). As can be seen from the figure, even in the case of a sufficiently short cable length of 3 m, the high dv/dt was induced at the motor terminals due to the fast rise time and the voltage reflection phenomenon. The 3L NPC and T-NPC inverter generally provided lower dv/dt than the 2L inverter. This was due to the fact that lower voltages were applied across each device in 3L inverters. In the case when the cable length was 10 m, a large high frequency transient could be noted, which did not expire, especially in the case of the 2L inverter. Overall, almost all dv/dt values were higher than the ones permitted by the standard on voltage stress in motors and drives.

Figures 3b, 4b and 5b show the change in the overvoltages for the fixed cable length (L_{cable}) and different values of the gate resistance. The external gate resistance (R_g) was varied as follows: $R_g = 10 \Omega, 20 \Omega, 30 \Omega$. For the higher values of R_g , the decrease in the overvoltages can be seen, since both the rise time was increased and the peak was decreased. In order to have a fair comparison for the three systems, the same overvoltages were considered, i.e., the value of R_g for the 2L SiC MOSFET based inverter was increased from 12Ω to 25Ω (resulting in the decrease of dv/dt from $11.68 \text{ kV}/\mu\text{s}$ to $8.6 \text{ kV}/\mu\text{s}$), while in the case of 3L inverters, R_g was kept the same, i.e., 10Ω . In this way, the same dv/dt of $8.6 \text{ kV}/\mu\text{s}$ for the three systems was considered, and the power loss comparison (using the steady state analysis) is given for that specific case in the following section. In addition, the THD of the output currents and the output voltage capabilities were the same.

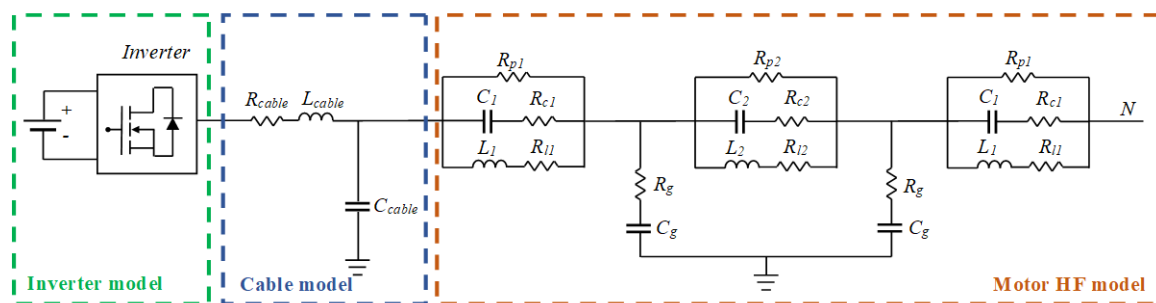


Figure 2. High frequency (HF) equivalent circuit of the inverter-cable-motor system.

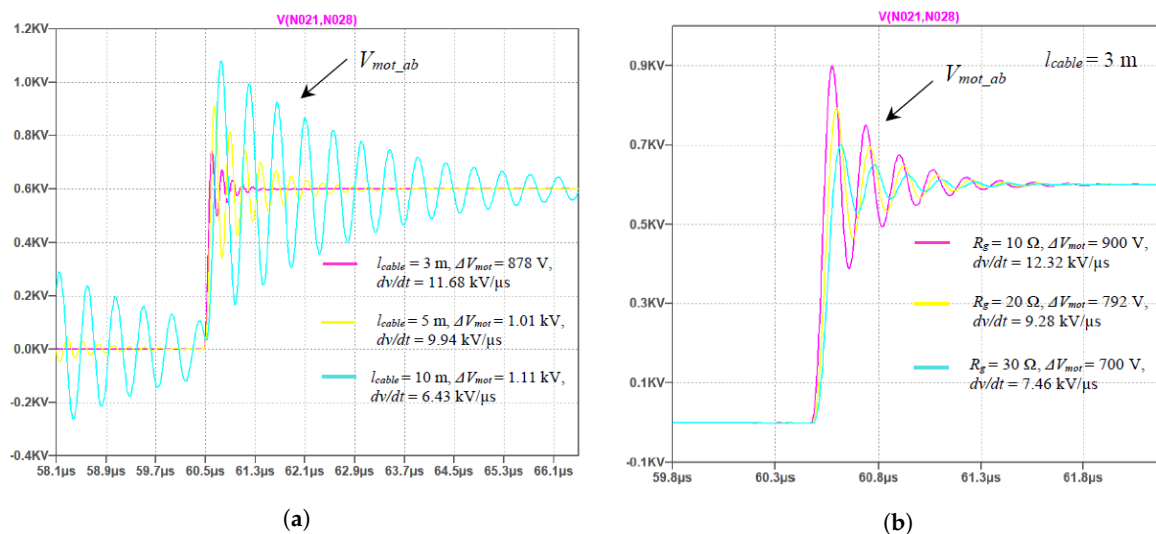


Figure 3. Simulation results of the motor line-to-line voltages for the 2L SiC MOSFET inverter in the case of: (a) different lengths of the power cable and (b) different values of gate resistance.

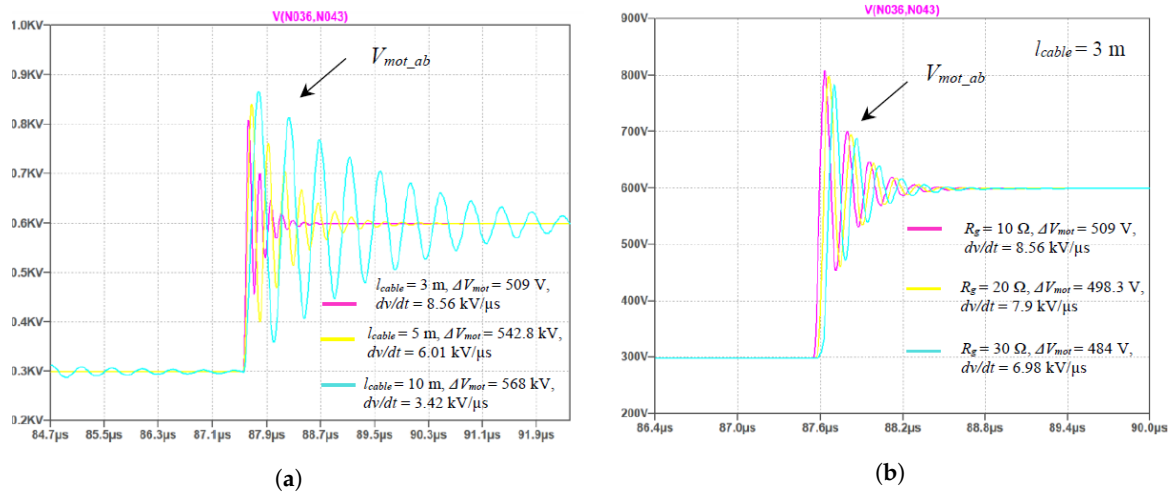


Figure 4. Simulation results of the motor line-to-line voltages for the 3L IGBT NPC inverter in the case of: (a) different lengths of the power cable and (b) different values of gate resistance.

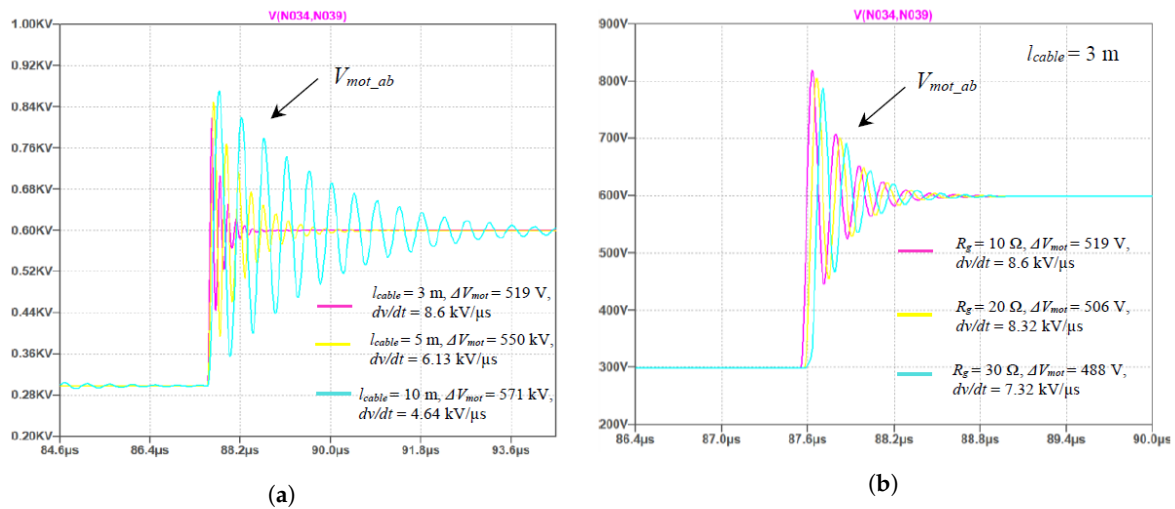


Figure 5. Simulation results of the motor line-to-line voltages for the 3L IGBT T-NPC inverter in the case of: (a) different lengths of the power cable and (b) different values of gate resistance.

4. Power Loss Analysis

Device losses were mainly resulting from two causes: the conduction losses and switching losses. The IGBT conduction loss model was obtained by using its dynamic on resistance $R_{on,IGBT}$ and zero on-state voltage V_0 , i.e.,

$$P_{con,IGBT} = V_0 I_{av} + R_{on,IGBT} I_{rms}^2 \quad (1)$$

where I_{av} and I_{rms} are the average and rms currents through the device. For the SiC MOSFETs, the on resistance $R_{DS(on)}$ was needed to determine conduction losses, i.e.,

$$P_{con,MOSFET} = R_{DS(on)} I_{rms}^2 \quad (2)$$

The conduction losses for the diodes were based on their threshold voltage V_T and dynamic on resistance $R_{on,diode}$, i.e.,

$$P_{con,diode} = V_T I_{av} + R_{on,diode} I_{rms}^2 \quad (3)$$

The switching losses had a linear relationship to the switched current. The overall averaged switching losses can be expressed as:

$$P_{sw,device} = f_{sw} \frac{1}{T} \int_{0+\phi}^{\frac{T}{2}} (E_{on,device} + E_{off,device}) dt \quad (4)$$

where $E_{on,device}$ and $E_{off,device}$ are the dissipated energy of the device during turning on and off and ϕ is the phase angle.

These equations are valid for the general case and are not connected to the specific application. In the next subsections are given the losses analysis connected to the specific applications, i.e., the 2L SiC MOSFET based inverter and NPC and T-NPC inverter.

4.1. 2L SiC MOSFET Based Inverter

When considering the specific applications, i.e., the 2L inverter adopting SiC MOSFET and the SiC Schottky diode, the losses can be calculated according to the following formulae [26]:

$$P_{con,MOSFET} = R_{DS(on)} I_{rms}^2 = R_{DS(on)} \hat{I}^2 \left(\frac{1}{8} + \frac{m \cos \phi}{3\pi} \right) \quad (5)$$

where \hat{I} is the peak value of the output current, m is the modulation index, $m = 2V^*/V_{DC}$, and V^* is the amplitude of the reference output voltage. Diode conduction losses can be expressed as:

$$P_{con,diode} = V_T I_{av} + R_{on,diode} I_{rms}^2 = V_T \hat{I} \left(\frac{1}{2\pi} - \frac{m \cos \phi}{8} \right) + R_{on,diode} \hat{I}^2 \left(\frac{1}{8} - \frac{m \cos \phi}{3\pi} \right) \quad (6)$$

For the switching losses, we can write:

$$P_{sw,device} = f_{sw} \frac{1}{\pi} \frac{\hat{I}}{I_{ref}} E_{sw,device} \quad (7)$$

where I_{ref} is the reference current value of the switching loss measurement, available in the component's datasheet.

4.2. NPC and T-NPC Inverter

In the case of the NPC and T-NPC inverter adopting the Si IGBT and Si diode, the conduction and switching losses can be expressed as follows [18,27]:

- NPC inverter:

$$P_{con,S_1\&S_4} = V_0 I_{av} + R_{on,IGBT} I_{rms}^2 = \frac{m \hat{I}}{12\pi} \{ 3V_0 [(\pi - \phi) \cos \phi + \sin \phi] + 2R_{on,IGBT} \hat{I} [1 + \cos \phi]^2 \} \quad (8)$$

m being the modulation index, $m = 2V^*/\sqrt{3} V_{DC}$.

$$P_{sw,S_1\&S_4} = f_{sw} E_{sw,device} \left(\frac{\hat{I}}{I_{ref}} \right)^{K_I} \left(\frac{V_{cc}}{V_{ref}} \right)^{K_V} \left\{ \frac{1}{2\pi} [1 + \cos \phi] \right\} G_I \quad (9)$$

where V_{cc} is the collector-emitter supply voltage and I_{ref} and V_{ref} are the reference current and voltage of the switching loss measurement available in the component's datasheets, respectively. The coefficients K_I , K_V , and G_I [27] are defined as:

- $K_I = 1$ for IGBT and $K_I = 0.6$ for diode,
- $K_V = 1.4$ for IGBT and $K_V = 0.6$ for diode,
- $G_I = 1$ for IGBT and $G_I = 1.15$ for diode

For diodes, we can write:

$$P_{con,D_1\&D_4} = V_T I_{av} + R_{on,diode} I_{rms}^2 = \frac{m\hat{I}}{12\pi} \{3V_T[-\phi\cos\phi + \sin\phi] + 2R_{on,diode}\hat{I}[1 - \cos\phi]^2\} \quad (10)$$

$$P_{sw,D_1\&D_4} = f_{sw} E_{sw,device} \left(\frac{\hat{I}}{I_{ref}}\right)^{K_I} \left(\frac{V_{cc}}{V_{ref}}\right)^{K_V} \left\{\frac{1}{2\pi}[1 - \cos\phi]\right\} G_I \quad (11)$$

For the remaining two switches, S_2 and S_3 in Figure 1b, we can write:

$$P_{con,S_2\&S_3} = \frac{\hat{I}}{12\pi} \{V_0[12 + 3m(\phi\cos\phi - \sin\phi)] + R_{on,IGBT}\hat{I}[3\pi - 2m(1 - \cos\phi)^2]\} \quad (12)$$

$$P_{sw,S_2\&S_3} = f_{sw} E_{sw,device} \left(\frac{\hat{I}}{I_{ref}}\right)^{K_I} \left(\frac{V_{cc}}{V_{ref}}\right)^{K_V} \left\{\frac{1}{2\pi}[1 - \cos\phi]\right\} G_I \quad (13)$$

$$P_{con,D_2\&D_3} = \frac{m\hat{I}}{12\pi} \{3V_T[-\phi\cos\phi + \sin\phi] + 2R_{on,diode}\hat{I}[1 - \cos\phi]^2\} \quad (14)$$

$$P_{sw,D_2\&D_3} = 0 \quad (15)$$

For diodes D_5 and D_6 , we can write:

$$P_{con,D_5\&D_6} = \frac{\hat{I}}{12\pi} \{V_T[12 + 3m[(2\phi - \pi)\cos\phi - 2\sin\phi]] + R_{on,diode}\hat{I}[3\pi - 4m(1 + \cos^2\phi)]\} \quad (16)$$

$$P_{sw,D_5\&D_6} = f_{sw} E_{sw,device} \left(\frac{\hat{I}}{I_{ref}}\right)^{K_I} \left(\frac{V_{cc}}{V_{ref}}\right)^{K_V} \left\{\frac{1}{2\pi}[1 + \cos\phi]\right\} G_I \quad (17)$$

Similarly, for the T-NPC inverter, we can write the following equations:

- T-NPC inverter:

$$P_{con,S_1\&S_4} = \frac{m\hat{I}}{12\pi} \{3V_0[(\pi - \phi)\cos\phi + \sin\phi] + 2R_{on,IGBT}\hat{I}[1 + \cos\phi]^2\} \quad (18)$$

$$P_{sw,S_1\&S_4} = f_{sw} E_{sw,device} \left(\frac{\hat{I}}{I_{ref}}\right)^{K_I} \left(\frac{V_{cc}}{V_{ref}}\right)^{K_V} \left\{\frac{1}{2\pi}[1 + \cos\phi]\right\} G_I \quad (19)$$

For diodes, we can write:

$$P_{con,D_1\&D_4} = \frac{m\hat{I}}{12\pi} \{3V_T[-\phi\cos\phi + \sin\phi] + 2R_{on,diode}\hat{I}[1 - \cos\phi]^2\} \quad (20)$$

$$P_{sw,D_1\&D_4} = f_{sw} E_{sw,device} \left(\frac{\hat{I}}{I_{ref}}\right)^{K_I} \left(\frac{V_{cc}}{V_{ref}}\right)^{K_V} \left\{\frac{1}{2\pi}[1 - \cos\phi]\right\} G_I \quad (21)$$

For the switches S_2 and S_3 in Figure 1c, we can write:

$$P_{con,S_2\&S_3} = \frac{\hat{I}}{12\pi} \{V_0[12 + 6m(\phi\cos\phi - \sin\phi) - 3m\pi\cos\phi] + R_{on,IGBT}\hat{I}[3\pi - 4m(1 + \cos^2\phi)]\} \quad (22)$$

$$P_{sw,S_2\&S_3} = f_{sw} E_{sw,device} \left(\frac{\hat{I}}{I_{ref}}\right)^{K_I} \left(\frac{V_{cc}}{V_{ref}}\right)^{K_V} \left\{\frac{1}{2\pi}[1 - \cos\phi]\right\} G_I \quad (23)$$

$$P_{con,D_2\&D_3} = \frac{\hat{I}}{12\pi} \{V_T[12 + 6m(\phi\cos\phi - \sin\phi) - 3m\pi\cos\phi] + R_{on,diode}\hat{I}[3\pi - 4m(1 + \cos^2\phi)]\} \quad (24)$$

$$P_{sw,D_2\&D_3} = f_{sw} E_{sw,device} \left(\frac{\hat{I}}{I_{ref}} \right)^{K_I} \left(\frac{V_{cc}}{V_{ref}} \right)^{K_V} \left\{ \frac{1}{2\pi} [1 + \cos\phi] \right\} G_I \quad (25)$$

4.3. Double Pulse Test and PLECS Analysis

The simulation package PLECS enables the user to merge the thermal design with the electrical design, providing in this way the requirements for the cooling solution suitable for the particular application. The switches are ideal, and the switching and conduction losses are inserted in terms of 3D look-up tables for the specific semiconductor's operating condition (forward current, blocking voltage, junction temperature) before and after each switch operation. In this way, depending also on the application, the simulation speed is not necessarily affected. Moreover, there is the possibility to use steady state analysis, which skips the long transient in the thermal analysis and displays the steady state. The thermal description of the device is done by a thermal network, either Cauer or Foster.

To determine the device switching and conduction losses, the standard double pulse test was used for each device in LTspice, as presented in Figure 6a in the case of IGBT. In Figure 6b are presented the turn on losses in the case of the 600 V IGBT RGCL80TK60D Rohm. In the double pulse test, the first gate pulse was used to charge the inductive load L to a desired current level, and the freewheeling diode (FWD) was used to keep the current level when the device under test (DUT) was off. A second short pulse was used for IGBT switching transient characterization. It is to be noted that when IGBT was used with a fast recovery diode, the diode losses were not added to the IGBT's turn on losses, but presented with turn off losses as the negative part. Similarly, also the losses for the SiC MOSFET can be introduced.

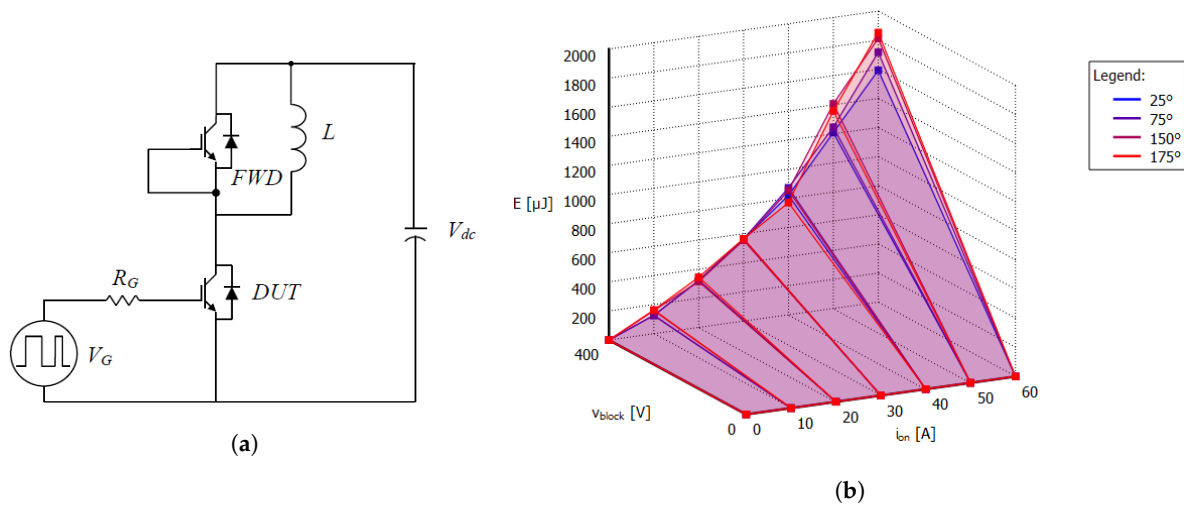


Figure 6. Double pulse test: (a) schematic of the double pulse test and (b) example of the IGBT's switching on losses for different temperatures.

After the losses' description was added in PLECS, it was possible to place the heat sink and obtain the device junction and case temperatures, as well as the respective losses for a specific application.

4.4. Power Loss Comparison

Switching and conduction losses were analyzed using the power electronics simulation package LTspice and PLECS, as explained in Section 4.3. Namely, from the double pulse test on real device models in LTspice, the conduction and switching losses were obtained. These losses were introduced in the look-up tables that the PLECS simulation package was using for the characterization of each device. The complete inverter-passive RL load systems were then developed in PLECS, having the three inverter configurations. Moreover, for a fair comparison, the same overvoltages were set for the three systems, having a 25 Ω gate resistance value in the case of the 2L SiC based inverter, while for

the NPC and T-NPC inverters, the values from the datasheet were kept ($R_g = 10 \Omega$). Consequently, also the double pulse tests and analytical considerations were done considering these values. The fact that the gate resistance for the 2L SiC inverter was much higher than the value from the datasheet, i.e., 12Ω , can be considered a somewhat unrealistic condition for the 2L SiC inverter, but it is useful for the comparison; in this way, the three systems could be compared for the same value of dv/dt .

The same conditions were kept as in Section 3, i.e., the same output voltage capabilities and the same output current THD, just in this case, the inverters were supplying passive RL load. The PLECS simulation package used for the steady state analysis enabled a fast way to obtain the steady state and also provided the cooling solution. Figure 7 shows the comparison of the analytical (as presented in Section 4.2) and simulation losses in the case of the T-NPC inverter for the maximum output power, i.e., 11.4 kW. The good agreement between the analytical results and the results obtained with the PLECS simulation package can be noted from the figure.

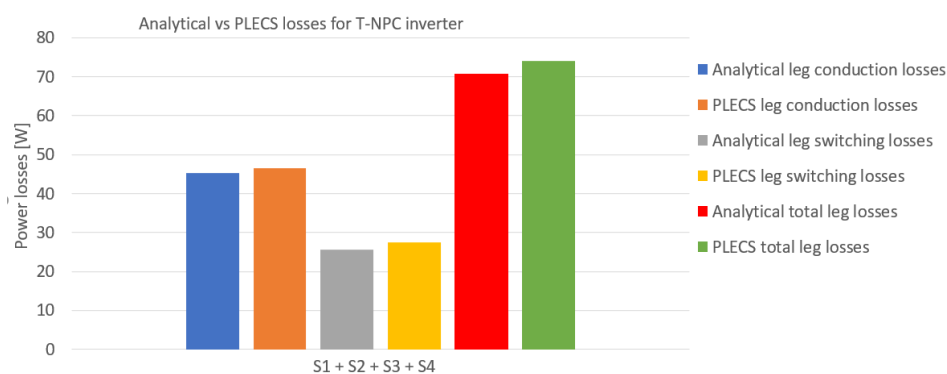


Figure 7. Analytical and simulation switching, conduction, and total losses of one inverter leg with maximum output power for the 3L T-NPC IGBT based inverter

Figure 8 summarizes the analytical and simulation total losses of one inverter leg in the case of the inverter output power having different values. Total losses of the three configurations in the case of the fair comparison, i.e., same voltage capabilities, same output current THD, and same overvoltage, were almost the same for low output powers, i.e., 25% of the maximum output power. For higher values of the output power, the 2L SiC inverter had a greater increase in the total losses when compared to the NPC and T-NPC inverter. In the case of 50% of the max power, the 2L SiC inverter had 14% more losses than the NPC inverter and 30% more losses than the T-NPC inverter. For the maximum output power, the 2L SiC inverter had 42% more losses when compared to the lowest, which in this case was the T-NPC inverter. The T-NPC inverter had also slightly lower losses than the NPC inverter, as expected.

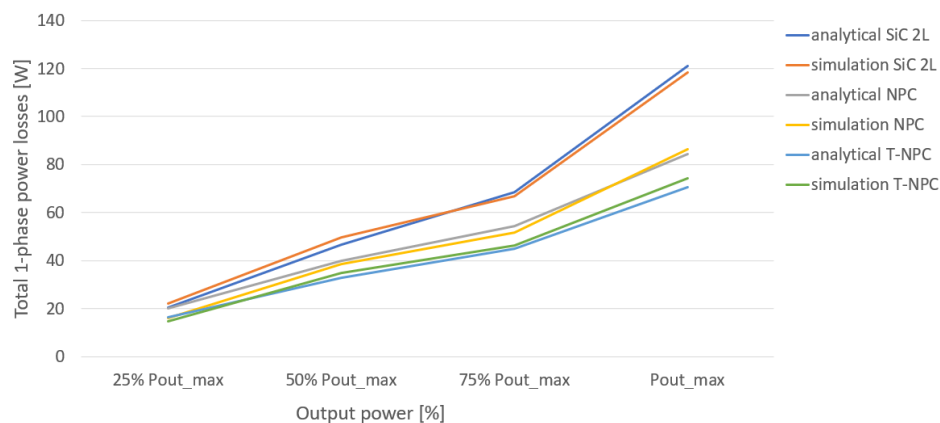


Figure 8. Analytical and simulation total one phase power device losses of the inverters with different values of the output power.

4.5. Heat Sink Volume

The thermal network of switching devices is presented in Figure 9a. N is the number of devices; T_j is the junction temperature; r_{jc} is the junction to case thermal resistance; r_{ch} is the case to heat sink thermal resistance; r_h is the heat sink thermal resistance; T_c is the case temperature; and T_a is the ambient temperature.

The heat sink volume analysis was based on the power losses of three systems at maximum output power and considering heat sink temperatures between 75 °C and 125 °C. According to Figure 9a, we can write the following expressions:

$$T_{j1\dots n} = P_{loss1\dots n} \frac{r_{jc1\dots n} + r_{ch1\dots n}}{2} + T_h \tag{26}$$

$$r_h = \frac{T_h - T_a}{P_{tloss}} \tag{27}$$

where P_{tloss} is the total inverter loss.

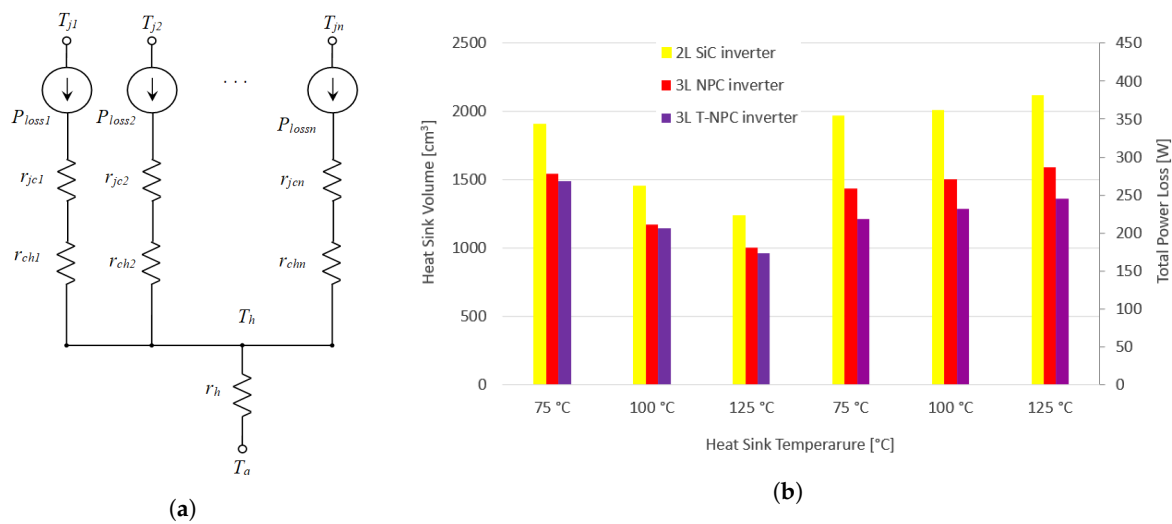


Figure 9. Heat sink design: (a) general thermal network; (b) heat sink volume and total inverter power loss for three inverters and different heat sink temperatures.

The calculated r_h can be used to calculate the heat sink volume based on natural air convection. The calculation of the fitting function applied to the minimum heat sink volume available at a given r_h value can be found in [18]:

$$Vol_{heatsink} = 3263e^{-13.09r_h} + 1756e^{-1.698r_h} \tag{28}$$

Equation (28) [18] is obtained from the curve fitting based on the volume of various extruded naturally cooled heat sinks against heat sink thermal resistance.

Heat sink volume calculations for three different inverters with respect to heat sink temperature are presented in Figure 9b. A room temperature of 25 °C was chosen for the ambient temperature. The results showed that the 2L SiC MOSFET based converter had an increase of around 20% in the heat sink volume when compared to the 3L NPC and T-NPC inverter at a 75 °C heat sink temperature. The same trend can be seen also for the other temperature values. Additionally, the volume of the heat sink can be reduced by a factor of 1.5 for the SiC based inverter by increasing the temperature from 75 °C to 125 °C, which on the other hand would bring 7% more losses. The 3L NPC and T-NPC inverters had a similar heat sink volume, with T-NPC being slightly lower (4% in the case of a 75 °C heat sink temperature).

5. System Cost Analysis

In this section are given the costs of the inverter-motor system, taking into account only the switching devices together with gate drivers and the heat sink. Since the fair comparison considered the same dv/dt for the three systems, the output filters were considered of the same volume and were not taken into account for this analysis. The same price was considered for the other components as the price difference was none or negligible, and therefore was not included in this comparison. In particular, two cases were considered, when inverters were working with their maximum rated capacity and when they were working with 50% of the maximum rated capacity. Note that the prices in Table 2 are given in per unit, referring to the sample prices of the main parts' manufacturers in Europe.

Table 2. System cost comparison.

Component	NPC	T-NPC	2L SiC
Switching device/price trend (p.u.)	24.85/stable	27.43/stable	55.71/strong reduction
Heat sink/ P_{out_max} (p.u.)	20.74	17.68	27.23
Heat sink/50% P_{out_max} (p.u.)	12.55	10.8	14.32
Total cost/ P_{out_max} (p.u.)	45.6	45.1	82.94 ↓
Total cost/50% P_{out_max} (p.u.)	37.4	38.23	70.03 ↓

For all the considered cases, the 3L NPC IGBT based inverter showed the lowest total cost and the 2L SiC MOSFET based inverter the highest. When considering only the device cost, the 2L SiC MOSFET based inverter had more than two-times the cost of the NPC and T-NPC inverter. In the case of P_{out_max} , the total cost of the 2L SiC inverter was around 1.8-times the cost of the NPC inverter and T-NPC inverter. It was similar also in the case of 50% P_{out_max} . It is interesting to notice that the total cost of the T-NPC inverter was similar to the NPC inverter, but offering a 16% reduction of the losses when considering the case when inverters were working with maximum output power. The price of the 2L SiC inverter was dominant in all the considered cases, also when taking into account the passive components. However, a strong cost reduction in upcoming years for SiC devices is expected, so that fact is likely to change.

In Table 3 are summarized all the features analyzed in this paper for the three inverters, in terms of transient analysis where the dv/dt are given and steady state analysis where the losses, heat sink volume, and costs are given for the fair comparison.

Table 3. Summary.

Descriptors	NPC	T-NPC	2L SiC
Transient analysis/LTspice			
dv/dt for $l_{cable}=3$ m (kV/ μ s)	8.56	8.6	11.68
dv/dt for $l_{cable}=5$ m (kV/ μ s)	6.01	6.13	9.94
dv/dt for $l_{cable}=10$ m (kV/ μ s)	3.42	4.64	6.43
Steady-state analysis/PLECS			
Total losses @75 °C/50% P_{out_max} (W)	120	98.34	139.4
Total losses @75 °C/ P_{out_max} (W)	258.9	218.6	355
Heat sink volume/50% P_{out_max} (cm ³)	878.9	756	1002.6
Heat sink volume/ P_{out_max} (cm ³)	1452.9	1237.8	1906.5
Total cost/50% P_{out_max} (p.u.)	37.4	38.23	70.03 ↓
Total cost/ P_{out_max} (p.u.)	45.6	45.1	82.94 ↓

By looking at the transient analysis, it is clear that the 2L SiC inverter has a higher dv/dt , in some cases almost double. When it comes to the steady state analysis, for 50% of the output power and less, we could say that the 2L SiC inverter could be a better choice for a high speed motor drive system. This is, however, premature to say since the cost of the 2L SiC inverter and SiC devices in general is still rather high. With the reduction in the SiC devices' price, the need to mitigate the overvoltage problem in SiC based inverters is essential and inevitable, as they offer several benefits such as high

frequency operation and reduction in heat sink volume and output inductor volume when operated in realistic conditions, i.e., with lower values of gate resistance.

6. Conclusions

This paper discussed the comparison of the 2L SiC MOSFET based and 3L NPC and T-NPC Si IGBT based inverters in terms of the efficiency, overvoltages on motor terminals, heat sink design, and cost of the inverter-motor load system. The three systems considered a low voltage high speed electric drive application with a long power cable. A fair comparison was introduced for the first time and was based on the fact that the output voltages of the inverters were set in such a way as to produce along the cable and at motor terminals the same overvoltage for the three systems. The overvoltages are known to be the main cause of the partial discharge occurring in the stator winding, greatly influencing the life time and the reliability of an electric drive. To have a fair comparison, inverters had the same output voltage capabilities, the same output current THD, and the same overvoltages on motor terminals. The analysis was conducted on power modules' real dynamic models obtained from the manufacturer's experimental tests in the LTspice simulation tool (for the overvoltage and double pulse tests analysis) and the PLECS simulation package for the power losses and heat sink comparison.

The overvoltages were compared by using a high frequency motor-load circuit and considering three lengths of the power cable (3, 5, and 10 m). In most of the cases, high dv/dt could be noted, not complying with the standards on voltage stress in motors and drives.

Power loss comparison and steady state analysis where the inverters were supplying passive RL load were done in the PLECS simulation package. Switching and conduction losses were obtained by performing double pulse tests in LTspice on the devices' realistic dynamic models. In this case, a fixed length of the power cable (3 m) was considered, and the gate resistance was set in order to have the same overvoltages for the three systems. A power loss comparison was conducted for that specific case in PLECS, showing similar switching losses for the 2L SiC based VSI and 3L VSIs in the case of lower output power (less than 50% of the maximum output power). Moreover, the power loss analysis showed good agreement between the analytical and simulation results.

The heat sink volume was compared for the maximum inverter output power for the three systems. The SiC MOSFET based inverter, in this specific case of the fair comparison, had a 20% increase in the volume when compared to 3L Si IGBT based inverters for all the considered heat sink temperatures. It could, however, be reduced by the factor of 1.5 by increasing the heat sink temperature from 75 °C to 125 °C, which on the other hand would bring 7% more losses. The 3L T-NPC inverter had the lowest heat sink volume and lowest losses for all the considered temperatures.

For the inverter-motor cost analysis, two cases were considered, when inverters were working with their maximum rated capacity and when they were working with 50% of the maximum rated capacity. For all the considered cases, the 3L NPC IGBT based inverter had the lowest cost and 2L SiC MOSFET based inverter the highest, with 1.8-times the total cost of the NPC inverter and T-NPC inverter. With the price reduction in the next few years for SiC devices, this is likely to change, and 2L SiC based inverters can become competitive for high speed motor drives in the future.

Speaking for the present, the 2L SiC MOSFET based VSIs can be seen as a better solution when compared to the 3L NPC inverter in the case when the inverter is working at low output power. When considering higher output power and the upcoming price reduction of the SiC devices, the need to mitigate the overvoltage problem in SiC based inverters is inevitable, as they can offer several benefits such as high frequency operation, reduction in heat sink volume, etc. Moreover, the 2L inverter configuration is more reliable when compared to 3L configuration and could benefit from the usage of SiC devices.

Future work will include more detailed comparisons, including the experimental verification, but also other hybrid topologies. The investigation for the potential solutions for switching performance improvements and mitigation of reflected waves, as well as the future study of electric aging phenomena can then be performed.

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