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SiPM Readout Electronics

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Abstract

Due to the peculiar characteristics of SiPM sensors in terms of equivalent capacitance, gain and fast rise-time response, in several applications classic readout solutions for radiation detectors are not able to provide optimal performance. Thus, several ad hoc readout approaches have been developed to fully exploit the favorable features of this kind of detectors. In this note the main requirements for the SiPM readout electronics are discussed, for both energy and time measurements, in the light of the detector model, and an overview of the main architectures commonly employed is provided, along with a set of relevant design examples.

Keywords: SiPM; front-end electronics; readout ASIC

1. Introduction

Nowadays Silicon Photo-Multipliers (SiPM) represent a well consolidated and cost effective technology for a large range of applications requiring the detection of low light levels. In the last years, remarkable research efforts have been devoted, on the one hand, to improve the basic performance of this kind of detectors, for instance increasing the Photon Detection Efficiency (PDE), and, on the other hand, to reduce the impact of their

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main drawbacks, such as dark count rate, afterpulsing and optical crosstalk [1]. As a result, the possible application spectrum of SiPM detectors becomes wider and wider [2], covering fields where traditionally they have been considered a valid replacement for PMTs, such as Time of Flight Positron Emission Tomography (ToF-PET) [3] and calorimetry [4], but also more recently emerging areas, such as Light Detection and Ranging (LiDAR) [5] and Time Correlated Single Photon Counting (TCSPC) [6].

Often, front-end electronics plays a fundamental role in meeting the relevant specifications of a detection system based upon SiPMs and, in some cases, it even represents the bottleneck that limits the system performance. For instance, the Single Photon Time Resolution (SPTR) that is possible to achieve with a SiPM detector of large area is strongly dependent on the contribution of electronic noise [7], which causes statistic fluctuations of the instant when the output signal overcomes the chosen threshold. Thus, full exploitation of the favourable features of the detector requires the availability of suitable solutions for the front-end electronics, well-tuned to the peculiar characteristics of the SiPM. For energy measurements, often the main issue is not represented by the electronic noise, because of the large gain of the detector, around 10^6. Typically, energy resolution is dominated by the intrinsic noise of the detector, associated to afterpulsing, optical crosstalk, dark pulses and gain fluctuations among the micro-cells. Moreover, in the applications where a SiPM is used to read-out a scintillator, the accuracy of the energy measurements is also strongly affected by the statistics of the photons released by the crystal.

The classic Charge Sensitive Amplifier (CSA) shown schematically in Fig. 1, which is the standard front-end configuration for radiation detectors, due to its very good noise performance, often does not represent an optimal solution for a SiPM.

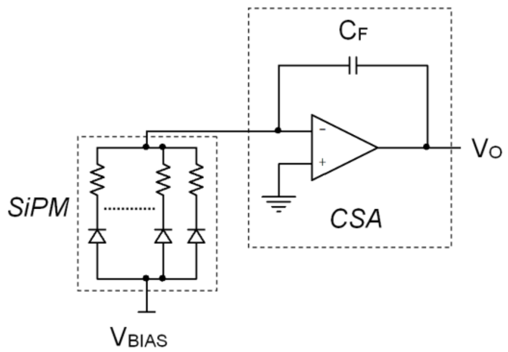

Fig. 1. Charge Sensitive Amplifier (CSA) coupled to a SiPM.

In fact, several applications are characterized by large values of the maximum input charge, due to the high gain of the detector, which makes direct charge integration on the feedback capacitance C_F impractical. Large values of the integration capacitance are needed, to limit the charge-to-voltage gain $1/C_F$ of the CSA, especially when deep-submicron CMOS technologies are used and the allowed voltage headroom is very limited, due to the low supply voltage. For instance, in a PET application with the detector coupled to an LSO crystal, the number of photoelectrons contributing to the SiPM signal can reach 2000 [8] and, if the SiPM gain is 10^6, this corresponds to an input charge of 320pC. If the maximum output voltage swing of the amplifier in Fig. 1 is 1V, the feedback capacitance needed would be 320pF, which is not feasible in a standard CMOS technology employed to design multichannel readout ASICs. Even though the requirement in terms of maximum input charge is relaxed with respect to the example above, the integration capacitance must be always quite large. This means that, if the electronics must preserve the fast rising edge of the signal produced by the detector in order to achieve good accuracy in time measurements, the amplifier must be able to drive large values of load capacitance while featuring large bandwidth, which is possible only if power consumption is adequately increased. Other issues can arise in terms of stability problems, once again due to large capacitive loads.

Concerning time measurements, in the vast majority of the SiPM applications Leading Edge Discrimination (LED) is adopted as time pick-off method and the uncertainty in the evaluation of the occurrence time of the detected event σ_t is related to the slope of the output signal of the front-end V_{OUT} around the chosen threshold V_{TH}, according to the well-known relation

$$\sigma_t = \frac{\sigma_n}{\left.\frac{dV_{OUT}}{dt}\right|_{V_{OUT}=V_{TH}}} \qquad (1)$$

where σ_n is the rms output noise of the front-end electronics [9]. The most relevant part of the charge released by the SiPM is contained in the long tail of its current pulse, characterized by a very slow time constant, thus the collection time of this fraction of the total charge is very long and the rise time of the output voltage of a CSA coupled to the detector is determined by this slow time constant. As a consequence, a front-end solution based on the CSA is not able to fully exploit the intrinsic fast leading edge of the current pulse generated by the SiPM and requires the introduction of a fast shaper, which basically, starting from the output of the integrator, tries to reconstruct a signal with fast rising edge, to be compared to a given threshold by means of a fast discriminator.

Instead of using a CSA, the most widespread approaches, adopted in several realizations of readout circuits for SiPM detectors, are based on interfacing the detector with a front-end at the same time able to preserve the intrinsic speed of the signal generated by the detector, thanks to well suited input impedance, and to reproduce at its output a replica of this signal, which can be conveniently applied to a fast discriminator for the extraction of the time information [10]. The choice of the most suitable solution for the electronics requires the availability of an accurate electric model of the SiPM, useful for reliably reproducing in simulations the interaction between the detector and the front-end electronics and much research work has been devoted in the past, and still is, to this task [11-13]. In any case a SiPM is always characterized by remarkable values of equivalent capacitance, especially when it is composed by a large number of micro-cells, thus the front-end architecture must cope with this feature.

The purpose of this note is discussing the issues related to the different approaches to the readout electronics for SiPMs, in the light of the characteristics of the detector, for both energy and time measurements. Some relevant solutions and realizations, representative of the different approaches, together with details about the implementation of the most relevant building blocks, will be also presented, trying to describe the progresses done and to understand the current trends.

2. SiPM signal and front-end electronics

As pointed out in the previous section, in many applications the classic CSA approach is not well suited for the readout of a SiPM, especially in multichannel integrated realizations using recent CMOS technologies, due to dynamic range, power consumption, stability and speed of response. Nevertheless, in applications characterized by limited input charge range, severe noise requirements and relaxed timing accuracy specifications, a CSA based front-end can be an interesting solution, due to its very good noise performance. Low gain SiPMs, with small micro-cell size and low total equivalent capacitance, can be conveniently read-out with a CSA preamplifier. An example of this kind of circuit is the ASIC VATA64HDR16 [14], which has been used, for instance, to read-out SiPM arrays coupled to continuous scintillation crystals for medical imaging applications [15] and in the detection of Cherenkov light, operating the detectors in photon counting mode [16].

Another possible solution, especially if timing accuracy is of interest, can be the transimpedance amplifier (TIA), depicted in Fig. 2.

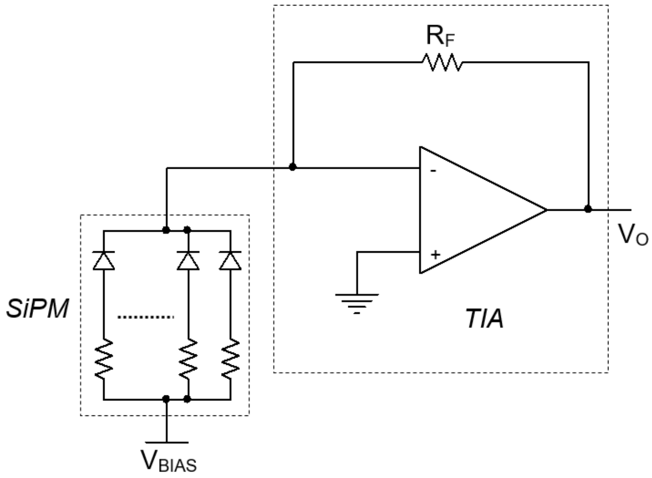

Fig. 2. Transimpedance amplifier (TIA) coupled to a SiPM.

The TIA converts the current pulse of the SiPM into a voltage and, if its bandwidth is large enough, it is able to preserve the fast rise time of the SiPM signal, thus enabling the achievement of good timing performance, according to (1). The main issue with this approach is once again the large equivalent capacitance of the detector C_{DET}: if acceptable values of the current to voltage gain, i.e. of the feedback resistor R_F, are needed, the quite slow pole formed by R_F and C_{DET} at the input of the amplifier causes stability problems, which can be mitigated only by adding a compensation capacitance in parallel to R_F, thus limiting the closed loop bandwidth of the system, with detrimental effects on the timing accuracy. Moreover if also the energy information is needed, the output signal of the TIA must be integrated, which can be done with an integrator/shaper, often based on an active filter implementation that requires a voltage to current conversion. Thus, with this approach, the current pulse of the detector is first converted into a voltage, then back again into a current and finally integrated.

Let us now consider a classic model of the SiPM [11,12,17] coupled to a generic front-end preamplifier characterized by input impedance R_{IN}, depicted in Fig. 3.

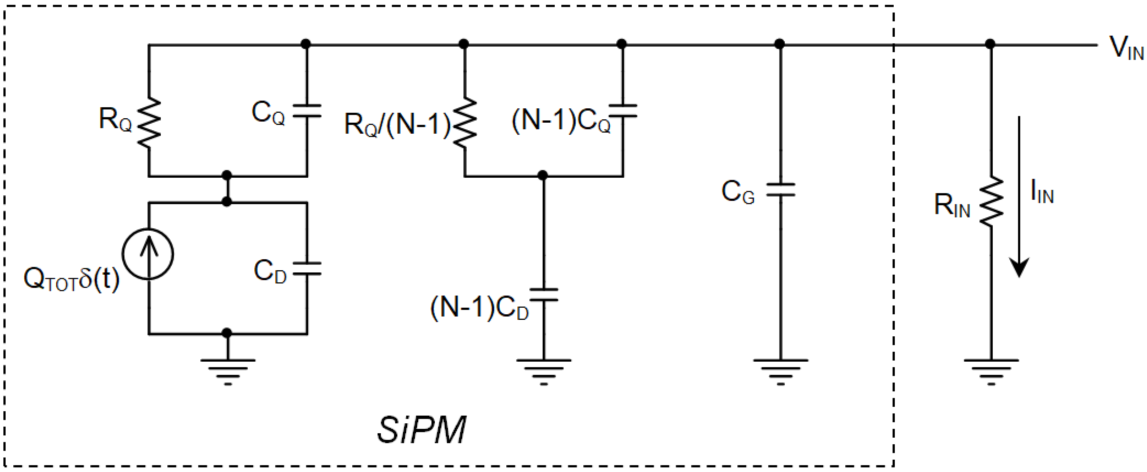

Fig. 3. SiPM model coupled to a generic preamplifier with input impedance R_{IN}.

In Fig. 3, C_D is the capacitance of the photodiode in the micro-cell of the SiPM, R_Q is the quenching resistance, C_Q is the small parasitic capacitance in parallel to R_Q and C_G accounts for the total parasitic capacitance associated to the large routing interconnections among all the micro-cells. In the left part of the figure a single fired micro-cell is represented and the avalanche current is represented as an ideal Dirac's pulse containing the total charge released by the detector

$$Q_{TOT} = \left(C_D + C_Q\right)\left(V_{BIAS} - V_{BR}\right) = \left(C_D + C_Q\right)\Delta V \qquad (2)$$

where V_{BIAS} is the bias voltage of the detector and V_{BR} is the breakdown voltage of the micro-cells. A Dirac's delta can be conveniently used to describe the avalanche current, since avalanche breakdown is very fast as compared to the time constant introduced by the circuit, especially considering the limitations inevitably introduced by the bandwidth of the amplifier. In the central part of Fig. 3, the load of the other N-1 micro-cells is inserted. It is useful to notice that the same circuit can also be used to model the case in which more than one micro-cell fires, by applying the superposition principle. The presence of C_Q accounts for the fast rising edge of the voltage V_{IN} at the input of the amplifier, since, without this parasitic capacitance, the charge collection would be dominated by the very slow time constant R_QC_D. In other words, C_Q represents a fast path for the charge generated by the avalanche towards the external circuit, since a fraction $Q_F= Q_{TOT}C_Q/(C_D+C_Q)$ of the total charge delivered by the avalanche flows almost instantaneously in C_Q and reaches very quickly the input node of the preamplifier. An approximate analysis of the circuit provides the following expression of the contribution $V_{INF}(t)$ of the "fast" charge Q_F to the input voltage of the preamplifier:

$$V_{INF}(t) \cong \frac{Q_F}{C_{HF}} e^{-\frac{t}{\tau_F}} , \qquad (3)$$

where, for low values of R_{IN}, which are commonly used in the applications as explained in the following, the time constant τ_F is

$$\tau_F \cong R_{IN} C_{HF} \qquad (4)$$

and C_{HF} is the equivalent capacitance of the detector for high frequencies

$$C_{HF} \cong C_G + N \frac{C_D C_Q}{C_D + C_Q}. \qquad (5)$$

In practice, eq. (3) states that the "fast" charge Q_F is almost immediately collected onto the high frequency equivalent capacitance of the detector C_{HF}, which is then discharged on the input resistance of the preamplifier R_{IN}. Note that Eq. (3) works very well in the first few ns after the micro-cell is fired, since the capacitance C_{HF} can be conveniently used to describe the behavior of the detector only for fast transients. The input capacitance C_{IN} of the electronics does not play a relevant role, since normally it is negligible compared to C_{HF}.

Concerning the rest of the total charge Q_{TOT}, i.e. $Q_D = Q_{TOT}C_D/(C_D+C_Q)$, it is associated to the discharge current $I_D(t)$ of the capacitance C_D through the parallel connection of C_Q and R_Q, according to the slow recovery time constant of the SiPM $\tau_R= R_Q(C_D+C_Q)$:

$$I_D(t) = \frac{Q_D}{\tau_R} e^{-\frac{t}{\tau_R}} \quad . \qquad (6)$$

Considering again an approximate analysis of the circuit, the corresponding contribution to the input voltage of the preamplifier is the following $V_{INS}(t)$:

$$V_{INS}(t) \cong R_{IN} \frac{Q_D}{\tau_S - \tau_F} \left(e^{-\frac{t}{\tau_S}} - e^{-\frac{t}{\tau_F}}\right) , \qquad (7)$$

which exhibits a rise time dominated by the fast time constant τ_F and a long tail dominated by the slow time constant τ_S:

$$\tau_S \cong \tau_R + R_{IN}(C_G + NC_D) = \tau_R + R_{IN} C_{LF}, \qquad (8)$$

being C_{LF}=(C_G+NC_D) the equivalent capacitance of the detector for low frequencies.

Of course, good timing performance can be achieved only thanks to the fast component $V_{INF}(t)$ of the signal, whereas the slow component $V_{INS}(t)$ has poor relevance in this respect. Fig. 4 shows the results of a simulation of the components of $V_{INF}(t)$ and $V_{INS}(t)$ for two different values of R_{IN}, i.e. 10Ω and 20Ω, considering values of the parameters extracted for a SiPM with 3600 micro-cells [17], summarized in Table I.

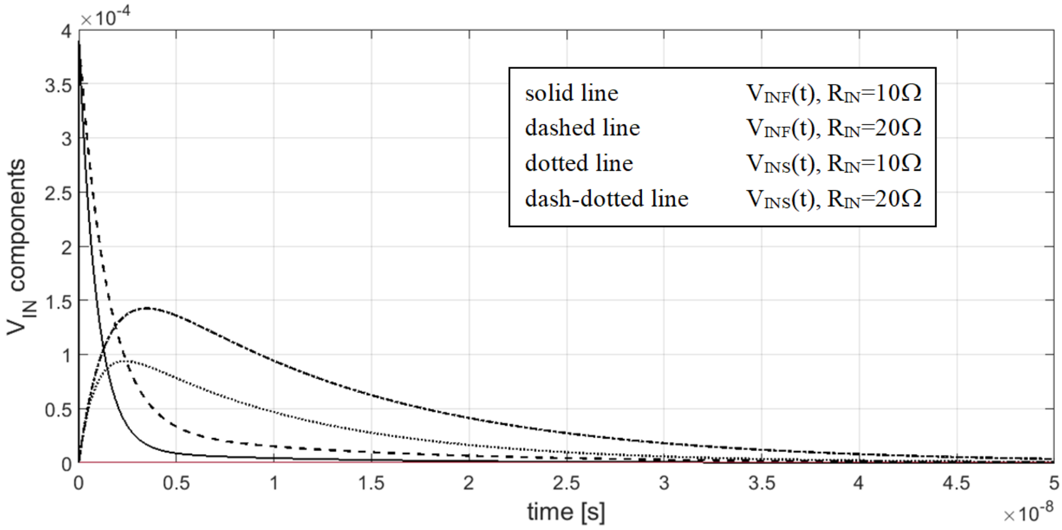

Fig. 4. Simulation of the fast and slow components of the signal $V_{IN}(t)$ for two different values of R_{IN}.

Table 1

SiPM parameters used for the SPICE simulations in Fig. 4

Parameter	Value
C_D	74fF
C_Q	30fF
R_Q	71kΩ
Q_{TOT}	160fC

In Fig. 4 the effects of the variation of R_{IN} on the fast and slow components of the signal $V_{IN}(t)$ are highlighted. First, if R_{IN} is decreased, the contribution of the slow component $V_{INS}(t)$ becomes less relevant and the fall time of the fast component $V_{INF}(t)$ gets faster. This means that the charge released by the detector is collected more quickly if the input resistance of the front-end is reduced, because of the faster discharge of C_{HF}, due to a larger discharge current flowing in R_{IN}. Moreover, the tail of the signal is apparently slower for larger values of R_{IN}. Consequently, if R_{IN} increases the rate of the event sustainable by the detection system is reduced, due to possible pile-up effects. In addition, the timing performance is affected, especially in case the time pick-off technique of choice is leading edge discrimination, since the time when the signal overcomes the threshold fluctuates, due to baseline variations. The previous considerations suggest that a very low input resistance is preferable for the front-end electronics of a SiPM detector. For instance, when the SiPM is used to read out a scintillator, low values of the input resistance are also required to limit the variation of the voltage across the detector as the photons impinge on it according to the characteristic time constant of the crystal. In fact, large voltage variations on the SiPM will cause non-linearity in the energy measurements, because the micro-cells undergoing avalanche breakdown at different times will experience appreciably different gain values.

The waveforms depicted in Fig. 4 are ideal, in that some important parasitics significantly affect, for instance, the rise time of the fast component $V_{INF}(t)$, limited only by the very fast time constants of the avalanche breakdown in the previous analysis. A remarkable contribution in this sense comes from the parasitic inductance L associated to the interconnection between the detector and the front-end electronics [18, 19]. If the simulations in Fig. 4 are repeated in presence of an inductance L=10nH, the waveforms $V_{INF}(t)$ and $V_{INS}(t)$ are modified as shown in Fig. 5.

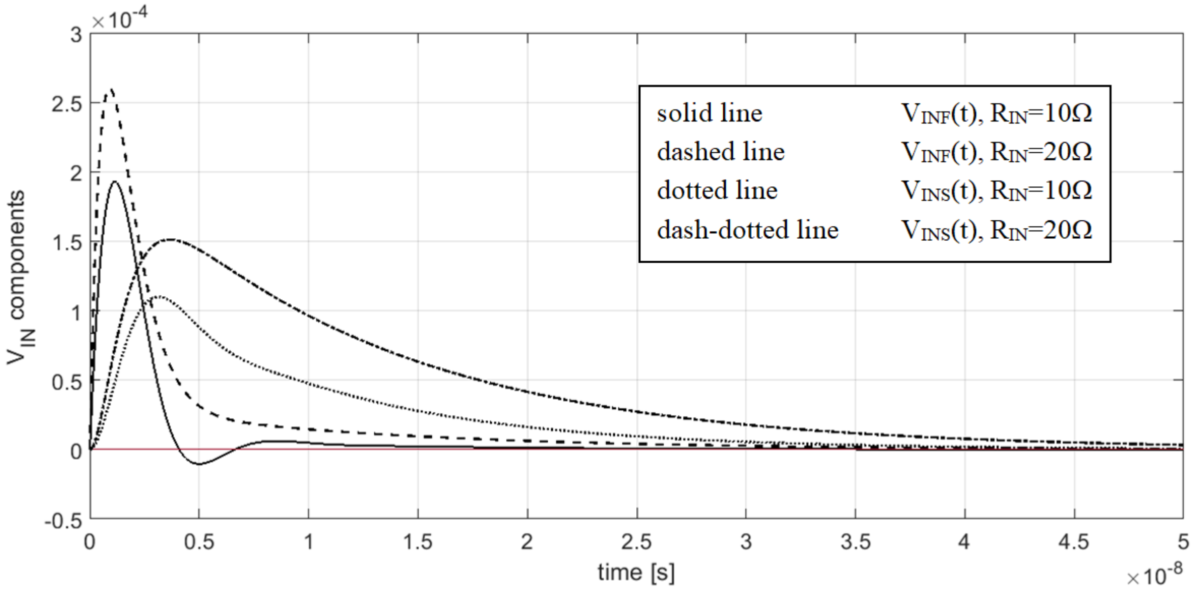

Fig. 5. Simulation of the fast and slow components of the signal $V_{IN}(t)$ for two different values of R_{IN}, in presence of a parasitic interconnection inductance L=10nH.

On the one hand, the waveforms reported in Fig. 5 show that the slope of the fast component of the voltage signal is larger when R_{IN} is increased, which is good for timing accuracy. On the other hand, this feature cannot be fully exploited because once again increasing the resistance R_{IN} causes slower collection of the charge and longer signal tail also in presence of the parasitic L, as in the ideal case, leading to the same increased pile-up probability and non-linearity problems previously quoted. When the SiPM must be coupled to the electronics through a long cable, RF circuit techniques and 50Ω impedance matching can be applied to avoid signal reflections.

If the current I_{IN} which flows into the input resistance of the preamplifier is considered, some interesting conclusions can be drawn. The behavior of the fast and the slow components of this current, $I_{INF}(t)$ and $I_{INS}(t)$ respectively, are shown in Fig. 6, obtained with simulations carried out in the same conditions of Fig. 5. Apparently, lower values of the input resistance correspond to both larger values of the slope of the fast component $I_{INF}(t)$ and shorter tails for both components. This suggests that a very effective read-out approach can be based on a current mode preamplifier which reads the current pulse generated by the SiPM at very low impedance, discharging quickly the large equivalent capacitance of the detector C_{HF}, and reproduces this current on a high impedance node, so that it can be further processed for the extraction of the time and energy information. This is a very common approach for the front-end electronics used for SiPM and different implementations of this scheme have been applied in several realizations of read-out circuits.

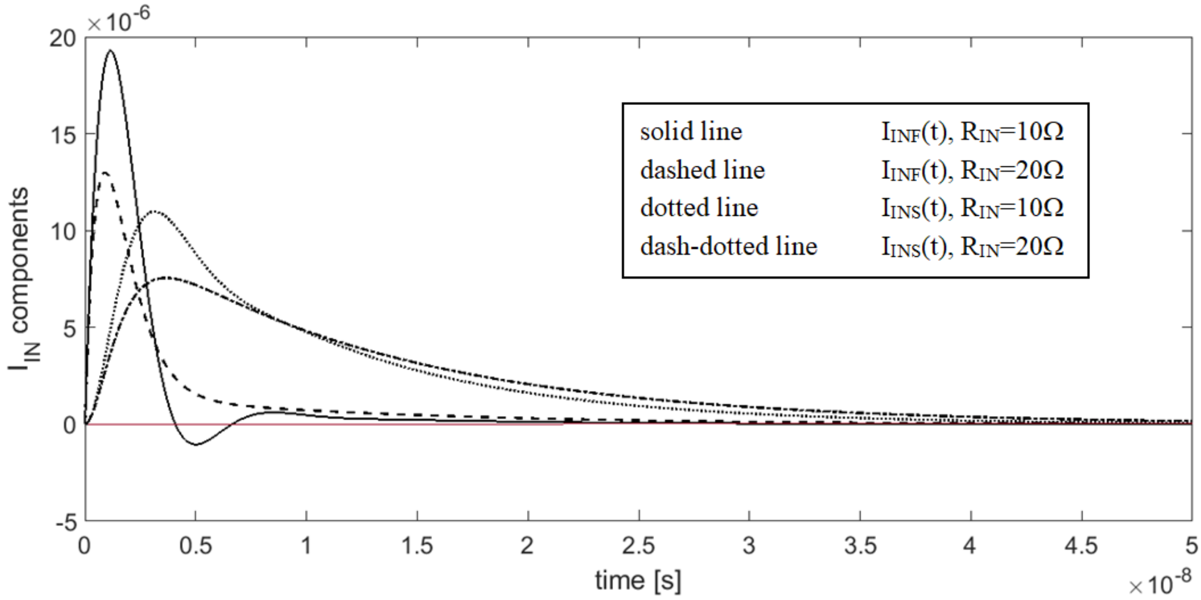

Fig. 6. Simulation of the fast and slow components of the current $I_{IN}(t)$ for two different values of R_{IN}, in presence of a parasitic interconnection inductance L=10nH.

3. Voltage mode readout approach

In any case, according to eq. (1) in order to achieve good timing performance, the preamplifier must be able to preserve as much as possible the fast rise time of the input signal at its output, thus it must feature large bandwidth. In case a voltage amplifier is used to read-out the detector, since R_{IN}, as discussed above, cannot be large, the amplifier should also have sufficient gain, to reproduce an output signal of suitable amplitude, so that it can be conveniently processed by the next blocks, e.g. an integrator and a comparator for energy or time measurements respectively, as schematically depicted in Fig. 7. Such specifications, i.e. large gain-bandwidth product, are difficult to be achieved without large power consumptions, making this approach not effective in applications where very low levels of lights must be detected, timing accuracy is a relevant specification and the number of readout channels is large. On the other hand, when the dynamic range of the input signal is large, thus low voltage gain values are needed, and the specifications on the time accuracy are relaxed, the voltage mode approach can be conveniently applied. As far as the noise performance of the circuit in Fig. 7 are concerned, the total equivalent input voltage noise of the voltage amplifier, which is typically associated to a common source input transistor, is directly summed to the voltage across R_{IN}, causing limitations in the Signal to Noise Ratio (SNR) and in the timing resolution that is possible to achieve, according to (1).

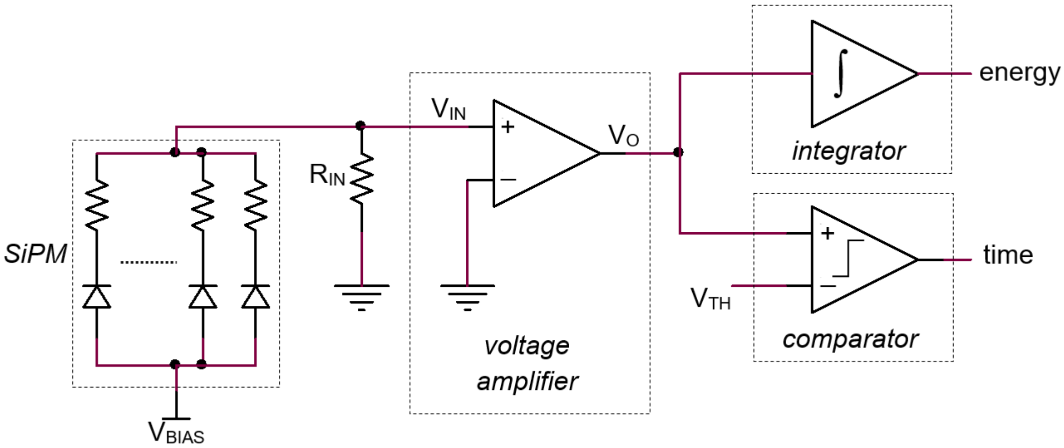

Fig. 7. SiPM readout with voltage mode approach.

In the following, some examples of readout ASICs for SiPM detectors based on the voltage mode approach are presented. SPIROC [20] and EASIROC [21], designed in 0.35μm technology, exploit an external 50Ω input resistance, DC decoupled, and an inverting voltage preamplifier to convert into a voltage and amplify the current pulse of the SiPM. The preamplifier has the classic inverting feedback structure and the gain is set by means of the capacitors C_S and C_F, as illustrated in Fig. 8 (SPIROC). Two different values of the gain can be chosen for the preamplifier, i.e. 1 and 10.

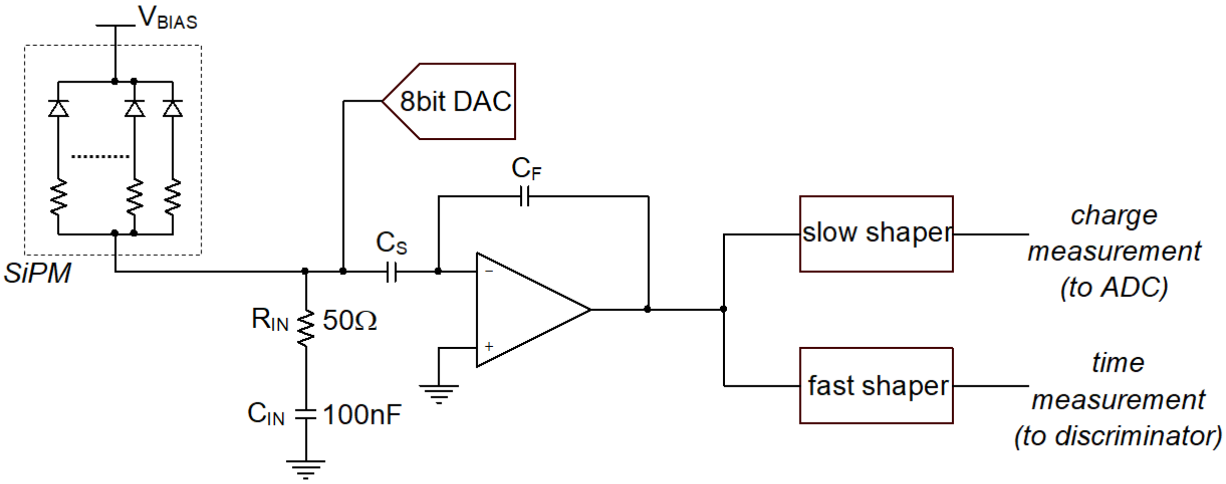

Fig. 8. Structure of the analog channel of the ASIC SPIROC.

An 8 bit DAC is added at the input of the preamplifier to allow fine adjustments of the bias voltage of the detector, which is DC coupled to the electronics. The CRRC^2 slow shaper integrates the output signal of the voltage preamplifier with a selectable shaping time and, in parallel, a bipolar fast shaper, with shaping time of 15ns, is used to drive the fast voltage discriminator which generates the trigger signal.

The dynamic range of the charge measurements for both ASICs is 320fC, which corresponds to 2000 micro-cells of a SiPM with gain 10^6. The time resolution obtained is about 1ns rms for SPIROC, which exploits power-pulsing techniques to reduce power consumption down to 25μW/channel, and is better for EASIROC, being lower than 0.3ns rms for discriminator threshold set to 3pe (i.e. 0.48pC) and injected charges higher than 0.64pC, with a power consumption of 4.84 mW/channel [22]. For both ASICs the threshold can be set down to 50fC, making possible the detection of single photons. These circuits are not intended for applications with severe requirements in terms of timing accuracy, such as ToF-PET, but are conveniently used in energy measurements for physics experiments, for instance in calorimeters.

Considering the same ASIC family, in order to improve timing performance the PETIROC circuit [23] has been designed in a SiGe technology, which offers HBT devices with f_t > 60GHz and allows achieving very large bandwidth with limited power consumption. In this ASIC, in parallel with the inverting input stage followed by the slow shaper used for the energy measurement, the signal path for the time measurements exploits an RF common emitter preamplifier with a 10GHz gain-bandwidth product, followed by a fast voltage discriminator. The measured jitter of the trigger signal generated with the front-end coupled to a 1x1mm^2 Hamamatsu MPPC, using a fast laser to inject 15 photoelectrons and setting the threshold at 1photoelectron, is 46ps, with a power consumption of 3.6mW/channel, excluding the output buffer used to observe the signal.

A further example of voltage mode preamplifier for SiPM detectors is the front-end of the first version of the ASIC PETA [24] designed as an evolution of a previous circuit intended for photomultiplier tubes [25]. In this circuit, the fast signal path used for time measurements is based on a fully differential voltage amplifier composed by the cascade of 5 low-gain, high speed differential gain stages with diode loads, to maximize the bandwidth [26] (see Fig. 9). The fully differential structure guarantees immunity from common mode noise and is less sensitive to ground bounce and noise coming from the switching of digital parts, but more off-chip passive components are needed (AC coupling) and the input pad number of the ASIC is doubled. The preamplifier reads out the signal across an internal, adjustable termination resistance with nominal value of 50Ω. The gain of the preamplifier is 20 and its maximum bandwidth is 900MHz, which can be limited in two steps by means of a low pass filter. A slow common mode feedback block is also used to stabilize the common mode of the preamplifier and a differential current mode logic (DCL) buffer, AC coupled to the preamplifier, acts as a fast discriminator.

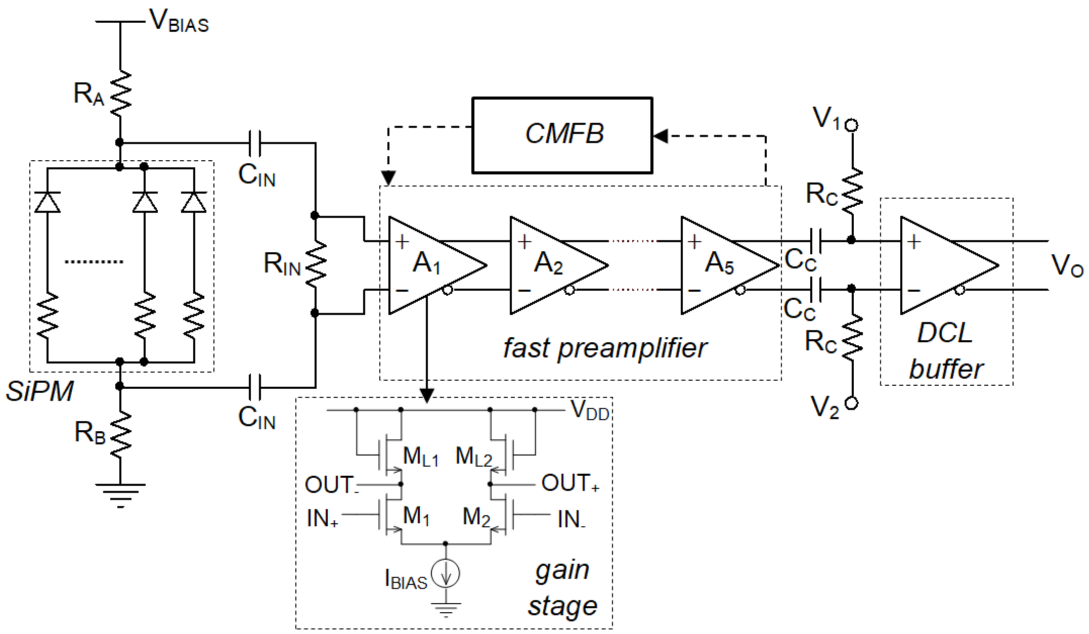

Fig. 9. Fast path of the ASIC PETA.

The PETA3 version of the ASIC provides very interesting results in terms of time resolution: the Coincidence Resolving Time (CRT) obtained by coupling two channels of the ASIC to 3x3mm^2 FBK SiPMs, used to read out 3x3x5mm^3 LYSO scintillators exposed to 511keV γ-rays, is 190ps FWHM [27], but the power consumption is a remarkable 32mW/channel.

Always using a voltage mode approach, excellent timing accuracy can also be obtained with front-ends based on commercial low-noise RF amplifiers intended for telecommunication and wireless applications, which exhibit 50Ω input and output impedance and allow impedance matching, as mentioned in Section 2. For instance, in [28] several experiments have been carried out with a monolithic RF amplifier with 2GHz bandwidth, noise-figure of about 3.7 dB at 1 GHz and gain of 12 dB (Minicircuits Mar-3SM+) coupled to a 3x3mm^2 Hamamatsu MPPC and, using 2×2×3mm^3 LSO scintillators, a very good CRT of about 125ps has been achieved. However, also in this case the power dissipation is huge, about 400mW, and systems with a large number of channels are unpractical.

4. Current mode readout approach

As pointed out in the conclusions of Section 2, current mode preamplifiers are commonly used to read out SiPM detectors and also implementations with discrete components have been proposed in the literature [19]. Fig. 10 shows the basic principle of this approach: a current buffer with very low input impedance is coupled to the detector and exploits the advantages of small R_{IN} values, illustrated in Section 2.

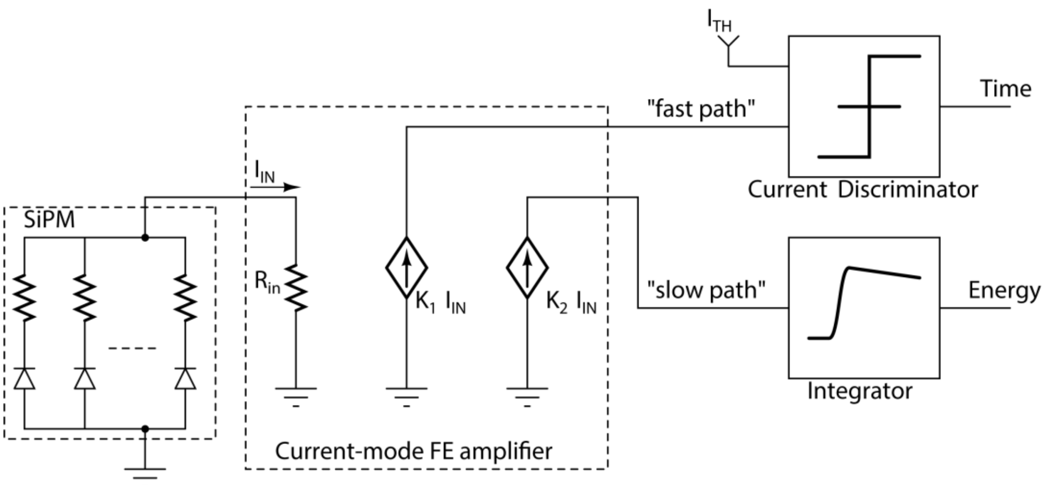

Fig. 10. Basic structure of a current mode analog channel for SiPM.

The output signal of the buffer is a high impedance replica of the current pulse generated by the detector that can be easily reproduced with different scaling factors (K_1 and K_2 in Fig. 10) and used to establish different “fast” and “slow” signal paths, optimized for charge or time measurements [29]. Typically, large bandwidths are easier to be achieved with current mode amplifiers, because of the absence of high impedance nodes, thus the output signal can follow the very fast leading edge of the current pulse generated by a SiPM, resulting in good performance in terms of time resolution.

Several implementations of the current mode preamplifier have been proposed in the past. The simplest one is based on a common gate current follower and one of the most relevant realization of this approach is the front-end of the NINO ASIC [8,30], schematically depicted in Fig. 11.

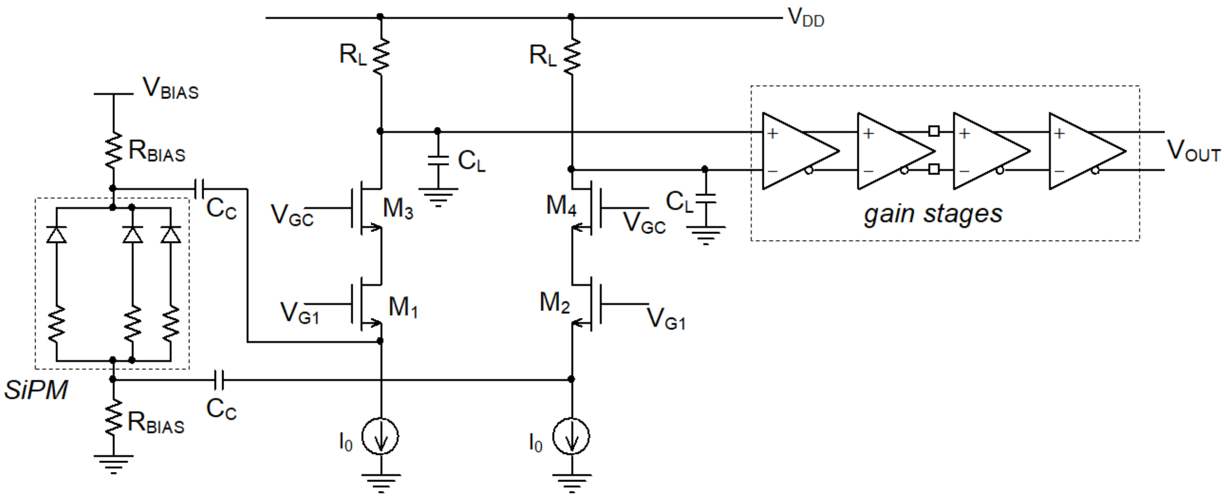

Fig. 11. Analog channel of the ASIC NINO.

A fully differential configuration is employed to increase the immunity of the circuit against power supply and ground noises. Cascode transistors M_3 and M_4 are used to decouple the drains of the input common gate MOSFETs M_1 and M_2 from the output nodes and to increase the output resistance of the current buffer. The current signal of the detector is converted into a voltage by means of the load resistors R_L, which form the dominant time constant of the circuit (about 760ps) with the load capacitance C_L [31]. The input resistance of the stage is set by the transconductance g_m=50mA/V of the common gate MOSFETs, corresponding to a total differential resistance seen by the SiPM of 40Ω. The open loop configuration of the front-end makes the circuit very fast and avoids any stability concerns. Considering a 3x3mm^2 Hamamatsu MPPC with an overvoltage of 1.5V, the rise time of the preamplifier output signal is 1.5ns for a single fired micro-cell and the estimated time jitter, with a signal-to-noise ratio of 15, is 100ps rms [8]. The front-end is followed by four differential gain stages, each with a voltage gain of 6 and 500MHz bandwidth, which form the discriminator, and the power consumption of the preamp+discriminator is about 20mW [32]. Recent measurements carried out by coupling the detector to a Hamamatsu S13360-3050CS SiPM biased at 62V achieve a Single Photon Time Resolution (SPTR) of 64ps rms [33].

A similar configuration is adopted also by the circuit STiC3 [34], which also uses a differential front-end based on an open-loop input common gate stage and a load resistor to form a voltage signal that is compared to a threshold by means of a fast comparator for the generation of the trigger signal. In the last version of the circuit, the load resistor has been implemented by means of a diode connected MOSFET [35] as depicted in Fig. 12 (only one branch of the differential structure). The capacitance C_C allows keeping the value of the input resistance R_{IN} close to $1/g_{mIN}$ also at high frequencies, mitigating the effects of the output resistance R_{DAC} of the DAC used to fine tune the bias voltage of the SiPM. The results in terms of SPTR are very similar to the ones reported for the NINO ASIC: using the same detector (Hamamatsu S13360-3050CS) an SPTR of 67.1ps rms has been achieved, with a total power consumption of 25mW/channel [36].

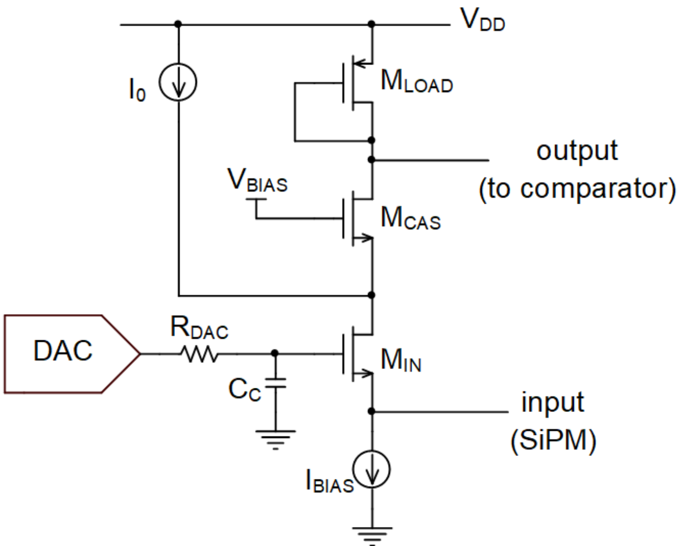

Fig. 12. Front-end of the ASIC STiC (only one branch of the differential current mode preamplifier).

Considering the noise performance of these preamplifiers, based on a common gate configuration biased by a current source, the contribution of the input transistor to the total noise at the output node of the preamplifier appears only at high frequencies, where the equivalent capacitance of the detector short-circuits to ground the source of the input MOSFET. At low frequencies, only the noise of the bias current source (I_0 in Fig. 11 and I_{BIAS} in Fig. 12) can reach the output node through the common gate transistor, but this contribution can be made negligible by reducing the transconductance of the MOSFET which provides the bias current. As a result, in general the common gate stage exhibits better noise performance as compared to a common source preamplifier, very often used in the voltage mode readout approach. This advantage of the current mode readout in terms of noise, which translates in better timing performance due to eq. (1), decreases when large detectors, characterized by large equivalent capacitance, are used. On the other hand, the output dynamic range of the common gate amplifier is reduced by the presence of the bias current source, whereas this limitation does not apply to a common source stage, thus, in principle, we can conclude that the current mode approach is worse than the voltage mode in terms of dynamic range.

Feedback is often employed in order to decrease the input resistance of the current mode preamplifier while saving power. One of the most used topologies is the regulated common gate transimpedance amplifier, schematically depicted in Fig. 13. Here, the open-loop input resistance of the preamplifier $1/g_{m1}$ is decreased by a factor equal to the loop gain of the applied feedback $g_{m2}R_2$, thus there are more degrees of freedom, with respect to the simple common gate solution, that can be exploited to find a good compromise solution among low R_{IN}, power consumption and noise. Also stability is of concern in this kind of circuit and one of the main design guidelines is limiting the Q factor of the complex conjugate poles of the circuit to values less than 1, to control the damped oscillatory behavior of its impulse response. Detailed circuit analysis can be found in [37] and shows that the output noise is dominated by the contribution of the noise current of M_2, which can be reduced by increasing g_{m2} with respect to g_{m1}, thus ascribing to the feedback the task of reducing the input resistance of the preamplifier.

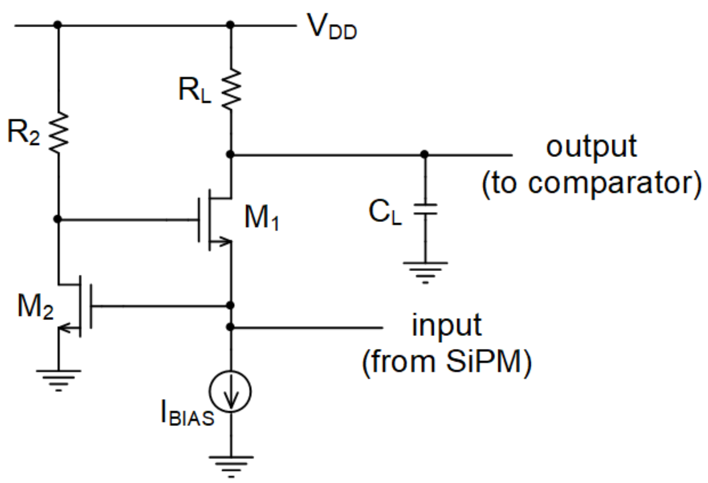

Fig. 13. Regulated common gate as a front-end for SiPM.

An example of read out ASIC intended for SiPM detectors and based on the regulated common gate approach is the TOFPET2 circuit [38]. The front-end can be coupled to both n-on-p and p-on-n devices: Fig. 14 shows the basic circuit used for one of the two SiPM polarities. The load of the regulated common gate is the diode connected PMOSFET M_3, which is AC coupled to a common source amplifier with passive load, to convert the current pulse of the detector into the input voltage of the discriminator. The operating point of the common source M_4 is settled by means of the voltage reference formed by I_{REF} and M_{REF}, connected to the gate of M_4 via a large resistor, in the order of GΩ, realized by the back-to-back cut-off MOSFETS M_5 and M_6. The same arrangement, basically consisting in an AC coupled current mirror, is replicated to obtain different signal paths with suitable scaling factors, to be used for energy and time measurements. As an example of the timing performance of the TOFPET2 ASIC, an SPTR of 95 ps rms has been measured using a fast laser source and one of the SiPM of the Hamamatsu 4x4 array HPK S13361-3050AE-04, biased at 7.5V overvoltage [39]. The overall power consumption of the ASIC is less than 10mW per channel.

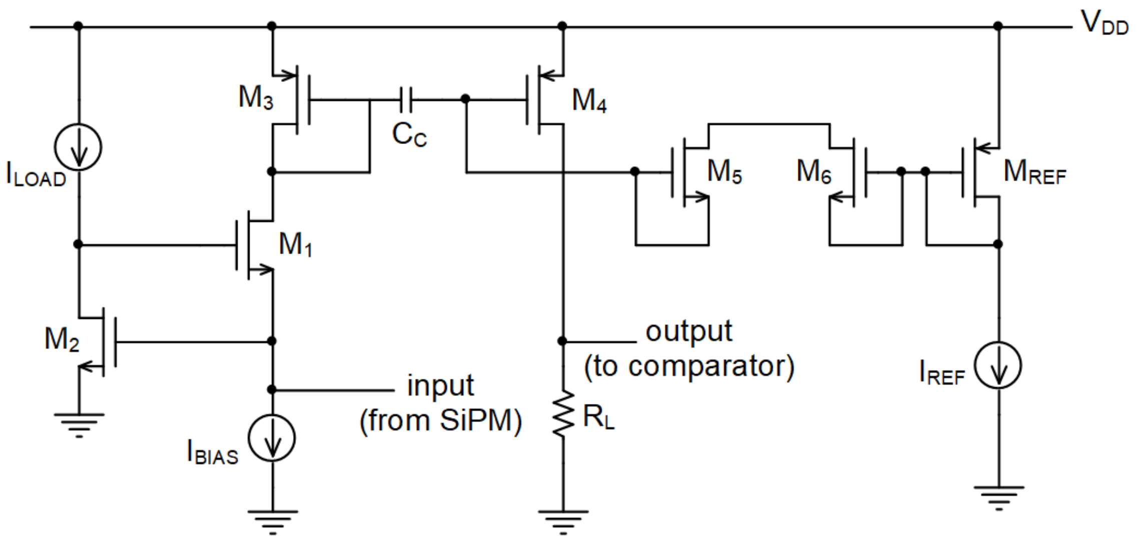

Fig. 14. The regulated common gate preamplifier of the ASIC TOFPET2.

A slightly different implementation of the regulated common gate that can be found in several realizations is the one depicted in Fig. 15 [40-43].

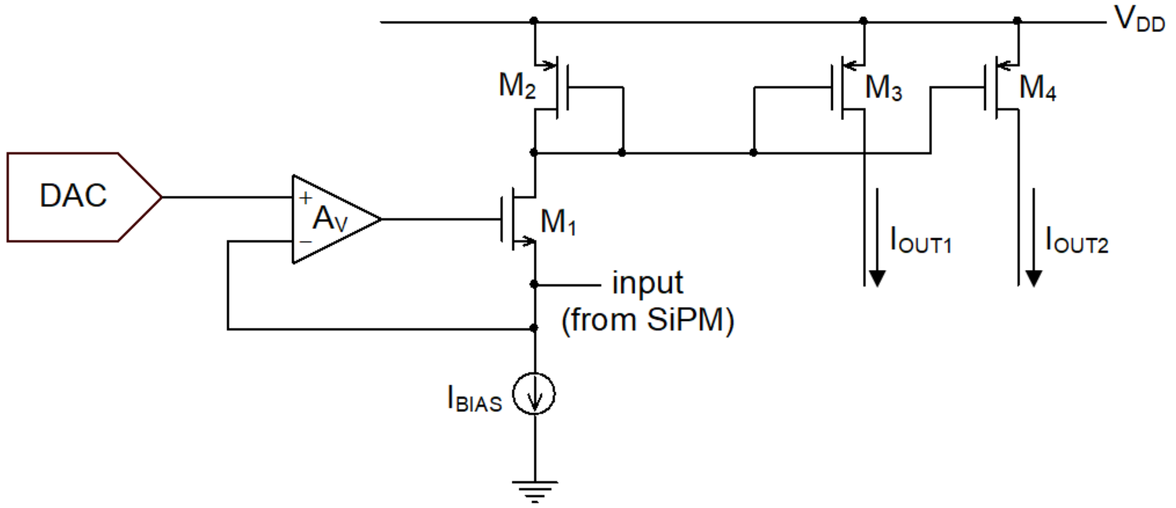

Fig. 15. Regulated common gate front-end with gain boosting realized by means of a differential amplifier.

Here the input resistance of the preamplifier is given by $R_{IN}=1/g_{m1}A_V$, where A_V is the gain of the differential gain boosting stage in the regulation feedback loop. Also in this case the stability issue must be carefully taken into account in the design and the gain-bandwidth product of the differential amplifier must be large, to guarantee low values of the input impedance of the preamplifier also at high frequencies. The main advantage associated to the structure of Fig. 15 is the possibility of fine tuning the bias voltage of the SiPM by exploiting the virtual short circuit at the terminals of the differential amplifier, using a DAC.

As already mentioned, in several cases two different signal paths are established and optimized to carry out in effective way both time and energy measurements. In the architectures considered up to now, these paths are formed after the front-end stage, for instance exploiting current mirrors. In [44] a different approach is proposed: the current pulse of the SiPM is split into two fractions directly at the input of the preamplifier, by exploiting two matched HBTs, available in the SiGe technology used to design the circuit, suitable scaled of a factor M and arranged in a regulated common base configuration, as shown in Fig. 16. The same configuration has been also used for the input stage in [45], using MOSFETs instead of HBTs.

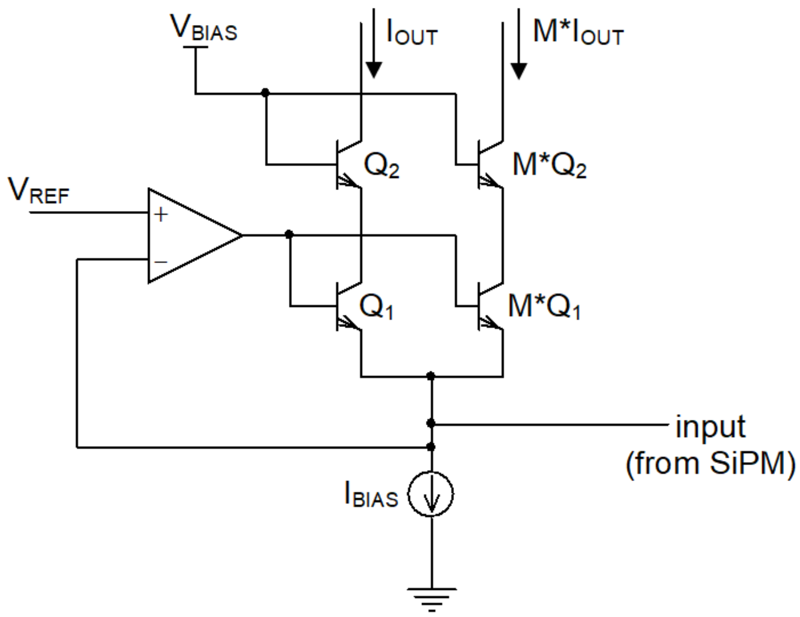

Fig. 16. Two signal paths formed directly al the input of the preamplifier my means of matched HBTs arranged in a regulated common base configuration.

Several further examples of current mode front-ends for SiPM that exploit feedback in different ways to decrease the input resistance of the circuit can be found in the literature [45-50], thus we can conclude that the current mode approach is the most common solution used for the readout of this kind of detectors, especially in applications where timing resolution is of interest, for instance ToF-PET.

5. Energy measurements: main circuit solutions

As discussed in the previous sections, the very front-end of an electronic channel intended for SiPMs must preserve as much as possible the favourable features of the detector and provides an output signal proportional to the current pulse of the detector. In order to extract the information about the charge associated to the signal, proportional to the energy of the detected event, the most straightforward approach is integration of the signal itself. In case a voltage mode preamplifier has been used, integration can be performed by means of a slow shaper cascaded to the front-end. The shaper can be implemented with a passive RC network or, more frequently, with an active filter. For instance, in the ROC ASIC family, a CRRC^2 shaper has been cascaded to the inverting voltage preamplifier in the slow path of the signal. The shaping time is variable between 25ns and 200ns, to accommodate the requirements of different applications [51]. Fig. 17 shows an example of the structure of the slow shaper with programmable shaping time [52].

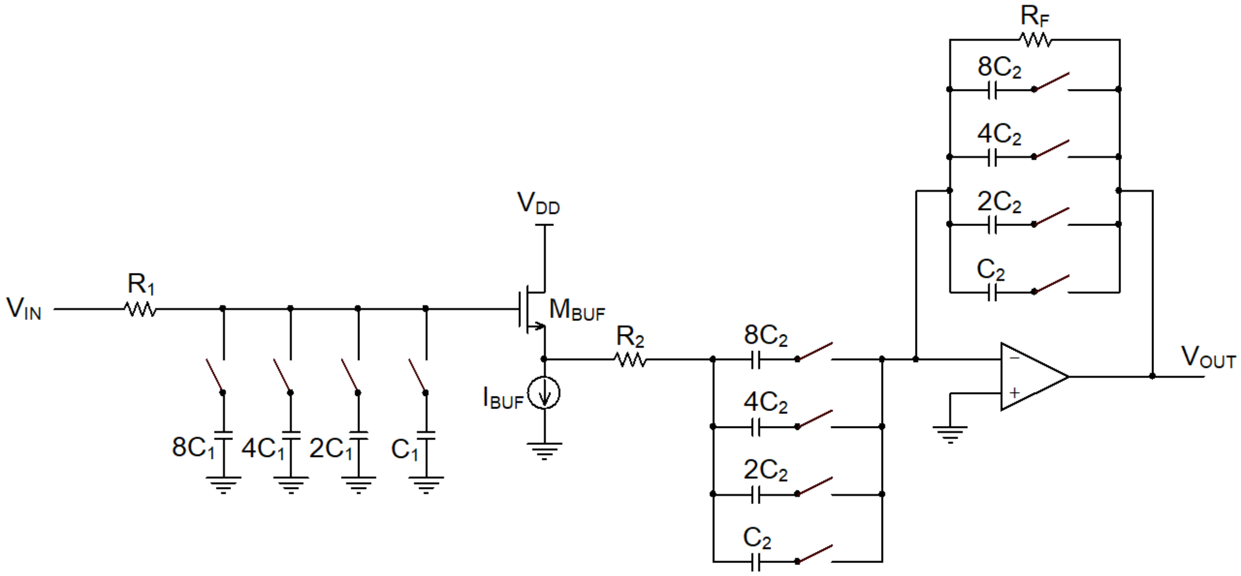

Fig. 17. Configuration of the CRRC^2 slow shaper used to integrate the output signal of the SPIROC preamplifier.

In the circuit of Fig. 17, the first pole is realized by means of a passive low-pass RC circuit and the rest of the transfer function of the shaper has been implemented using an active band-pass filter, decoupled from the passive RC network by means of a voltage buffer.

For instance, in PET applications the signal in response to a 511keV event is the result of the convolution between the single-photon response of the SiPM, characterized by its long tail, and the function of time which describes the photon emission rate of the scintillator, characterized by its time constant. The peaking time should be long enough to integrate as much as possible the resulting signal, for accurate evaluation of the energy, and typical values in this case are around 200ns, for LYSO or LSO scintillators. Of course long shaping times limit the event rate that can be sustained by the channel.

In case a current mode approach is used for the front-end, integration of the current signal of the fast path, as in Fig. 9, is a straightforward task and can be carried out by means of a passive RC network [45,47] or using a CSA [29]. These two solutions are illustrated in Fig. 18, which represents the front-end and the integrator of the ASIC Klaus (Fig. 18a) [47] and BASIC (Fig. 18b) [29]. In Fig. 18 the different approaches applied in these two cases for the application of feedback to the input current buffer can be distinguished.

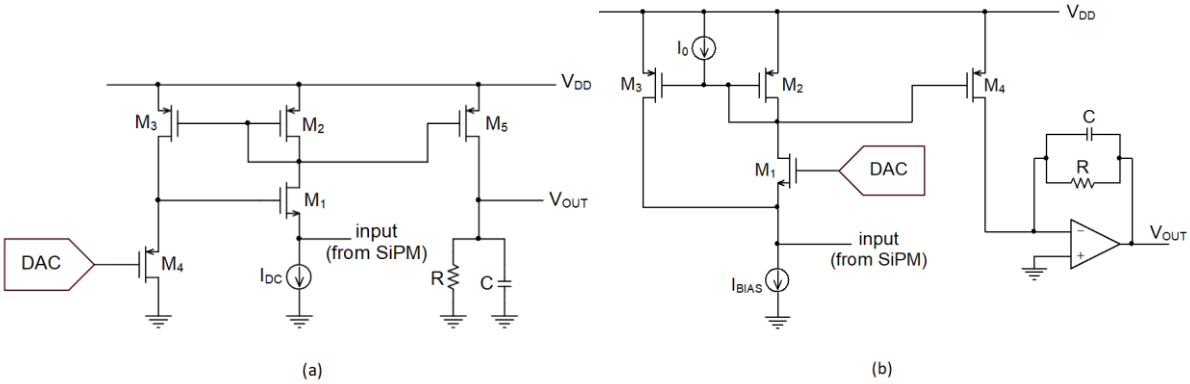

Fig. 18. Front-end and slow path of the analog channels of the ASICs Klaus (a) and BASIC (b).

In both voltage and current mode, the peak of the integrator output is the signature of the energy to be measured, thus it must be sampled and made available for further processing, for instance analog to digital conversion. This can be accomplished by using an external signal to sample the integrator output voltage at the peaking time of the shaper, generated by means of a delay after the fast discriminator has fired. This sampling signal can be used to store the integrator output in an analog memory realized with a switched capacitor array properly addressed, as in the ROC family [20,21,23]. As an alternative, a peak stretcher circuit can be used to detect and store the peak voltage of the integrator [29,48]. This circuit is often realized according to the structure proposed in [53] and schematically represented in Fig. 19. The current mirror M_1-M_2 works as a rectifying element in a feedback loop and the circuit can be easily configured so that, while waiting for a valid signal, the voltage on the capacitor C_P follows the input voltage ($\phi_1=1$; $\phi_2=1$). As soon as a valid event has been detected, the current I_{BIAS} is switched off (ϕ1=1; ϕ_2=0) and the C_P cannot be discharged, thus the voltage across C_P tracks the peak of the input voltage. Last, when the peak is reached, the OPAMP goes into positive saturation, the current mirror is switched off and the circuit is reconfigured as an analog memory (ϕ1=0; ϕ_2=0), presenting at the output the voltage across C_P.

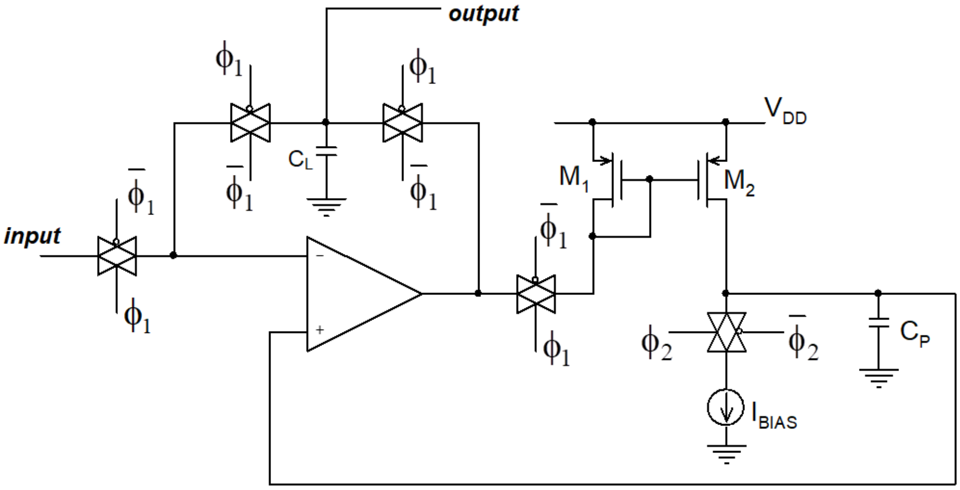

Fig. 19. Peak detection circuit.

Another approach consists in integrating the output signal of the front-end in a time window of suitable duration, often programmable, started when the fast discriminator fires [24,38,54]. In the ASIC TOFPET2 [38], which features a front-end based on a current mode approach as described in Section 4, the output current of the front-end is switched on a capacitor array, via current mirrors, to integrate the current pulse when the fast discriminator fires (S_1 closed, S_2 open in Fig. 20).

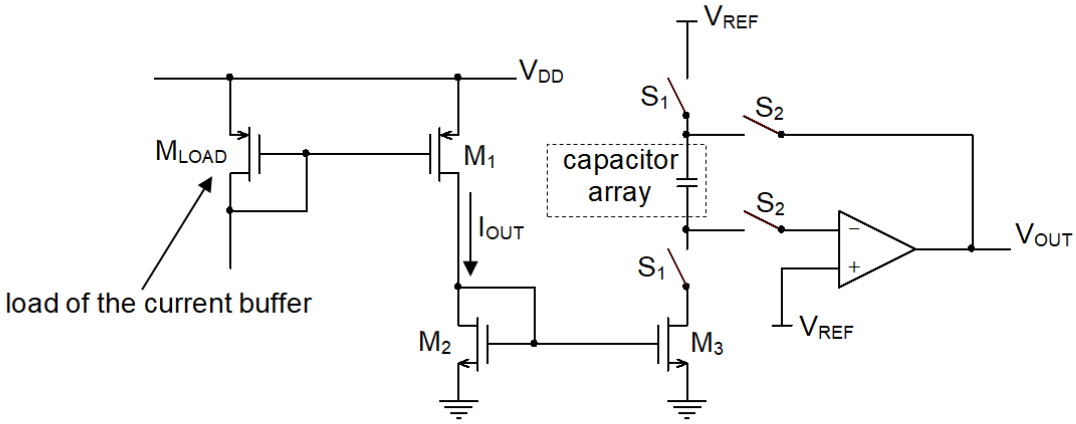

Fig. 20. Slow path of the ASIC TOFPET2.

At the expiration of the integration time window, the capacitor array is switched on a differential output buffer (S_1 open, S_2 closed).

Instead, in [24] the front-end output is a voltage pulse, which is converted into a current and integrated in the chosen time window using a classic CSA without resistive feedback, as illustrated in Fig. 21. A slow feedback loop around the integrator, based on an Operational Transconductance Amplifier (OTA), is used to compensate the DC component of the input voltage. This loop is opened as soon as the Start signal, provided by the fast discriminator, is activated, so that the output current of the OTA stays constant and only the AC component of the input voltage is integrated. The integration time window is closed by the Stop signal, generated by a timer circuit.

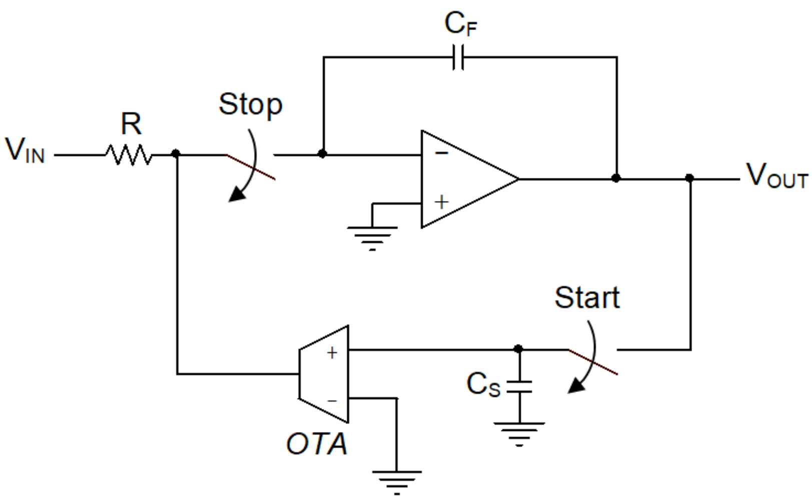

Fig. 21. Integrator of the ASIC PETA.

Often, the integrator is followed by an ADC and the energy information is made available in digital format [20,38,55], so that it is easily transferred to the external electronics for further processing via fast digital links.
All the approaches discussed so far guarantee very good linearity in energy measurements, which is needed in applications such as gamma spectroscopy or calorimetry.

When linearity is not of particular concern, one of the most common techniques for evaluating the energy of the detected events is Time over Threshold (ToT), which consists in measuring the duration of the preamplifier output pulse, associated to the charge generated by the detector. Usually, the pulse duration is evaluated as the time interval in which the pulse amplitude is comprised between two different thresholds, as depicted in principle in Fig. 22: the first one, V_{TH1}, is the same very low threshold of the fast discriminator, used for the measurement of the event occurrence time, whereas the second one, V_{TH2}, is higher, in order to improve the energy resolution which can be achieved.

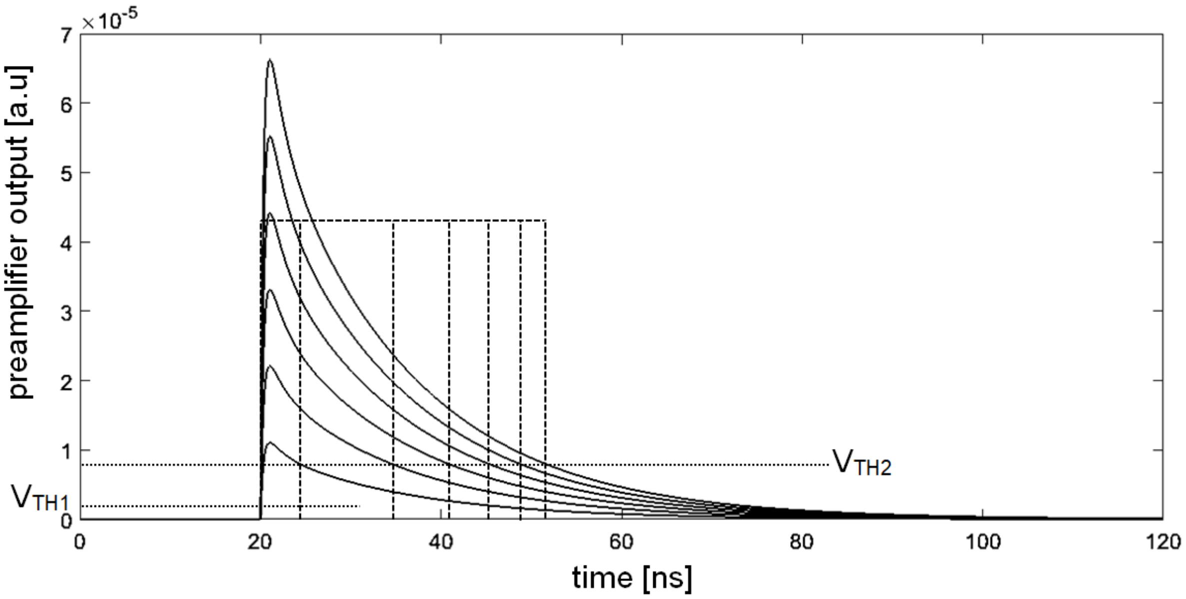

Fig. 22. Time over Threshold (ToT) technique for energy measurements.

In this way, also the energy measurements are carried out by means of time measurements and, for instance, a Time to Digital Converter (TDC) can be exploited for both time and energy evaluation, resulting in more compact electronics and power consumption saving. In any case the relationship between the duration of the pulse obtained with this technique and the charge generated by the detector is strongly non-linear, as Fig. 22

clearly shows. For instance, in [8] a differential passive filter has been interposed between the SiPM terminals and the input of the NINO preamplifier, in order to shape the waveform of the current pulse, so as to mitigate non-linearity of the ToT technique and extend the dynamic range of the charge that can be processed. In general, ToT can be conveniently exploited in applications that do not require much accuracy in the energy measurements, in order to optimize the requirements of the electronics in terms of compactness and power consumption. For instance, this technique is applied in PET applications, for identification of the photo-peak and correction of the time-walk in time measurements [32,42].

To improve the linearity of the ToT technique for charge measurements, another approach can be exploited: the output pulse of the front-end, converted into a current in case a voltage mode preamplifier is used, is integrated within a time window of suitable duration TW, using a capacitor. Then, the integration capacitor is discharged with a constant current down to the threshold, obtaining a ramp signal with duration proportional to the total integrated charge. This technique, illustrated in Fig. 23, has been applied, for instance, in [46,56,57] and makes possible the exploitation of a TDC for energy measurements also in applications based on a continuous crystal read-out by an array of SiPMs, in which the energy resolution achieved with a simple ToT solution is not sufficient, due to the large statistic dispersion of the long tail of the SiPM signal.

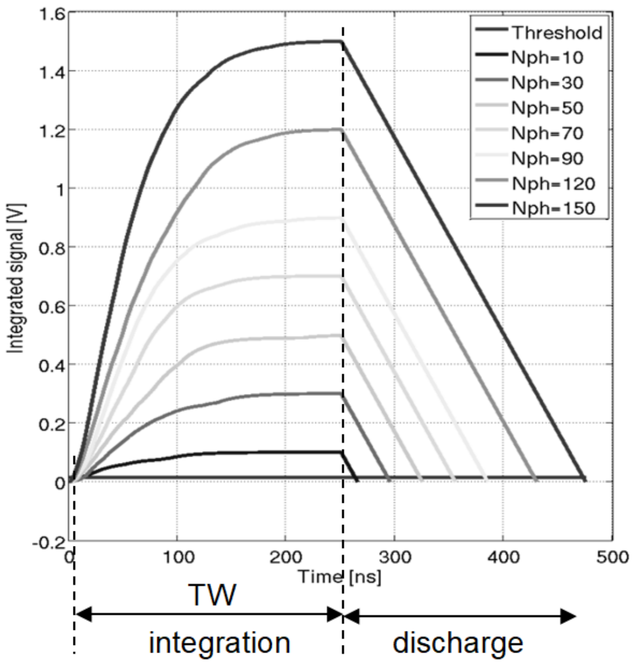

Fig. 23. Linearized Time over Threshold (ToT) technique for energy measurements: fixed integration time TW and variable discharge time for signals corresponding to increasing number of photoelectrons Nph.

In [35] a similar technique exploits the saturation of the input common gate stage, which turns off when the amplitude of the detector current increases, to integrate the charge on the same capacitance of the detector. Then this capacitance is discharged by the bias current of the input stage.

As a general observation concerning the accuracy of energy measurements with the ToT, the slope of the slow falling edge of the SiPM pulse is very small, especially when the number of photons to be detected is low. According to eq. (1), this affects the time jitter of the output signal of the discriminator and makes problematic the recourse to the ToT techniques when the application requires the identification of the number of photons and single photon spectrum is needed.

6. Time pick off solutions

As already pointed out in the introduction, LED is the favourite time pick-off method with SiPMs and in several read out circuits, based on both voltage and current mode, a fast voltage comparator is used to form an output signal with a very sharp transition when the detector pulse overcomes the threshold. This trigger signal marks the arrival of the event and can be time-stamped by means of a Time to Digital Converter (TDC). In some cases [8,24], as already shown, the discriminator is composed by the cascade of low gain, large bandwidth voltage amplifiers, with overall gain sufficient to generate a fast, full swing output pulse in response to the signal generated by a single micro-cell of the SiPM undergoing avalanche breakdown. Hysteresis can be added to the discriminator by means of a small amount of positive feedback, to avoid undesired output transitions due to the noise [8].

In current mode front-end circuits, a current discriminator is often used in the fast signal path to compare the output current pulse of the front-end to a threshold current, thus no further current to voltage conversion is needed, as in case a voltage discriminator is employed. A common structure for the fast discriminator is the one proposed in [58], schematically represented in Fig. 24. In DC, the PMOS M_1 is ON and carries the difference between the threshold I_{TH} and the output current of the front-end I_{OUT}, so that the output voltage of the inverting amplifier is low. As soon as I_{OUT} overcomes the threshold, due to the arrival of a valid event, M_1 turns off and the

NMOS M_2 turns on, thus the output of the amplifier makes a fast positive transition, sensed by the cascaded inverters. Examples of readout circuits which exploit this current comparator structure are, for instance, [29,40,49,59,60].

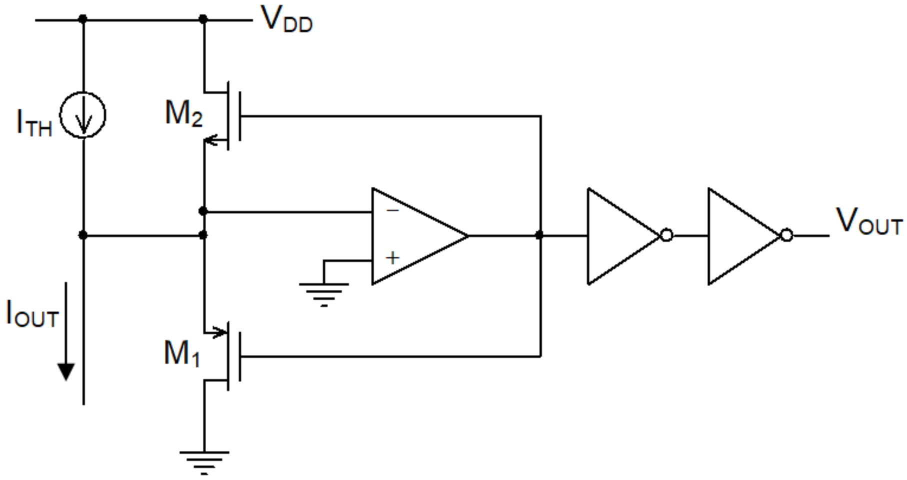

Fig. 24. Structure of a current discriminator.

Time walk, i.e. the dependence of the time when the threshold is overcome on the amplitude of the signal, is a typical issue of the LED time pick-off technique, and the classic circuit solution for this problem is Constant Fraction Discrimination (CFD) [9]. However, very few examples of application of this technique to SiPM readout exist. For instance, in [61] a comparison is reported between the results obtained in terms of timing accuracy by using LED and CFD applied to the output of the same current mode front-end. When the front-end is coupled to a 3x3mm^2 Hamamatsu MPPC, used to readout a 3x3x15mm^3 LFS crystal, a time resolution of 479ps and 712ps FWHM have been achieved with LED and CFD respectively. Non-linearity of the current differentiation stage used in the CFD circuit and large variability of the rise time of the SiPM signal are identified as the main causes of the worse results obtained with CFD. Moreover, in relevant applications, such as PET, only the events around the photo-peak are of interest, thus the amplitude variability is not the main cause of errors in time measurements.

Another interesting method proposed to improve time resolution in SiPM readout systems used for PET is the Differential Leading Edge Discrimination (DLED) technique [62]. This method is useful to get rid of the baseline fluctuations due to the long tail of SiPM dark pulses, which causes errors in the evaluation of the time when a valid event overcomes the discriminator threshold. The tail of the SiPM signal, characterized by the slow time constant τ_S, is compensated by means of a linear filter introduced in the fast signal path, which adds a zero with the same time constant to the overall transfer function of the front-end. A simple example of this pole-zero cancellation filter is reported in Fig. 25. This results in a fast return to zero of the dark pulses generated by the detector, without affecting the rise time of the response to the single photon. A downside of this method is that the differentiation introduced by the filter tends to increase the contribution of the electronic noise in eq. (1), thus the DLED technique cannot be used when this effect becomes relevant. Moreover the time constant of the zero must be adjustable if the readout circuit is intended to be coupled to different kinds of SiPM.

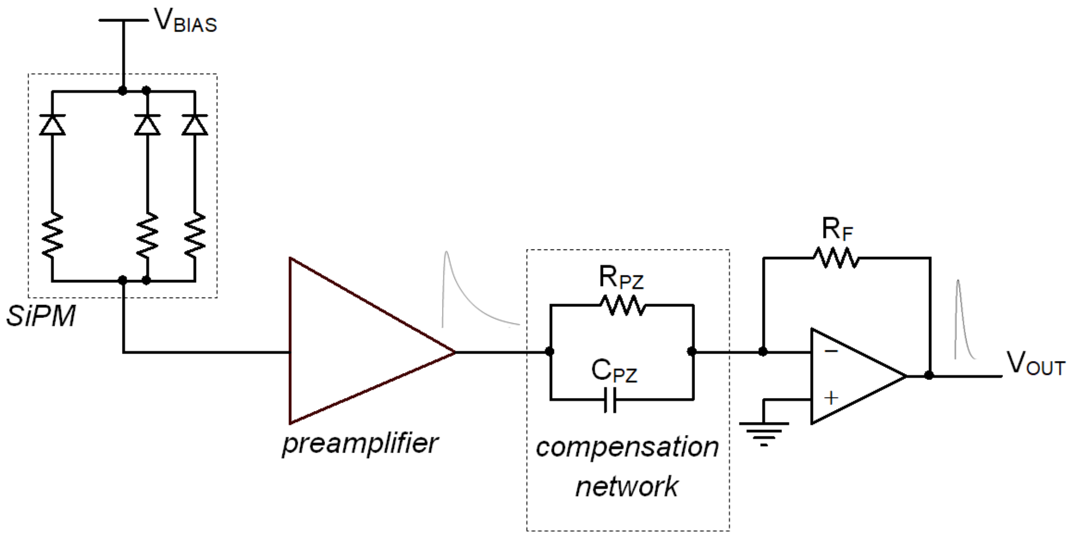

Fig. 25. The DLED technique, based on the compensation of the SiPM tail by means of pole-zero cancellation.

A similar technique is presented in [63], where the compensation zero is introduced by choosing a suitable value for the capacitor used for AC coupling of the detector to the front-end electronics, according to the value of the input resistance R_{IN} of the front-end.

Very good time resolution can be obtained with more sophisticated time pick-off techniques, based on digital processing of a number of samples of the SiPM pulse [64,65]. Several examples of multichannel fast digitizer ASICs have been proposed in the literature [66-69]. The basic circuit structure exploited in this class of circuits is a fast Switched Capacitor Array (SCA), and a simple example of architecture is illustrated in Fig. 26 [70]. The sampling signal propagates through the inverter chain, which forms a ring oscillator, and the capacitors are used as analog memories to store the samples of the signal. The depth of the capacitor array allows the storage of the SiPM pulse and, after the sampling phase, the shift register allows the readout of the array towards an ADC, which can be internal or external. As an example of performance of this kind of circuits, the DRS4 ASIC [69] hosts 8+1 channels composed by an array of 1024 storage cells; the sampling rate can be varied from 700MS/s and 6GS/s, the analog bandwidth is 950MHz and the power consumption is between 10 and 40mW/channel, depending on the sampling speed and the selected mode of operation.

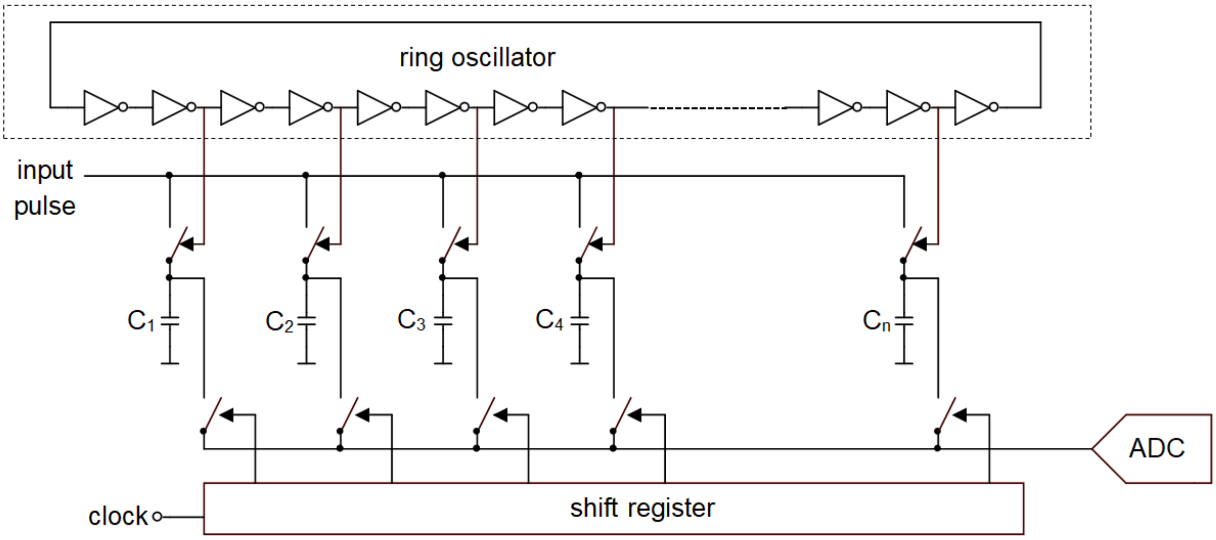

Fig. 26. An example of fast sampler: Domino structure.

Concerning the digital time pick-off methods that can be used if several samples of the raising edge of the detector pulse are available, there is a broad range of solutions. A large class of the techniques are an extension of the corresponding analog ones and exploit the samples of the signal in order to reduce the effects of noise and make more accurate the evaluation of the time when the threshold is crossed. For instance, in Digital Constant Fraction Discrimination the time when the signal overcomes a fixed fraction of the pulse amplitude is computed using the measured samples of the pulse [71]. In [72] the two consecutive samples of the pulse raising edge characterized by the maximum difference (maximum slope) are found and the time of the event is obtained by means of the intersection of the line which connects these samples with the baseline of the pulse.

Interpolation of the available samples around the threshold and normalization of the pulse amplitude is often used to increase the total number of samples and improve the accuracy in the determination of the threshold crossing time: for instance in [73] cubic spline interpolation is applied for this task.

Another class of methods is based on true digital algorithms. A possible approach tries to find a matching between a reference pulse, evaluated by means of real data or by theoretical analysis, and the measured samples, in order to reconstruct the start time of the event from the start time of the matched reference signal. For instance in [74], the pulse is modelled with the sum of two exponentials and the least mean square difference between the normalized measured pulse and the reference pulse progressively shifted is minimized. Deconvolution by means of an optimal filter is also used to reduce the effects of noise [73,75]. The application of digital processing techniques requires remarkable computing resources, depending on the nature and the complexity of the chosen technique, thus much effort is devoted in trying to simplify the algorithms employed and to make them suitable to be implemented on compact and easy to use devices, such as FPGA and DSP.

7. Conclusions

A review of the main approaches commonly applied for the readout electronics dedicated to SiPM detector has been proposed and the related issues have been discussed. A comparison between voltage mode and current mode front-end circuits has been done in the light of a simple model of the detector, showing why the latter is now the favourite choice, especially in the integrated realizations. The most common solutions used for energy and time measurements have been also presented and compared. Concerning the development perspectives in the field of front-end electronics for SiPMs, accurate modelling of the detector is one of the main issues that is still open and the role of the parasitic elements, associated to the interconnections between the SiPM and the electronics, in the formation of the signal deserves more detailed studies, so that an optimal choice for the specifications of the preamplifier, such as its input resistance and bandwidth, can be made. Another relevant issue is the evolution of the integrated technologies towards nanometer devices, mainly oriented to digital applications and very challenging when analog circuits have to be designed. For instance power supply reduction is one of the main concerns and require the development of suitable solutions to preserve the slope of the output pulse of the preamplifier, thus the accuracy in time measurements and, at the same time, a large dynamic range for the charge measurements. On the other hand the resort to this kind of technologies opens opportunities in terms of possible integration of more digital resources on chip, making possible the realization of very compact Systems on Chip (SoC) and increasing the data communication bandwidth. In this respect, a very important factor that must be taken into account is the cost of the development of electronics in these nanometer technologies. The required investments are increasing more and more and accessibility to this kind of technologies will be probably limited only to large collaborations.

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