

A Procedure to Analyze a CNTFET-Based NOT Gate with Parasitic Elements of Interconnection Lines

Roberto Marani¹ and Anna Gina Perri^{2,*}

¹Institute of Intelligent Industrial Technologies and Systems for Advanced Manufacturing (STIIMA), National Research Council of Italy, 70125, Bari, Italy

²Electronic Devices Laboratory, Department of Electrical and Information Engineering, Polytechnic University of Bari, 70126, Bari, Italy

(*) Corresponding author: annagina.perri@poliba.it
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Abstract

In this paper we analyze an application of CNTFET in the design of NOT gate, in which parasitic elements of interconnection lines are considered. At first we study the time domain analysis of NOT gate without to consider the parasitic elements of interconnection lines, in order to compare the obtained results with those in which the parasitic elements are considered, showing how they limit the high-speed performances of CNTs.

Keywords: CNTs, CNTFET, Modelling, NOT gate, Integrated circuit interconnections, VLSI, ADS.

1. INTRODUCTION

Carbon Nano Tubes (CNTs) are a promising material that can be used to realize the channel of Carbon Nano Tube Field Effect Transistors (CNTFETs), a new kind of molecular device able to work better at nanometer scale [1-13].

In this paper we present the analysis and design of a CNTFET-based NOT gate in which the parasitic elements (capacitances, inductances and resistances) of interconnection lines are considered.

At first we study the time domain analysis of NOT gate without to consider the parasitic elements of interconnection lines.

Then we present the analysis considering the parasitic elements, showing how they limit the high-speed performances of CNTs.

The presentation of the paper is organized as follows. At first we describe briefly the CNTs structure. Then we present a brief review of the CNTFET model used in this paper, and already proposed by us in [14, 15].

The simulation results are shown and discussed, together with conclusions and future developments.

2. A BRIEF REVIEW OF CNTS

A Carbon Nanotube (CNT) is a sheet of hexagonal arranged carbon atoms rolled up in a tube of a few nanometers in diameter, which can be many microns long. Graphene is a single sheet of carbon atoms arranged in the well known honeycomb structure [1].

A CNT can be single-wall (SWCNT) or multi-wall (MWCNT). In particular a SWCNT is composed by a single cylinder, having a diameter between 0.7 nm and 2 nm. Therefore the high length/diameter ratio allows considering it as a one-dimensional structure.

As it is known [1], the electronic properties of CNTs depend strongly on the chirality of the nanotube, i.e. on the indices n and m , with $0 \leq m \leq n$ for reasons of symmetry related to the honeycomb lattice: m values outside this range provide the

same results. In fact, depending on their chiral vector, CNTs have either semi-conducting or metallic behavior.

In particular, if $n = m$ or $n - m = 3i$, where i is an integer, the nanotube is metallic; in other cases it shows semi-conducting properties [16].

CNTs offer several advantages compared to Cu/low- κ interconnects because of their one dimensional nature, the peculiar band-structure of graphene, and the strong covalent bonds among carbon atoms.

In particular:

1. Higher conductivity due to their one-dimensional nature, the phase space for electron scattering in CNTs is limited, and electron mean free path is in the micron range for high quality nanotubes, in contrast to 40 nm in bulk copper. The conductivity of densely-packed CNTs is higher than scaled Cu interconnects for large lengths. Conductivity of short CNT bundles, however, is limited by their quantum resistance. Metallic SWCNTs have two conduction channels, and their quantum resistance is 6.5 k Ω ;
2. Resistance to electromigration: the strong sp^2 carbon bonds in graphene lead to an extraordinary mechanical strength and a very large current conduction capacity for CNTs, 10^9 A/cm² in contrast to 10^6 A/cm² in Cu. However, contacts may limit the maximum current density in CNT interconnects;
3. Thermal conductivity: the longitudinal thermal conductivity of an isolated CNT is expected to be very high, on the order of 6000 W/mK, as suggested by theoretical models and extrapolations on measured data from porous bundles. The thermal conduction in CNTs is highly anisotropic, and the transverse conduction is orders of magnitude lower than the longitudinal conduction [17].

However there are still numerous problems to be addressed before CNTs can

be utilized as interconnects, which are mainly:

1. Achieving a high-density integration with CNTs: CNT-bundles can outperform copper wires in terms of conductivity only if they are dense enough;
2. Selective growth of metallic SWCNTs: SWCNT growth processes developed to date cannot control chirality;
3. Achieving low-resistance contacts: the metal electrode contact with CNTs may cause reflection effects and cause contact resistance [17].

The main electronic applications of CNTs are the channel in field effect transistors [18-20].

In the simulations presented in this paper, we have used a CNTFET model, already proposed by us in [14-16], which we briefly refer to here.

3. A BRIEF REVIEW OF OUR CNTFET MODEL

An exhaustive description of our CNTFET model is in our Refs [2-3] and therefore the reader is requested to consult them. In this Section we just describe the main equations on which is based our model.

With the hypothesis that each sub-band decreases by the same quantity along the whole channel length [2], the total drain current can be expressed as:

$$I_{DS} = \frac{4qkT}{h} \sum_p \left[\ln(1 + \exp \xi_{Sp}) - \ln(1 + \exp \xi_{Dp}) \right] \quad (1)$$

where q is the electron charge, k is the Boltzmann constant, T is the absolute temperature, h is the Planck constant, p is the number of sub-bands, while ξ_{Sp} and ξ_{Dp} , depending on temperature through the sub-bands energy gap, and the surface potential, V_{CNT} , have the expressions reported in [2-3].

In order to simulate correctly the CNTFET behaviour, we needed to estimate parasitic capacitances and inductances as well as the drain and source contact

resistances. We have achieved this goal using an empirical method [2-3], more suitable for simulations in CAD environment, comparing the device characteristics with the measured ones. In this way all elements of the equivalent circuit can be determined [2-3].

4. DESIGN RULES OF I.C.

In order to estimate parasitic elements in CNTs embedded I.C., we have analyzed 50 nm technology. Moreover it is also possible a predictions analysis on 10 nm and 3 nm technology [21-22].

The first step of this work is to know the length, width and thickness of metal interconnection lines in integrated circuits. For this we have referred to MICROWIND software [23]. In particular MICROWIND is truly integrated software encompassing IC designs from concept to completion, enabling chip designers to design beyond their imagination.

MICROWIND integrates traditionally separated front-end and back-end chip design into one flow, accelerating the design cycle and reduces design complexities. For our purposes, MICROWIND 3 has been used. The software provides, over a tool for layout design itself, a list of design rules for every current type of technology. In Table 1 we have summarized the obtained results.

As we can see from Table 1, dimensions in integrated circuits are usually expressed in function of λ , which most of the times is half of the technology length, thus half of the channel length.

The 10 nm target has been achieved using FinFET, which were commercialized in the first half of the 2010s. In 2018, microchips utilizing FinFET gates first became the dominate gate design at 14 nm, 10 nm, and 7 nm process nodes [24].

Regarding CNTs, a theoretical limit of 10 nm should be set, because of various complex quantum mechanics phenomena which affect the sub-10 nm regime [12].

Table 1. 50 nm design rules.

Technology	50 nm
λ :	25 nm
Metal minimum length	3* λ (75 nm)
Metal minimum width	3* λ (75 nm)
Metal thickness	350 nm
Metal minimum spacing	4* λ (100 nm)
Contact minimum width	2* λ (50 nm)
Contact minimum spacing	3* λ (75 nm)

Therefore, design rules of CNT embedded in I.C. have been predicted considering design rules of previous technologies and lithography limits.

5. DYNAMIC ANALYSIS OF NOT GATE WITHOUT PARASITIC ELEMENTS

The schematic of a NOT gate implemented by Verilog-A language is shown in Figure 1. In this case we have not considered the parasitic elements of interconnection lines.

The gate consists of two MOS-like CNTFETs with n and p channel respectively. In Figure 1 Gate-in and out indicate the input and the output of the gate, while V+ and V- indicate the positive and negative power supply terminals. Two current probes have been introduced to evaluate static currents flowing through the two CNTFETs.

Finally two capacitors have been introduced to model the capacitance of the metallic interconnections with respect to ground.

To perform dynamic analysis, we have used the circuit reported in Figure 2, which shows a cascade of four NOT gates, which are internally composed as in Figure 1.

The input of the first gate is connected to an impulsive voltage generator that provides a binary signal with high level equal to $+V_{CC}$ and low level equal to $-V_{CC}$, rise and fall times equal to 1.78 ps (**slow transitions**), high level duration of 16 ps and period equal to 38 ps. The rise and fall times have been chosen to give in input a typical signal of the logic, with features similar to the output signal of the cascade.

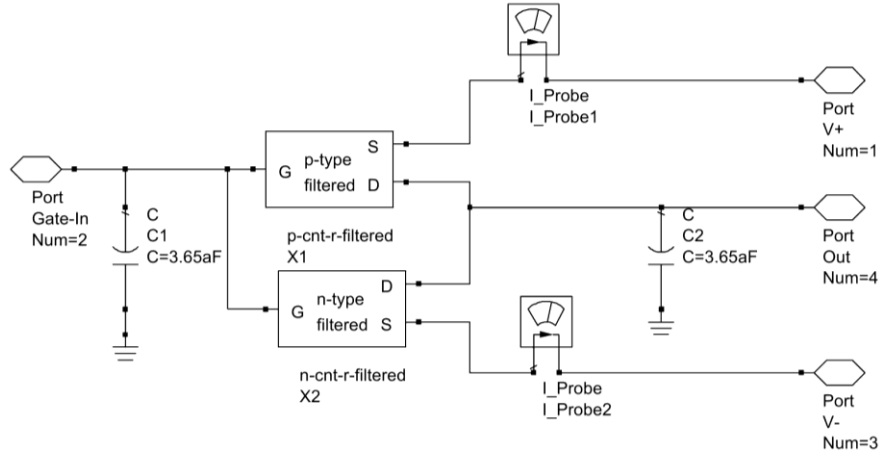


Figure 1. Schematic of a NOT gate without parasitic elements of interconnection lines.

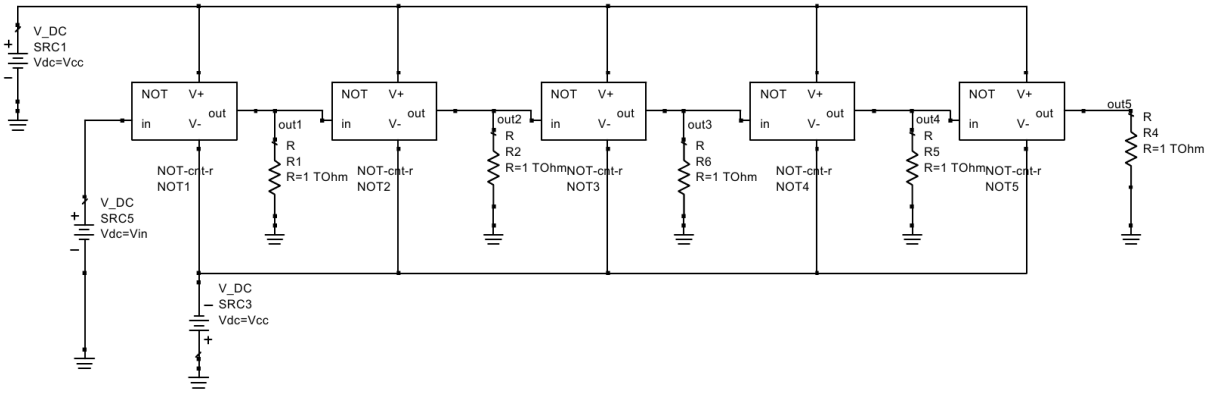


Figure 2. Schematic of a cascade of four NOT gates used for transient analysis.

For the following simulations we use a voltage supply $V_{CC} = 0.4V$, which determines the values of the high and low logic levels. In particular we chose a simulation time equal to 80 ps that allows to view the complete waveforms at the outputs of the gates.

Figure 3 shows the result of simulation for slow transitions for the proposed model, in which we have reported outputs of the first three gates, while the fourth one works as load of the third gate.

Through these diagrams we can pull out the parameters which describe the dynamic behavior of a logic gate. In particular we determine the propagation delays and the rise and fall times for the first and third gate of the cascade, so we can observe the logic gate behavior when the input signal comes directly from the generator and when the input signal had been passed

through some gates before reaching the gate in test.

Figures 4 and 5 allow determining the propagation delays for the high-to-low and low-to-high transitions respectively.

On these diagrams we have superposed some markers in order to determine the times corresponding to the 50% points of the transitions. The 50% points are equal to 0 V. In this way we can easily determine the propagation delays τ_{PHL} and τ_{PLH} , as described in [13].

For example, for the first NOT gate we obtain:

$$\tau_{PHL1} = t_{m2} - t_{m1} = 45.63 \text{ ps} - 44.50 \text{ ps} = 1.13 \text{ ps}$$

$$\tau_{PLH1} = t_{m6} - t_{m5} = 64.63 \text{ ps} - 63.50 \text{ ps} = 1.13 \text{ ps}$$

Moreover Figures 6 and 7 allow to evaluate the rise and fall times of the input and output signals at the first NOT of the cascade, with our model.

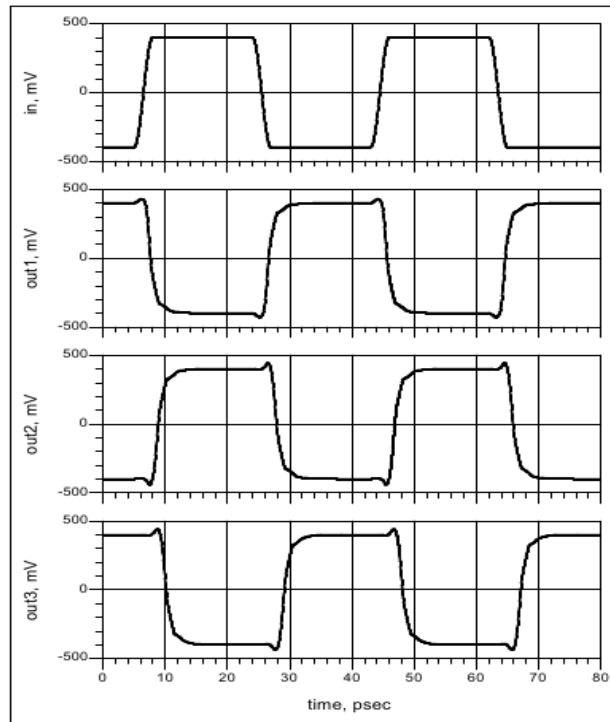


Figure 3. Output of the first four NOT gates and input signal vs time for slow transitions.

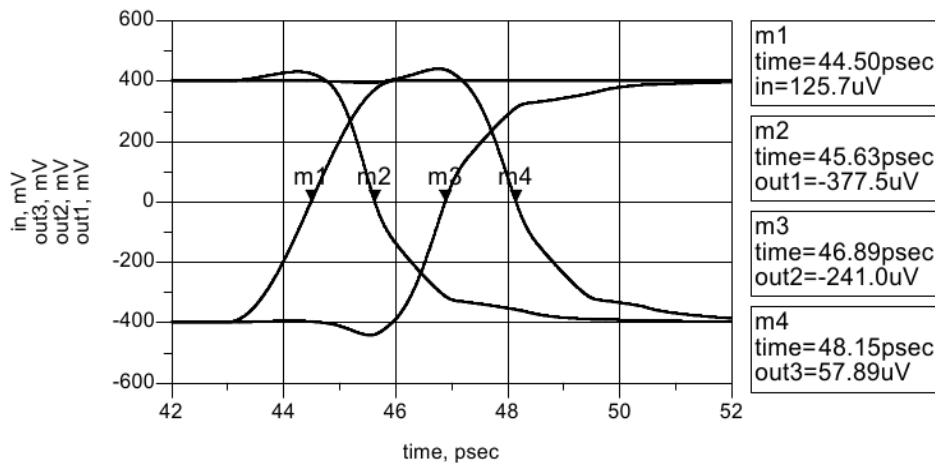


Figure 4. Input and output of transients of the NOT gates for high-to-low transitions.

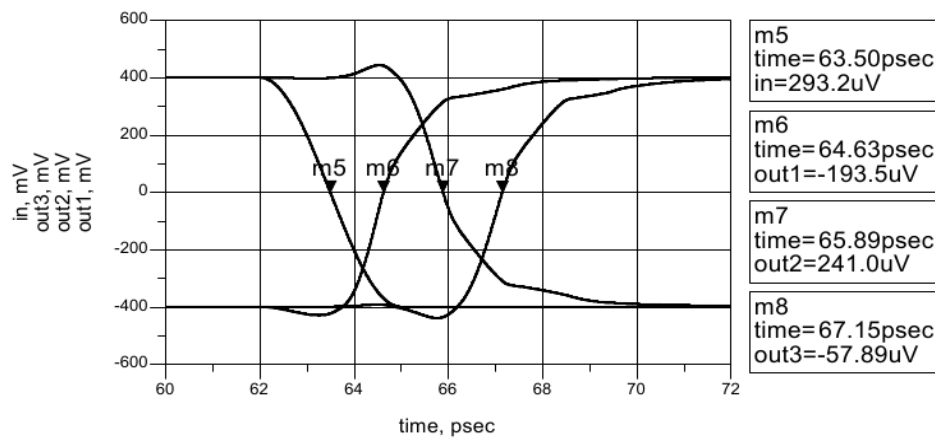


Figure 5. Input and output of transients of the NOT gates for low-to-high transitions.

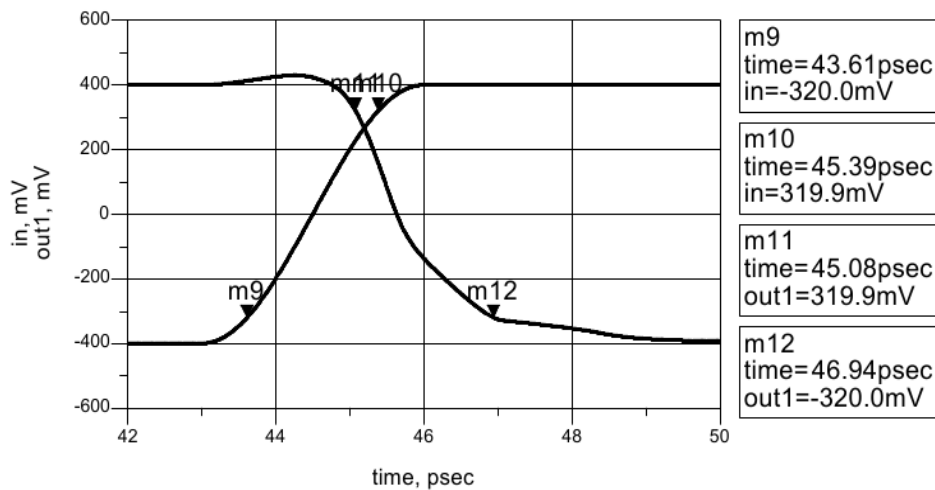


Figure 6. Input and output of transients of the first NOT gate for high-to-low transitions.

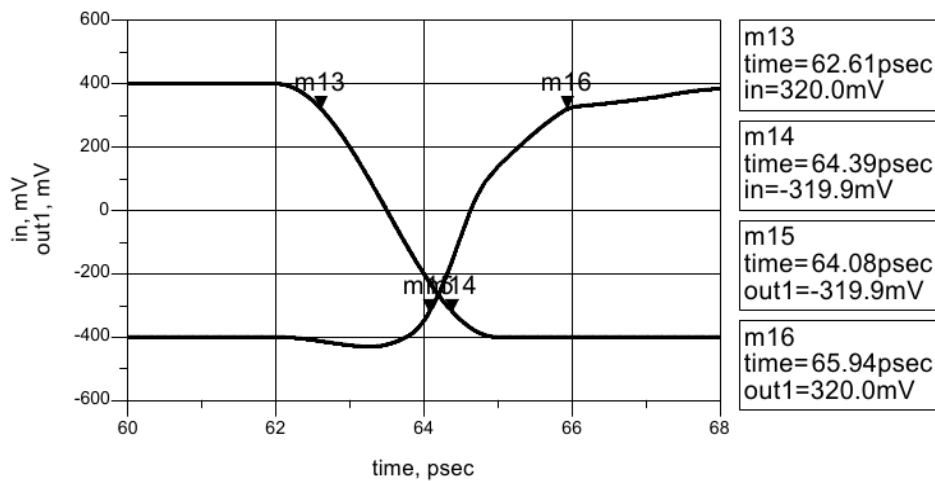


Figure 7. Input and output of transients of the first NOT gate for low-to-high transitions.

The markers on the diagrams have been positioned at the 10% and 90% points of the level transition: in this way it is possible to determine easily the rise times t_r and the fall times t_f in the following way:

$$V_{10\%} = V_L + 0.1\Delta V = -400 \text{ mV} + 0.1 \cdot 800 \text{ mV} = -320 \text{ mV}$$

$$V_{90\%} = V_L + 0.9\Delta V = -400 \text{ mV} + 0.9 \cdot 800 \text{ mV} = 320 \text{ mV}$$

$$\text{where } \Delta V = V_H - V_L = 400 \text{ mV} - (-400 \text{ mV}) = 800 \text{ mV}$$

Corresponding to the markers, it is possible to read the times referring to these points and, therefore we can determine the rise times t_r and the fall times t_f , which refer to the input and output signals.

For example, for the first gate:

$$t_{r1} = t_{m12} - t_{m11} = 47.43 \text{ ps} - 45.15 \text{ ps} = 2.28 \text{ ps}$$

$$t_{f1} = t_{m16} - t_{m15} = 66.43 \text{ ps} - 64.15 \text{ ps} = 2.28 \text{ ps}$$

6. DESIGN OF CNTFET NOT GATE WITH INTERCONNECTION LINES

In Figure 8 we show the layout of CNTFET NOT gate.

To characterize interconnection lines, the classical transmission line model, reported in Figure 9, is useful to the final purpose of estimating parasitic elements.

All parasitic elements (except for the mutual capacitance value) have been calculated with Wcalc software [25].

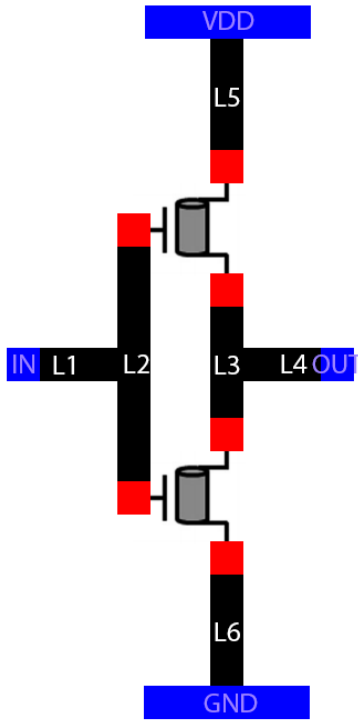


Figure 8. Layout of a CNTFET NOT gate.

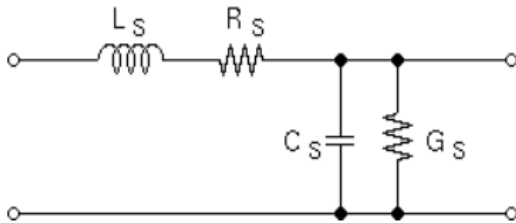


Figure 9. Transmission line model.

In particular Wcalc is a tool for the analysis and synthesis of transmission line structures and related components and provides the ability to analyze the electrical parameters of a particular structure based on the physical dimensions and material parameters. The synthesis portion calculates the required physical parameters to meet desired electrical specifications of CNTFET under test.

Regarding the expression of mutual capacitance, we referred to [26-28].

With reference to Figure 8, the metal is Cu (resistivity = $1.72 \times 10^{-8} \Omega\text{m}$) and the substrate is Si (relative permittivity = 11.8).

At first we have characterized the transmission lines, according the design

rules of I.C. previously examined, and in Table 2 we reported the parameter values in 50 nm technology.

Table 2. Values of parameters in 50 nm technology.

Parameter	Value
L1,L3,L4,L5,L6 length	100 nm
L2 length	150 nm
L1,L2,L3,L4,L5,L6 width	75 nm
Pad dimensions	50 nm x 50 nm
Channel length	50 nm
Substrate thickness	50 μm
Metal thickness	350 nm
L2-L3 distance	100 nm

The next step has been to estimate the values of parasitic elements of lines L_i ($i=1..6$), using Wcalc software tool [25].

The obtained results are reported in Table 3.

Table 3. Values of parasitic elements in 50 nm technology.

Line	Rs (0.00065 8314 Ω/nm)	Ls (1.389 46e-15 H/nm)	Cs (4.753 84e-20 F/nm)	Gs (6.784 42e-13 S/nm)
L1,3,4, 5,6	0.0658 Ω	1.3895 e-13 H	4.7538 4e-18 F	6.7844 2e-11 S
L2	0.0987 Ω	2.0842 e-13 H	7.1308 e-18 F	1.0177 e-10 S

The mutual inductance between L2-L3 is 6.92114×10^{-15} H (coupling coefficient equal to 0.424981) and the mutual capacitance between L2-L3 is 2.1335×10^{-20} F [26-28].

Similarly it is possible determined the parameter values in 10 nm and 3 nm technology and the relative values of parasitic elements of lines L_i ($i=1..6$).

7. TIME DOMAIN ANALYSIS

The following simulations are obtained in Verilog-A and then implemented on the simulator Advanced Design System (ADS) [29].

The NOT schematic, full up of parasitic elements, is shown in Figure 10. This schematic is the same for 50 nm, 10 nm

and 3 nm: only the values of parameters change.

As we can see from Figure 10, to make the circuit totally symmetrical, L2 and L3

lines (Figure 8) parasitic elements have been split in two parts. Therefore a mutual inductance between inductors L7-L9 and L8-L10 must be considered.

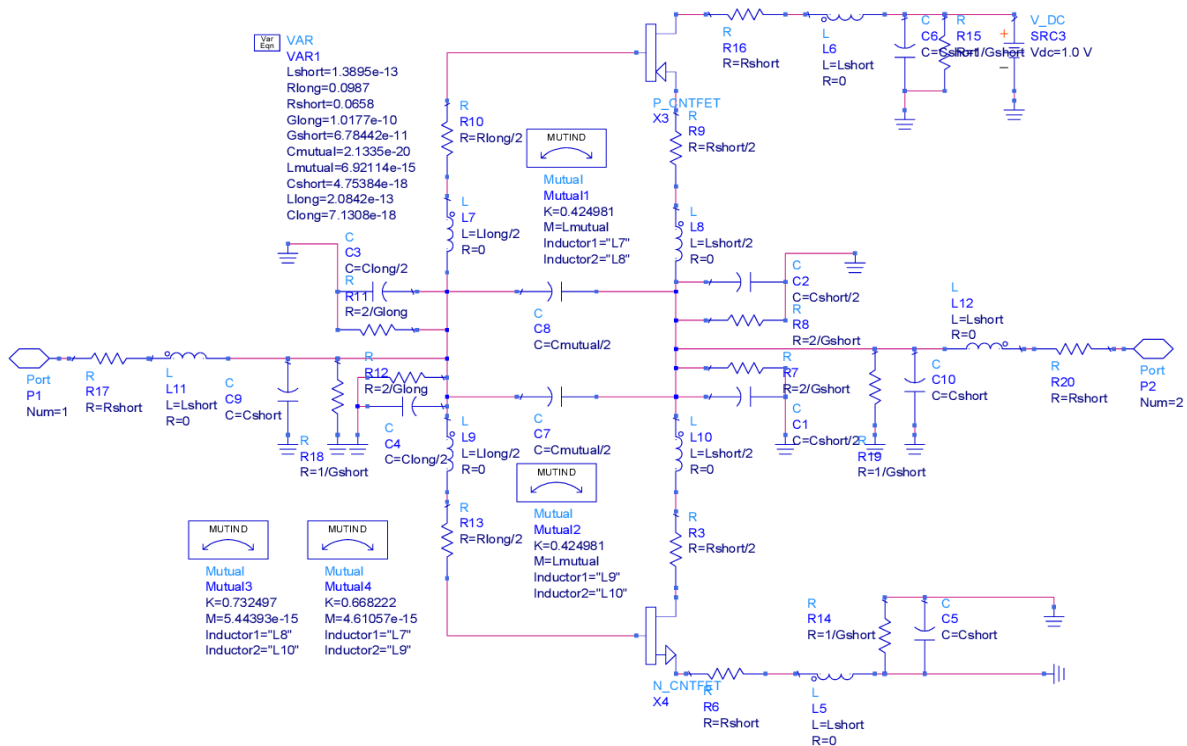


Figure 10. Schematic of 50 nm CNTFET NOT gate with parasitic elements.

The calculated values of the mutual inductance and of coupling coefficient are:
 L7-L9 mutual inductance and coupling coefficient: $4.61057e-15$ H 0.668222
 L8-L10 mutual inductance and coupling coefficient: $5.44393e-15$ H 0.732497.

The first step was to choose a proper power supply voltage because the circuit

must work as a good inverter, which means that the negative derivative of the gain must pass only two times across an horizontal straight line of value 1.

To choose the power supply, we used the circuit shown in Figure 11.

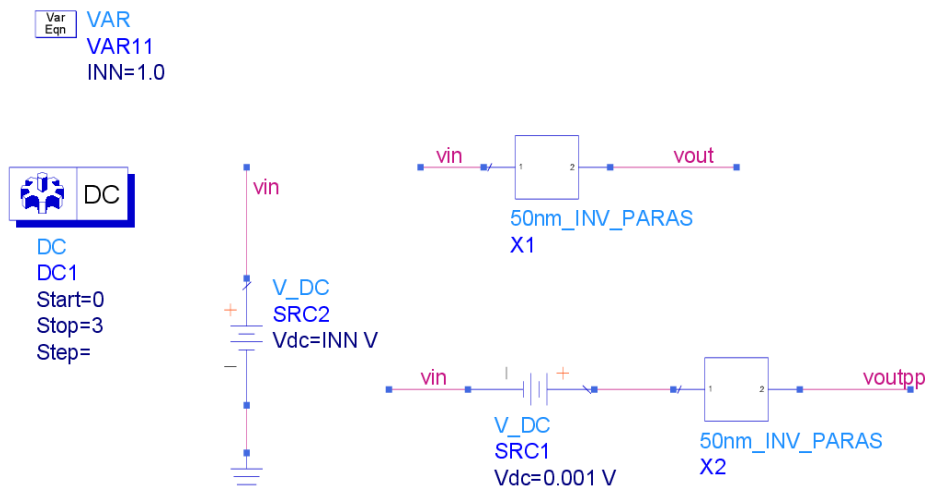


Figure 11. Gain test circuit.

The two boxes of Figure 11 symbolize the schematic of Figure 10.

A DC sweep on the input voltage provides the results shown in Figure 12.

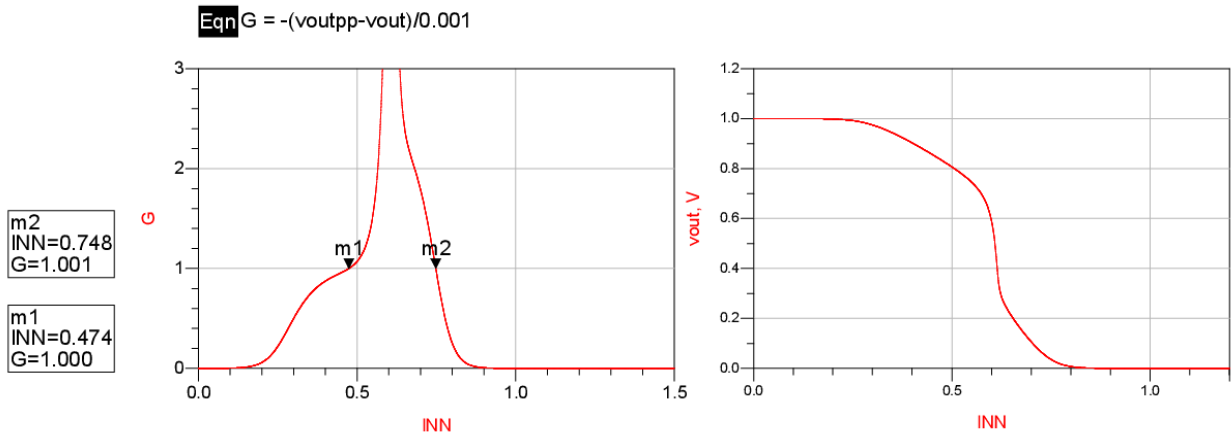


Figure 12. NOT gain in 50 nm technology.

On the left, the negative derivative of the gain is shown. As we can see, it passes only two time across a horizontal straight line of value 1, which means that the gain has only two points with a unitary derivative.

These two points, approximately 0.47 V and 0.75 V, are the thresholds of the inverter. For values of V_{in} between the thresholds, the gain must have a negative derivative greater than one.

On the right, a plot of V_{out}/V_{in} is shown. As we can see, the plot features a classical inverter characteristic.

To analyze the performance of the 50 nm NOT gate in 50 nm technology, the simulation circuit used is shown in Figure 13, in which every box symbolizes the schematic of Figure 10.

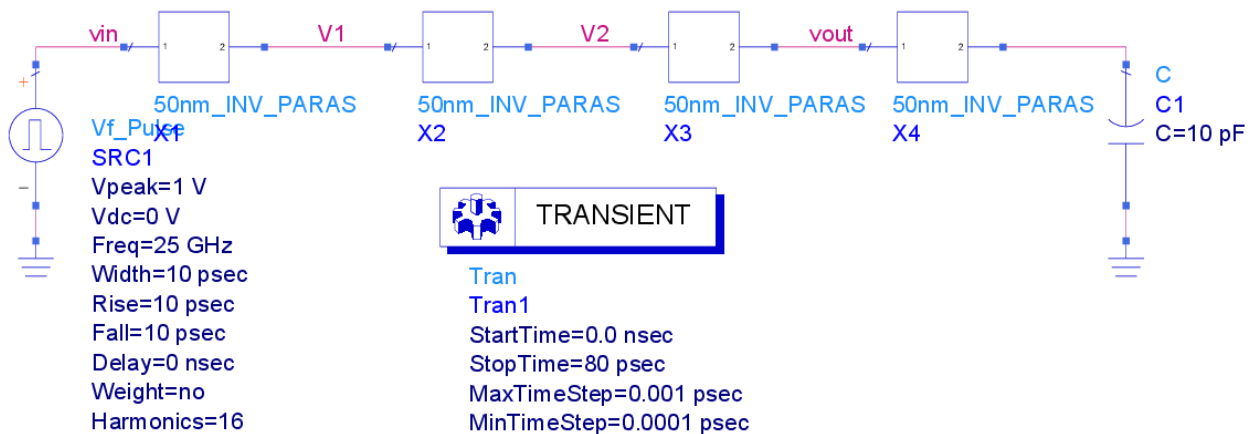


Figure 13. NOT gate in 50 nm technology.

Four CNTFET inverters, full of parasitic, have been used. This choice is justified by the fact that to perform a transient analysis it is necessary to simulate the non-linear load effects on a certain device. So, the

useful output voltage is the one of the third stage.

The simulation results are reported in Figure 14.

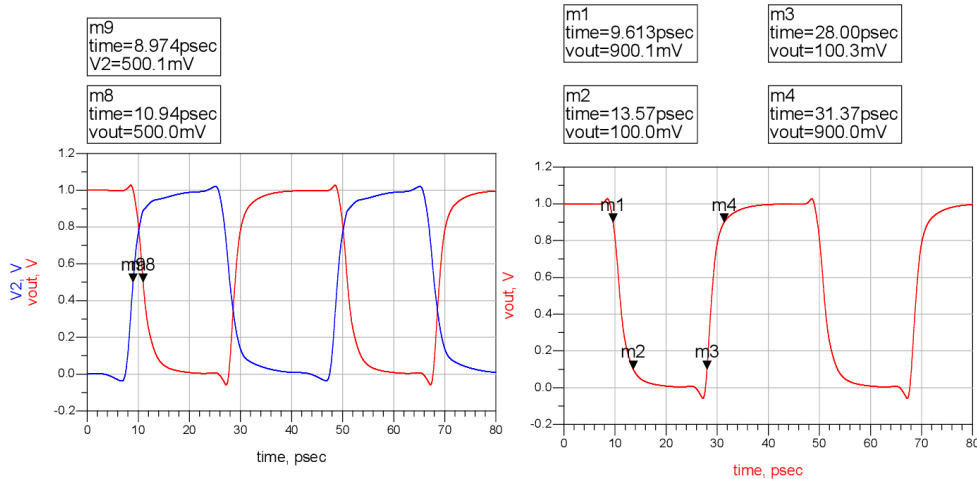


Figure 14. Time domain analysis in 50 nm technology.

On the right there is the output waveform out of the third stage, which is almost the inverted ideal pulse generator waveform.

On the left, there are the output waveforms out of the second stage and the third stage.

The measured fall time and rise time are respectively 3.96 ps and 3.37 ps.

The measured 50% delay is 1.97 ps.

We have applied the proposed procedure also to NOT gate in 10 nm and 3 nm technology, obtaining the fall time and rise times, and 50% delay time values, reported in Table 4.

Table 4. Time domain analysis: values of fall, rise time and 50% delay time.

Technology	Fall time	Rise time	50% delay
50 nm	3.96 ps	3.37 ps	1.97 ps
10 nm	0.73 ps	0.61 ps	0.36 ps
3 nm	0.59 ps	0.49 ps	0.29 ps

As was to be expected, these times decrease with technology dimensions and, for any technology, the effects of parasitic elements of interconnection lines is to

increase the characteristic times and therefore to limit the high-speed performances of CNTs.

8. CONCLUSION AND FUTURE DEVELOPMENTS

We have presented the analysis and design of a CNTFET-based NOT gate in which the parasitic elements of interconnection lines are considered.

At first we studied the time domain analysis of NOT gate without to consider the parasitic elements of interconnection lines.

Then we presented the analysis considering the parasitic elements, showing how they limit the high-speed performances of CNTs.

Currently we intend to repeat the proposed procedure using other CNTFET models such the model proposed in literature [30-31] in order to have comparable results.

CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

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