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Impact of the CNT Parameter Variations on Performance of Digital Circuits Based on CNTFET

Roberto Marani[1] and Anna Gina Perri[2,*]

[1]Institute of Intelligent Industrial Technologies and Systems for Advanced Manufacturing (STIIMA), National Research Council of Italy, 70125, Bari, Italy
[2]Electronic Devices Laboratory, Department of Electrical and Information Engineering, Polytechnic University of Bari, 70126, Bari, Italy

(*) Corresponding author: annagina.perri@poliba.it
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Abstract
In this paper we propose a method to study the impact of the CNT parameter variations on performance of CNTFET digital circuits. In particular we consider CNT parameters that fully identify the geometrical properties of a regular CNT, which are the length and structural indices (n, m) of CNT. We analyse in particular the effects on NAND gate using a N and P type CNTFET, polarizing at a fixed voltage and varying the CNT parameters. As regards the indices, we limit the analysis to zig-zag CNT, highlighting that the proposed procedure can be applied to other types of CNT.
Keywords: *Nanoelectronics, Nanodevices, CNT, CNTFET, Modelling, Digital circuits, Verilog-A.*

1. INRODUCTION

We have been dealing with Carbon NanoTubes (CNTs) [1] and Carbon NanoTube Field Effect Transistors (CNTFETs) [2-11] for many years now. In particular we have studied extensively MOSFET-like CNTFET for high-performance and low-power memory designs [12-45].

CNTs, when they are defect free, are identified by their length and their structural indices (*n, m*). Therefore, when they are used to build a CNTFET, these are the key parameters to identify the FET behavior. Of course, these parameters are not the only, since also contacts and parasitics have their influence, but these are technological parameters not related to intrinsic properties.

In [41] we proposed a procedure to study the impact of CNT parameter variations on the performance of CNTFET analog circuits, considering, as example, a linear common source amplifier based on a N type CNTFET, simulated with the model, already proposed by us [2-3].

In this paper we want to study the impact of the CNT parameter variations on performance of CNTFET digital circuits, in order to identify those values of considered parameters to obtain the best performance.

We also want to highlight that in previous works [46-48], the impact of the CNT diameter variations alone on performance of CNTFET digital circuits has been considered.

In particular, as an example, we study a NAND gate, considering the dependence of CNTFET on CNT index and length. As regards the indices, we present the analysis for a zig-zag CNT, but the proposed procedure can be applied to other types of CNT.

We obtain that the best results are for the shortest and thinnest CNT analysed in our study, that is index 17 and length 25 nm. Index larger than 25 should not be used since they have small noise margins, and length larger than 100 nm have large delay and rise/fall times.

All simulations are carried out using the software Advanced Design System (ADS), which is compatible with the Verilog-A programming language [49], avoiding so the instability problems presented in SPICE used in previous designs, proposed in literature [46].

The presentation of the paper is organized as follows.

In Sections 2 and 3 respectively we briefly recall the CNT properties and our I-V and C-V CNTFET models [2-3].

Then, in Section 4, varying the CNT parameters, we analyze their effects on a NAND gate using a N and P type CNTFET and we show and discuss the simulation results. Finally, Section 5 gives the conclusions and future developments.

2. REVIEW OF CNTs

A CNT is a sheet of hexagonal arranged carbon atoms rolled up in a tube of a few nanometers in diameter, which can be many microns long [1].

Since the CNT is made up of one or more sheets of graphene rolled up in a tubular structure, the binding in the CNT is nearly identical to that of graphite.

Figure 1 shows the construction of a graphene sheet, in which carbon atoms are located at each crossing and the lines indicate the chemical bonds, which are derived from sp^2-orbitals.

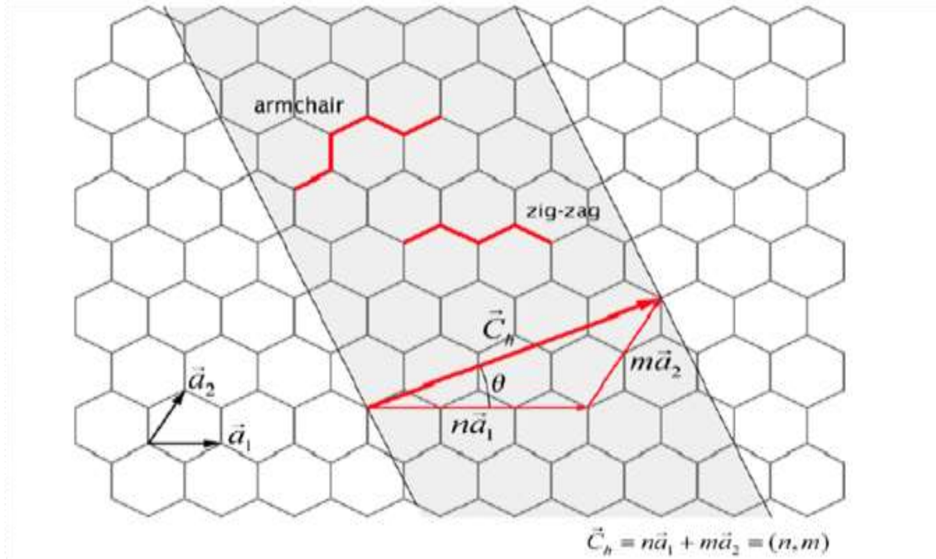

Figure 1. *Graphene sheet indicating the chiral vector.*

C_h is called *chiral vector* and is given by Eq. (1):

$$C_h = n\bar{a}_1 + m\,\bar{a}_2 \qquad (1)$$

being *n* and *m* a pair of integers and $\bar{a}_1$ and $\bar{a}_2$ the lattice vectors, which define a parallelogram constituting the primitive unit cell.

The angle θ is called *chiral angle*. In particular we have two particular types of nanotubes:

1. Those of *armchair* type (n = m, θ = 0°)
2. Those of *zig-zag* type (m = 0, θ = 30°).

For chiral angles 0° < θ < 30°, the CNT is named, more generally, as a *chiral type CNT*.

As it is known [1], the electronic properties of CNTs depend strongly on the chirality of the nanotube, i.e. on the indices n and m. It is required 0 ≤ m ≤ n for reasons of symmetry related to the honeycomb lattice: m values outside this range provide the same results. In fact, depending on their chiral vector, CNTs have either semi-conducting or metallic behavior.

In particular, if $n = m$ or $n - m = 3i$, where i is an integer, the nanotube is

metallic; in other cases, it shows semi-conducting properties [24].

3. REVIEW OF OUR I-V and C-V CNTFET MODELS

3.1. I-V Model

An exhaustive description of our CNTFET model is in [2-3] and therefore the reader is requested to consult them.

The model, based on the hypothesis of ballistic transport, makes reference to [50] and on the following improvements introduced in [51-52] to solve some numerical problems of the original paper [50].

In this Section we just describe the main equations on which our I-V model is based.

The total drain current in our model has been expressed through Eq. (2) [53]:

$$I_{DS} = \frac{4qkT}{h}\sum_{p}\left[\ln\left(1+\exp\xi_{Sp}\right)-\ln\left(1+\exp\xi_{Dp}\right)\right] \quad (2)$$

where q is the electron charge, k is the Boltzmann constant, T is the absolute temperature, h is the Planck constant, p is the number of sub-bands, while ξ_{Sp} and ξ_{Dp}, which depend on temperature through the sub-bands energy gap, and on the surface potential V_{CNT}, have the expressions reported in [2-3].

3.2. C-V Model

Regarding the C-V model, an exhaustive description of our C-V model is widely described in [7-8] and therefore the reader is requested to consult these references, in which the following expressions of quantum capacitances C_{GD} and C_{GS}, reported in Eq. (3), are widely explained:

$$\begin{cases} C_{GD} = q\sum_{p}\frac{\partial n_{Dp}}{\partial V_{GS}} = q\sum_{p}\frac{\partial n_{Dp}}{\partial \xi_{Dp}}\frac{\partial \xi_{Dp}}{\partial V_{CNT}}\frac{\partial V_{CNT}}{\partial V_{GS}} \\ C_{GS} = q\sum_{p}\frac{\partial n_{Sp}}{\partial V_{GS}} = q\sum_{p}\frac{\partial n_{Sp}}{\partial \xi_{Sp}}\frac{\partial \xi_{Sp}}{\partial V_{CNT}}\frac{\partial V_{CNT}}{\partial V_{GS}} \end{cases} \quad (3)$$

In order to simulate correctly the CNTFET behavior, we needed to estimate parasitic capacitances and inductances as well as the drain and source contact resistances.

We have achieved this goal using an empirical method exhaustively described in [2-3], where we explained that V_{FB}, R_D, R_S have been determined by a best-fit procedure between the measured and simulated values of I-V characteristics of the device, while the quantum capacitances have been computed from the charge in the channel. In this way all elements of the CNTFET equivalent circuit are determined.

Figure 2 shows our model, in which we have reported the values of circuital elements.

It is characterized by the flat band generator V_{FB}, the quantum capacitances C_{GS} and C_{GD}, the inductances of the CNT L_{drain} and L_{source} and the resistors R_{drain} and R_{source}, in which the parasitic effect due to the electrodes are also included.

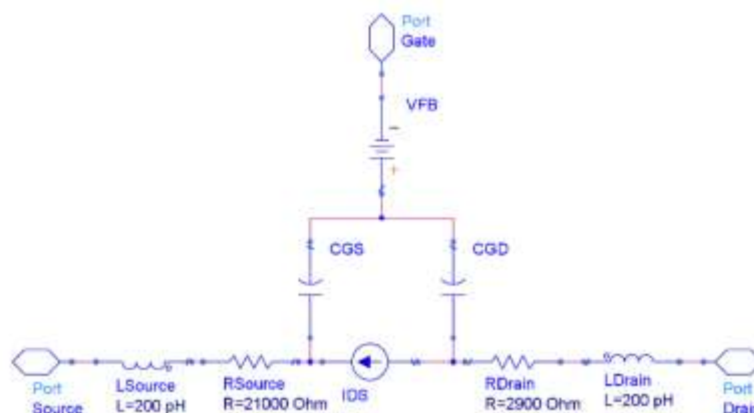

Figure 2. *Equivalent circuit of a n-type CNTFET.*

Other authors [54-55] have then assumed these parameters fixed to constant and typical values (i.e. $V_{FB} = 0$ V [54] and $R_D = R_S = 25\,k\Omega$ [55]), thus losing the dependence on the CNT diameter.

Regards to the CNT quantum inductance, as shown in Figure 2, we have assumed constant and equal to 4 pH/nm, which we have splitted up into two inductances of 2 pH/nm, while the classical self-inductance, as it is known [54], can be ignored.

4. EFFECTS OF CNT PARAMETERS IN THE DESIGN OF DIGITAL CIRCUITS

As we have already said, the CNTs, when they are defect free, are identified by their length and their structural indices (n, m). Therefore, these parameters are the key to identify the CNTFET behaviour. These parameters are not the only, since also contacts and parasites have their influence.

Now, as example, we study these effects on a NAND gate, shown in Figure 3.

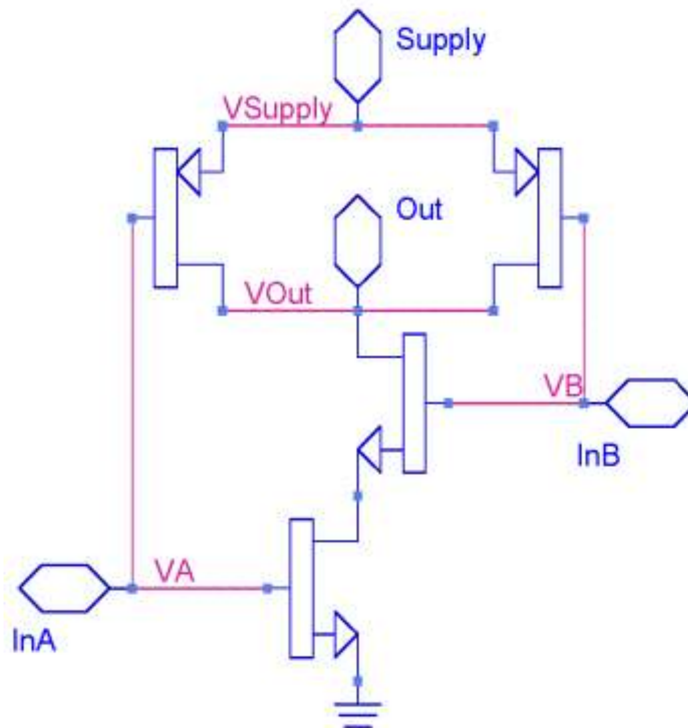

***Figure 3**. NAND gate based on P and N-type CNTFET.*

We fixed power supply $V_{dd} = 0.9$ V. Moreover, we have ignored parasitic effect coming from distributed capacitance and inductances since we are interested in intrinsic properties of the device.

During simulation we changed the CNT lengths using the following values 20 nm, 30 nm, 40 nm, 50 nm, 70 nm, 90 nm, 125 nm, 200 nm, 600 nm.

We name “upper CNTFET” those having the source connected directly to the positive supply, and “lower CNTFET” the two remaining. We used the same length for both the upper CNTFET and another length for both the lower CNTFET.

We also varied the CNT crystalline type using semiconductor zigzag types with the following structural indices: (17,0), (19,0), (23,0), (25,0), (29,0), (31,0). Of course, we avoided (18,0) (21,0) (24,0) (27,0) (30,0) since these are metallic CNT and we decided to sample only the odd values.

From now on we will identify the structural index using only the first index, since the second will be always 0. In circuit simulations we used all CNT of the same index for two main reason. First this

is would simplify the technological procedure for building these circuits. Second this choice limits the number of diagrams that we present in this analysis.

As reference configuration we used all CNT zigzag with index 17 and length 25 nm for the upper CNTFET and 70 nm for the lower CNTFET, but the proposed study can be applied to other types of CNT.

In the following simulations the unspecified CNT parameter have been set to those of reference configuration.

4.1. Static Characteristic

We simulated the static characteristic of a standing alone CNTFET NAND port using ADS [49].

We first studied the NAND input thresholds: the following figures present the dependence on the index, Figure 4, and the dependence on the length of the lower CNTFET (Figure 5) and upper one (Figure 6).

In all following Figures all data are represented by markers while we traced lines as guide for the eyes.

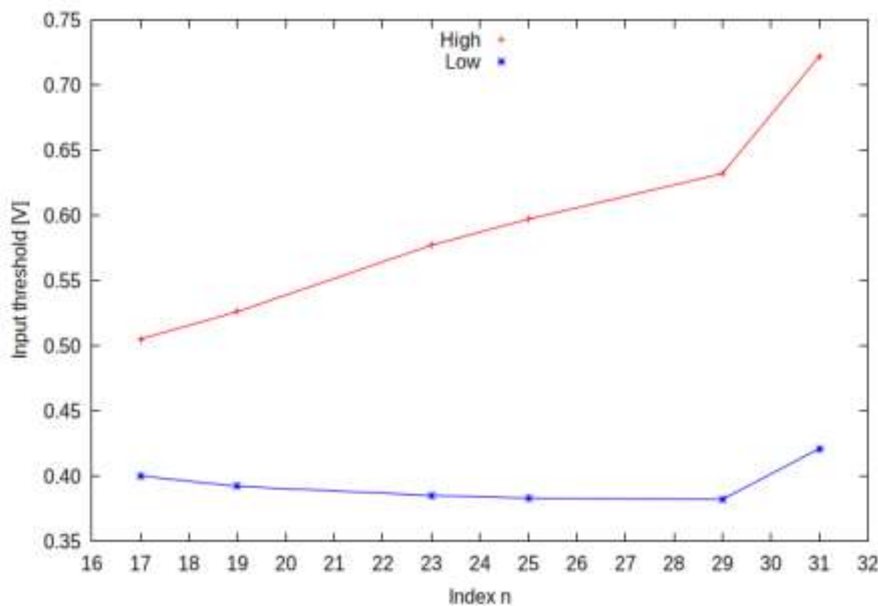

Figure 4. Input threshold voltage versus CNT index for both input logical states low and high.

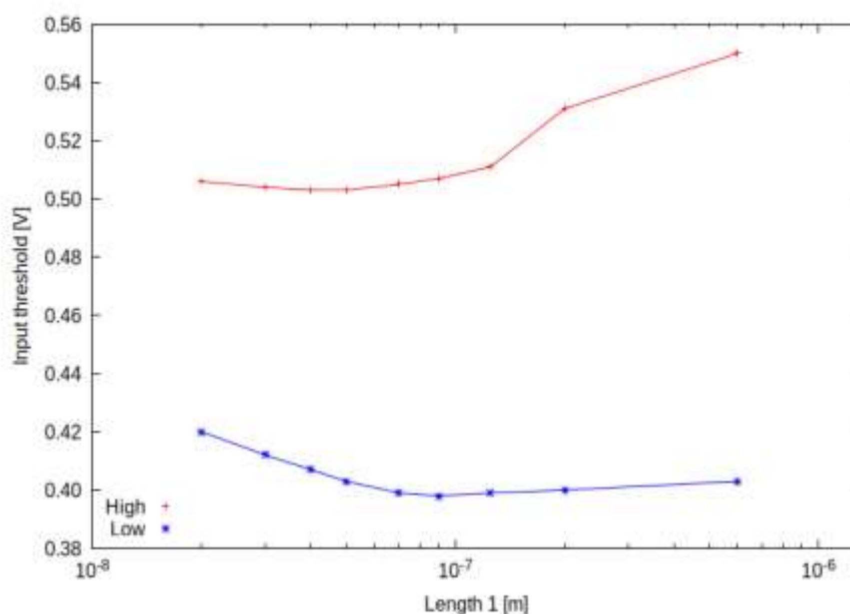

Figure 5. Input threshold voltage versus the length of the lower CNTFETs for both input logical states low and high.

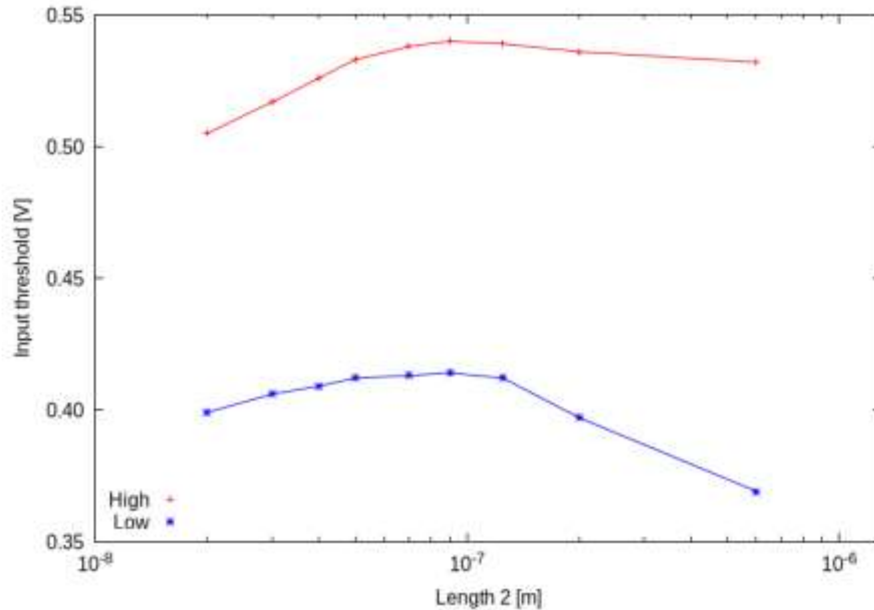

Figure 6. *Input threshold voltage versus the length of the upper CNTFETs for both input logical states low and high.*

Dependences on parameters are small, in all cases variations are less than 0.05 V except for input threshold for the logical state high which varies from 0.50 V to 0.72 V when index varies from 17 to 31.

Then we studied the NAND output thresholds: in the following figures we present the dependence on the index, Figure 7, and the dependence on the length of the lower (Figure 8) and upper (Figure 9) CNTFET.

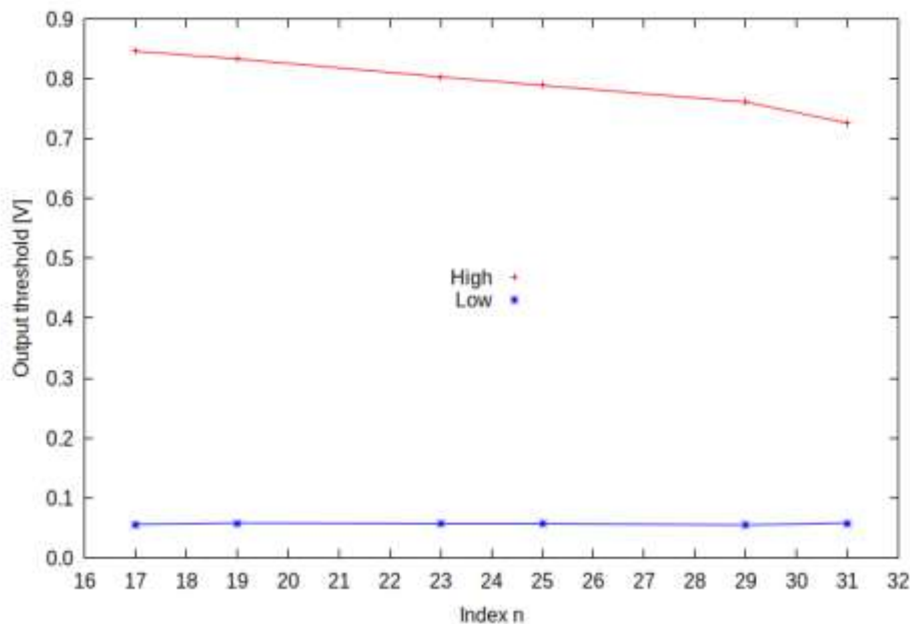

Figure 7*. Output threshold voltage versus CNT index for both input logical states low and high.*

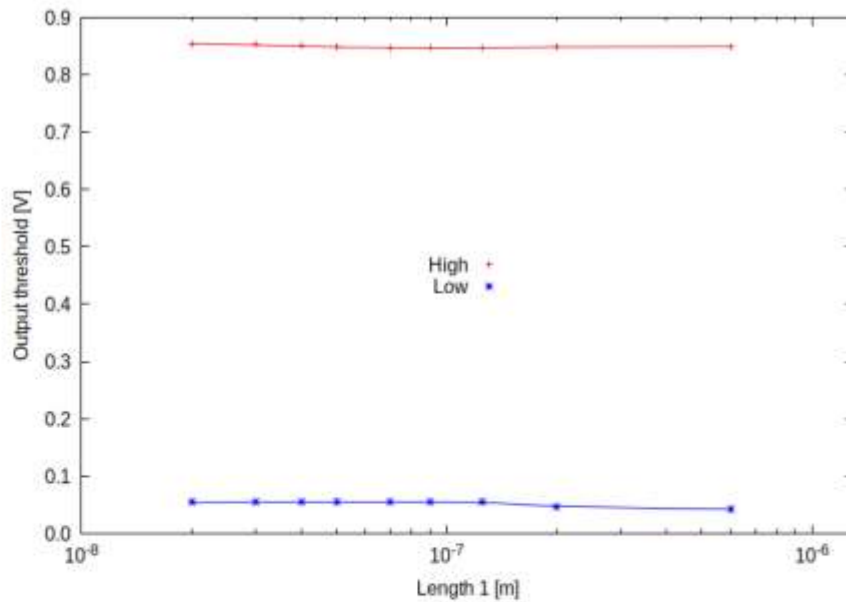

Figure 8*. Output threshold voltage versus the length of the lower CNTFETs for both input logical states low and high.*

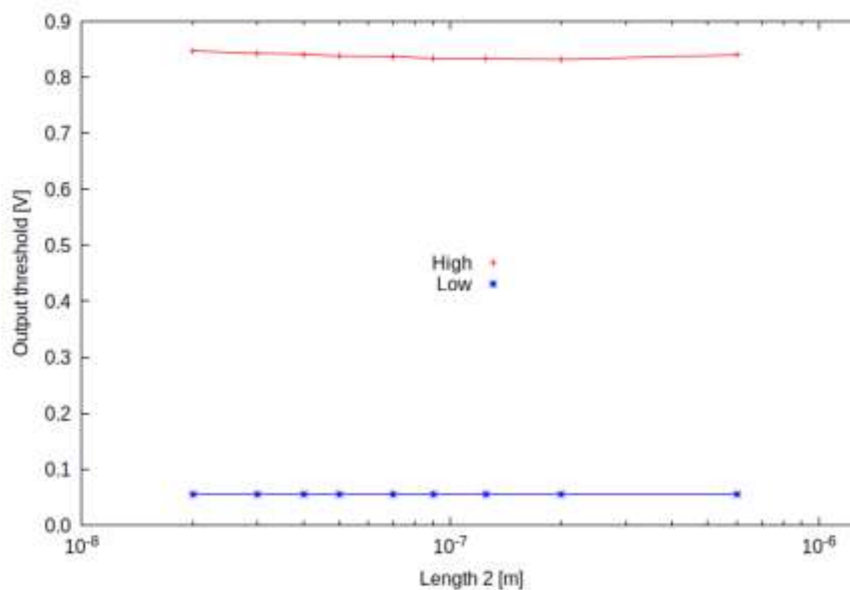

Figure 9*. Output threshold voltage versus the length of the upper CNTFETs for both input logical states low and high.*

Dependences on parameters are again small, in all cases variations are less than 0.02 V except for output threshold for the logical state high which varies from 0.84 V to 0.73 V when index varies from 17 to 31. To analyse the compatibility between input and output threshold we computed the NAND noise margin voltages, in the following figures we present the dependence on the index (Figure 10), and the dependence on the length of the lower (Figure 11) and upper (Figure 12) CNTFET.

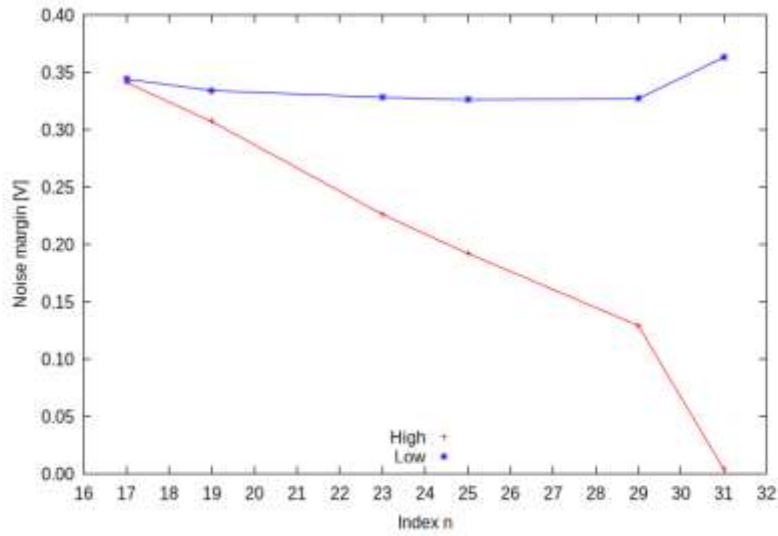

Figure 10. *Noise margin voltages versus CNT index for both input logical states low and high.*

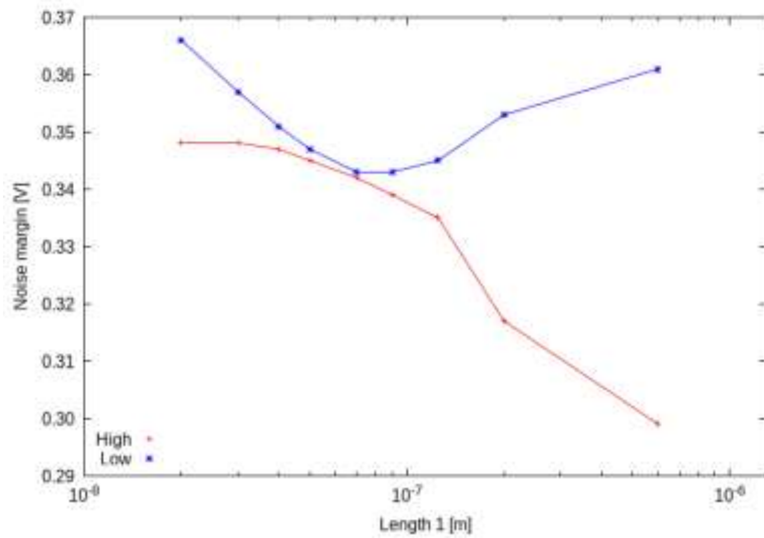

Figure 11. *Noise margin voltages versus the length of the lower CNTFETs for both input logical states low and high.*

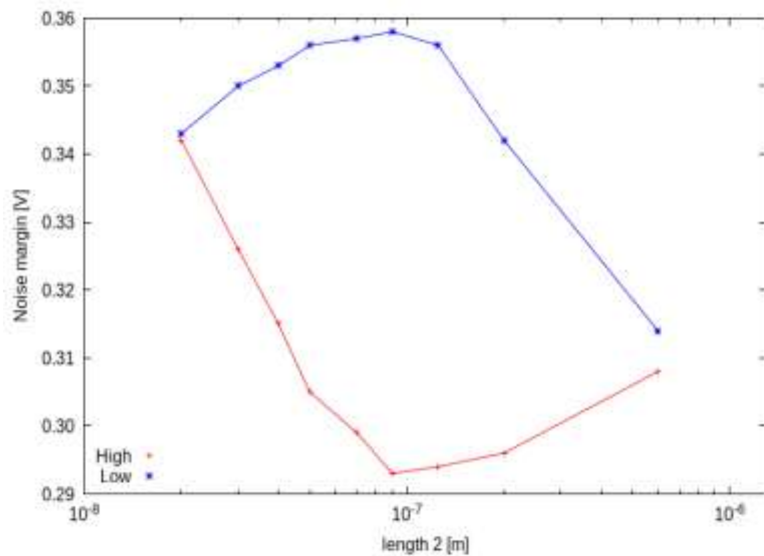

Figure 12. *Noise margin voltages versus the length of the upper CNTFETs for both input logical states low and high.*

As consequence of the previous analysis, the dependences on parameters are again small, in all cases noise margin voltages are at least 0.29 V except for output threshold for the logical state high which varies from 0.34 V to 0.004 V when index varies from 17 to 31. This suggest that while CNT length are not critical, the CNT index is critical and should be less than or equal to 25 to have a noise margin voltages greater or equal to 0.19 V.

4.2. Transient Analysis

For the determination of the characteristic times of this circuit we run a transient analysis on a chain of 2 of this NAND ports in series. The signal was supplied to the first one and we analysed the behaviour of the first one whose output is loaded by second port. The input signal applied to the two NAND input realised the logic sequence (1,0) (0,1) (0,0) (0,1) using voltage levels 0 V and 0.9 V, rise and fall time 5 ps and each state was maintained for 200 ps.

We simulated the circuit for different CNT index and we consider the transition when output swings high to low and low to high.

Figure 13 shows the delay time, while Figure 14 the falling and rising time.

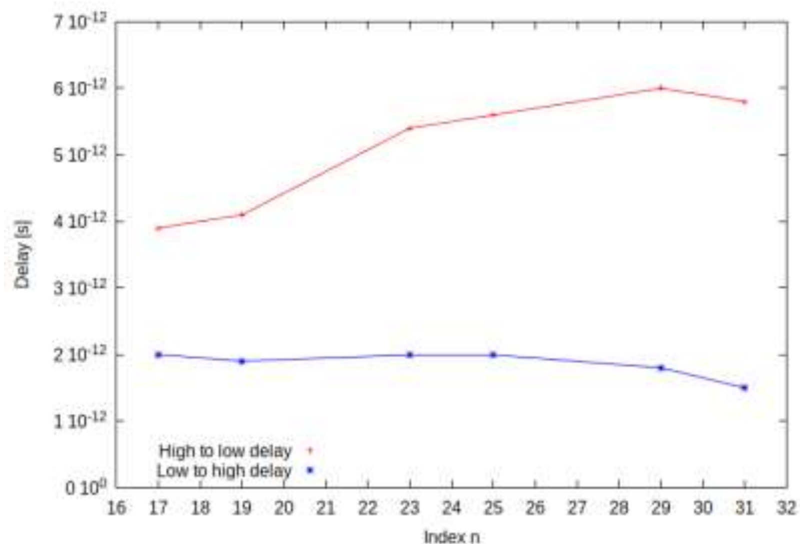

Figure 13. *Delay time versus the CNT index for output logical states going high to low and low to high.*

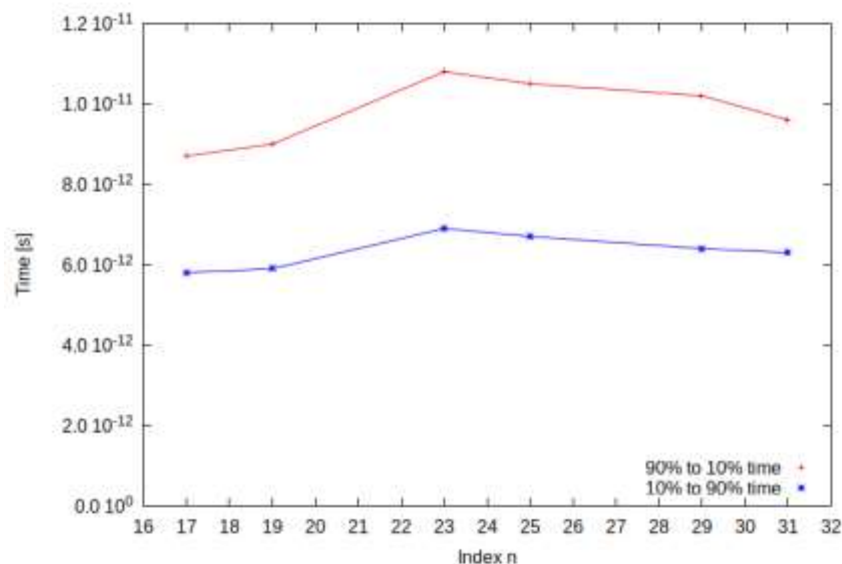

Figure 14. *Rise and fall time versus CNT index.*

We can observe that for smaller index the port is faster except for a small increase in delay time for transition low to high largely compensated by the higher gain in the inverse transition.

Then we simulated the circuit for various length of the upper and lower CNTFET and again we present the delay, fall and rise time in Figurers 15, 16, 17 and 18.

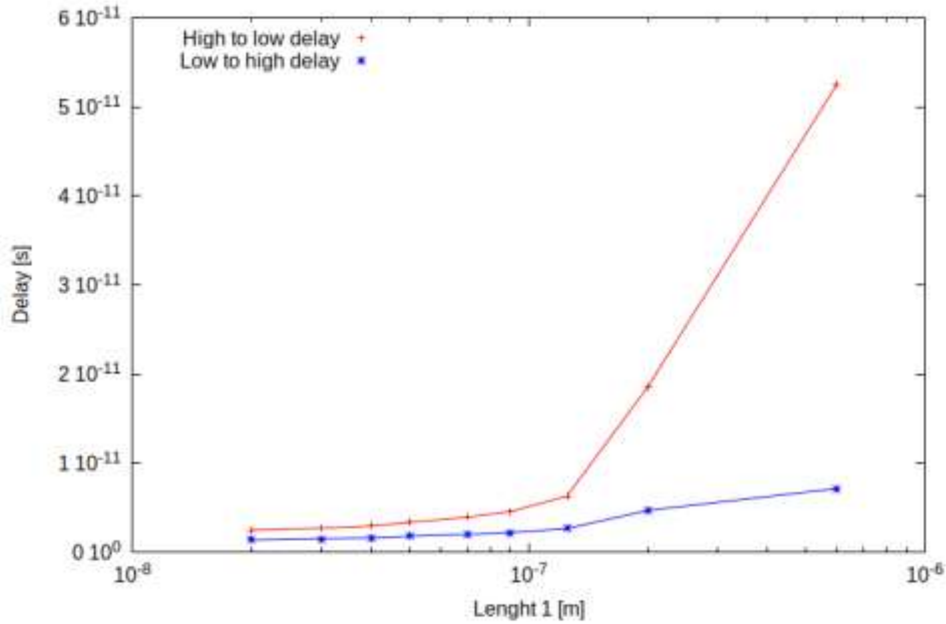

Figure 15. *Delay time versus the length of the lower CNTFET for output logical states going high to low and low to high.*

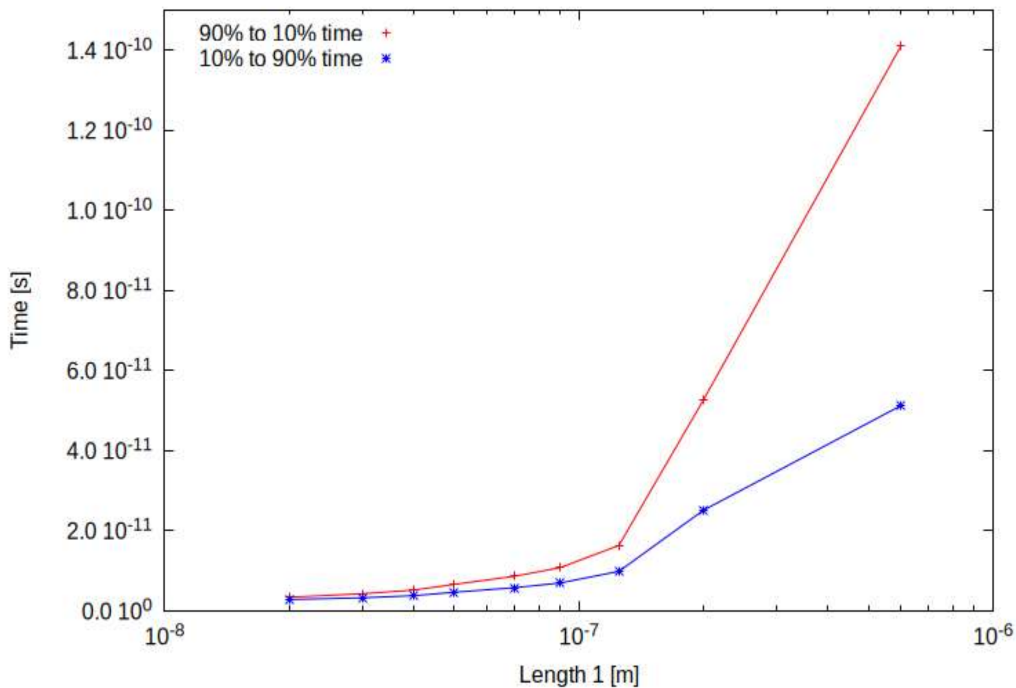

Figure 16. *Rise and fall time versus the length of the lower CNTFET.*

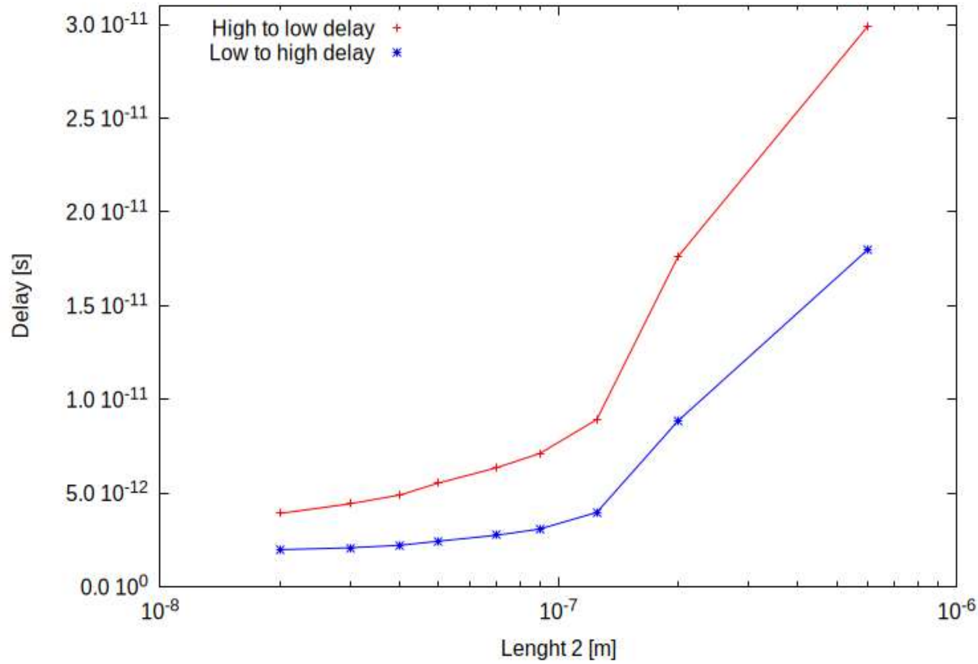

Figure 17. *Delay time versus the length of the upper CNTFET for output logical states going high to low and low to high.*

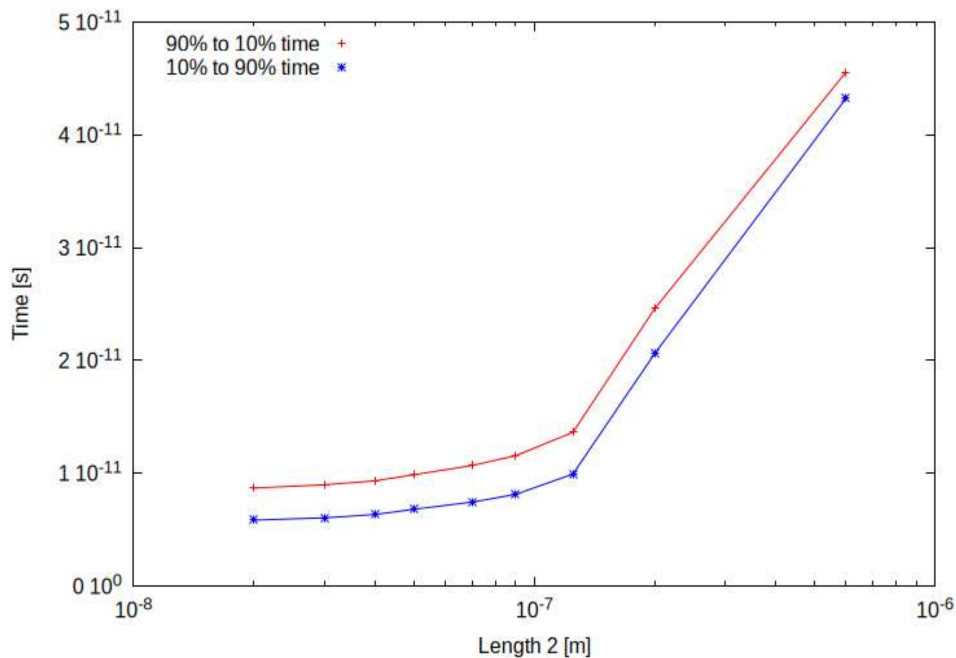

Figure 18. *Rise and fall time versus the length of the upper CNTFET.*

We observe that there is an increase in all these times when the lengths vary from 10 nm to 100 nm and a much larger increase for length over 100 nm. While length larger than 100 nm are not much interesting when the aim is the miniaturization, however this behavior pushes clearly to shortest CNTFET lengths as wished for miniaturization.

5. CONCLUSIONS AND FUTURE DEVELOPMENTS

In this paper we proposed a procedure to study the dependence of CNTFET digital circuits performance on CNT parameters, that fully identify the geometrical properties of a regular CNT. In particular the considered parameters have been the length and structural indices (n, m) of CNT, highlighting that in previous works

[46-48], only the CNT diameter variations have been considered.

The proposed procedure allowed to identify those values of parameters to obtain the best performance.

As an example, we studied a CNTFET NAND gate, observing that the best results are obtained for the shortest and thinnest CNT analysed in our study, that is index 17 and length 25 nm.

Index larger than 25 should not be used since they have small noise margins, and length larger than 100 nm have large delay and rise/fall times.

All simulations have been carried out using the software Advanced Design System (ADS), which is compatible with the Verilog-A programming language [49], avoiding so the instability problems presented in SPICE used in previous designs, proposed in literature [46].

Currently we intend to repeat the proposed simulations using other CNTFET models such the Stanford model [56-59] in order to compare results.

Moreover, we want also consider the impact of CNT parameter variations on the performance of CNTFET analog and digital circuits at variable temperatures.

CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

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