Analysis and Design of a CMOS E-Band Frequency Quadrupler With Transformer-Based Harmonic Reflectors

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***Abstract*—A frequency quadrupler based on cascaded push-push frequency doublers is presented in this work. Push-push frequency doublers have high harmonic rejection, but suffer from limited power efficiency and conversion gain, mainly due to second-harmonic feedback. Conventional harmonic reflectors minimize this undesired feedback introducing a common-mode second-harmonic resonance, at the price of increased area and reduced bandwidth. In the proposed design, the harmonic reflector is embedded into a transformer-based input matching network to decouple the differential-mode inductance from the common-mode inductance. This results in a more compact design, with higher output power and improved power efficiency. A common-gate transistor is stacked with the push-push pair to further boost the output power while reusing the same current. Two push-push frequency doublers are cascaded without additional power amplification stages. The quadrupler, implemented in 28nm CMOS, achieves a peak output power of 0 dBm and peak power efficiency of 5% at 77GHz and the 3-dB bandwidth is from 70 to 86 GHz.**

***Index Terms*—CMOS, frequency doubler, frequency quadrupler, millimeter wave, wideband, transformer**

I. Introduction

MILLIMETER-WAVE transceivers for radars and mobile communications require on-chip oscillators with high spectral purity. A common solution is the use of a sub-harmonic oscillator followed by a frequency multiplier [1], [2]. Operating the oscillator at a lower frequency allows to maximize its figure-of-merit, resulting in a better trade-off between power dissipation and phase noise. Multi-ratio frequency multipliers can also be used to extend the tuning range covered by a single oscillator [3]. Frequency multipliers, however, suffer from low power efficiency and can easily consume more power than the oscillator itself. Moreover, they generate unwanted harmonics and have limited bandwidth. This has motivated extensive research on frequency multiplier solutions [4]-[28]. Frequency multipliers are mostly based on one of two main approaches: harmonic generation by exploiting the intrinsic non-linearities of the transistor voltage-to-current characteristic [4]-[24], or signal self-multiplication using a mixer cell [25]-[28]. Frequency doublers are often implemented using transistors in push-push configuration. This balanced solution ensures high rejection of odd harmonics of the input frequency thanks to its intrinsic symmetry, while the resonant load can easily filter out the more distant even harmonics. Higher frequency multiplication factors are often needed. Fourth harmonic generation can be obtained exploiting device non-linearities in a stacked transistor pair, where the top transistor is driven in anti-phase with respect to the bottom one. In this type of frequency quadruplers [1][2], the key to combine good power efficiency and high harmonic rejection is the availability of a multi-phase signal, e.g. from a quadrature [1] or a distributed oscillator [2]. Alternatively, a fourth-harmonic generator can be constructed combining a third harmonic generator and a multiplier with its own fundamental input, provided that proper phasing is ensured [13]. Higher frequency multiplication factors are typically implemented using doublers and quadruplers as building blocks (e.g. in [14] an octupler based on a casaded quadrupler and doubler is reported). Frequency multiplication by four can be obtained by cascading two frequency doublers [15]-[16] [17]. In this case, due to the limited conversion gain of push-push frequency doublers (PPFD), some inter-stage amplification stage is typically required between the first and the second doubler, as well as as the quadrupler output. A common-gate amplifier stacked with the push-push pair can also be used [4] to boost the output power. Their main PPFD drawback lies in the undesired second-harmonic feedback, which limits their power efficiency [18]. Harmonic-reflectors (HR), forming a short around the second harmonic for common-mode input signals can alleviate this issue, at the cost of a reduced bandwidth or higher power dissipation [4]. An E-band transformer-based frequency quadrupler formed by cascaded push-push frequency doublers (PPFD) was proposed in [19]. The doublers incorporate a transformer-based HR and a stacked cascode common-gate amplifier. Even though in previous publications both a common-gate buffer [4] and a transformer [5] [6] [20] [21] have been used for the implementation of the matching network, the harmonic reflector was either not present or implemented as an additional resonant network. In [21] a push-push doubler with an harmonic reflector partly implemented using the input transformer is reported. The push-push transistors are driven both at the source and drain terminals. As a result, a smaller (ideally half) swing is required at the gate for the same gate-to-source drive, allowing the transistor to remain in saturation for a grater part of the period an enhancing the power efficiency. In this configuration, however, the push-push pair has a low input impedance (approximately $1/g_m$). As a result, the saturated output power level is achieved for a relatively large input power (around 12 dBm), higher than the saturated output power level (7 dBm), which makes it difficult to cascade similar structures to build a

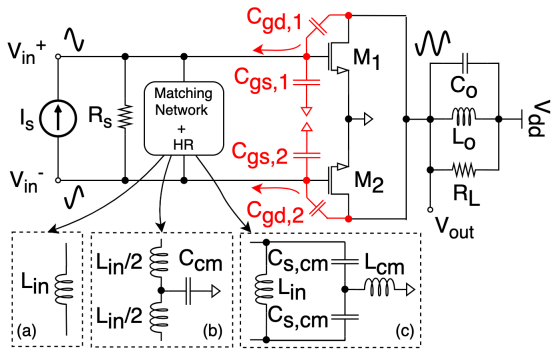


Fig. 1. Push-Push frequency doubler with: a) no harmonic reflector, b) LC harmonic reflector c) CL harmonic reflector.

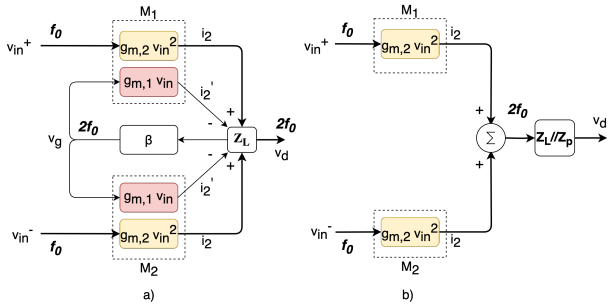


Fig. 2. Block diagram of the doubler that accounts for the feedback (a) and equivalent model with the shunt impedance Z_p (b).

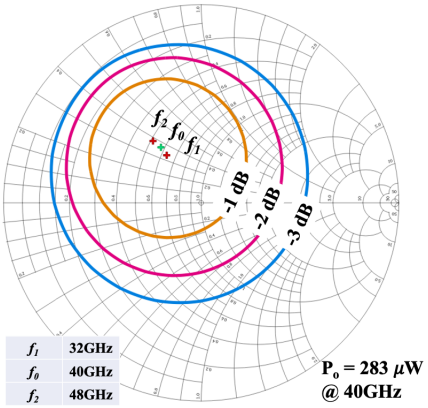


Fig. 3. Constant output power contours on the Smith Chart (w/o harmonic reflector). The dots beside f_0, f_1 and f_2 are the impedances at which the maximum power transfer to the load is achieved at the corresponding frequencies. The input signal has a peak voltage of $V_{in} = 450mV_p$ (single-ended) at 20GHz.

quadrupler without some inter-stage power gain cell. We will show that, using an HR merged with the transformer-based input matching network and a cascoded configuration, it is possible to minimize the unwanted second-harmonic feedback without degrading the operating bandwidth, while enhancing the conversion power gain and thus allowing to cascade several doublers without using interstage amplification stages. This approach can be extended, in principle, to frequency multipliers by eight. This work expands on [19], providing additional insights on its operation and design strategy, as well as additional measurements. The manuscript is organized as follows: Section II reviews the operation of the conventional PPFD, pointing out to the power efficiency limitations resulting from the undesired second-harmonic feedback, caused by the C_{gd} capacitance. A classic solution to address this issue, based on an harmonic reflector (HR) LC circuit is described in Section III.A. An improved solution, using a transformer-based HR, is proposed in Section III.B. Stability considerations are discussed in Section III.C, where it is proved that there are no conditions under which the quadrupler can oscillate. Further improvements in output power, DC-RF efficiency and bandwidth are achieved by stacking a common-gate amplifier on top of the push-push cell, as shown in Section III.D. Section IV describes the design of a frequency quadrupler implemented by cascading two PPFD that are based on the topology described in Section III, in particular Section IV.A discuss the trade-off between conversion efficiency and output power for sizing and biasing the common-source transistors of the push-push cell, Section IV.B and IV.C give more insight about the differential and common-mode analysis and design of the transformers. Section V reports the measurements results and Section VI concludes the paper.

II. Conventional Push-Push Frequency Doubler

The core of the PPFD is a pair of common-source transistors (M1 and M2 in Fig. 1) with differential inputs and a shared drain, connecting to an LC resonant load for harmonic selection. The transistors are biased in Class-C, to ensure high harmonic current generation. Assuming perfect device matching, the even harmonics of the two drain currents combine in phase, while the fundamental-frequency (f_0) and all odd harmonic components are canceled out. This eliminates the need for implementing a broadband fundamental-frequency short circuit at the output for fundamental suppression and makes PPFD more compact and superior to other multipliers in terms of harmonic rejection. The block diagram of Fig. 2 allows to better understand the PPFD principle of operation and its key limitations. The two transistors of the push-push pair are represented each with two blocks, a linear block $g_{m,1}v_{in}$ and a non-linear block $g_{m,2}v_{in}^2$, representing the first two terms of the transistor I-V characteristic large-signal polynomial expansion. Notice that $g_{m,1}$ and $g_{m,2}$ are to be intended as average values under large signal operation, not as small signal parameters. The non-linear blocks convert the input signal at f_0 into the output signal at $2f_0$ through the second-order nonlinear transconductance, $g_{m,2}$. The linear block β models the feedback due to the transistors gate-drain capacitance. The two transistors output signals are added up and converted to voltage by the load resonator impedance (Z_L). The optimum load impedance, for maximum power delivered to the load, is selected through a set of harmonic load-pull simulations at the output frequency, $2f_0$. The constant power contours on the Smith Chart for the device size reported in Table. I at an output frequency of 40 GHz are reported in Fig. 3. The optimum impedance is around $Z_{opt} = 28.8 + j18.4\Omega$, corresponding to a 253 pH inductance in parallel with a 40.5Ω resistance. This low impedance value can be explained considering the effect

of the feedback loop. In fact, the output voltage signal at $2f_0$ is fed back to the input through the voltage divider formed by the transistors gate-drain capacitance and the common-mode gate impedance. This feedback results in a nonzero second-harmonic voltage swing at the gates that is amplified by $g_{m,1}$ and appears as a second-harmonic current at the output that subtracts from the one generated by the second-order nonlinearity [4]-[18], lowering the output signal level. Since the feedback signal is only common-mode and, therefore, it does not alter the differential input signal driving the $g_{m,2}$ blocks, the effect of the feedback can be modelled as a loading impedance Z_p in parallel with the load. The feedback factor β is given by the ratio between the gate and drain voltage:

$$\beta = \frac{v_g}{v_d} = \frac{Z_G}{Z_G + Z_{C_{gd}}} \tag{1}$$

where Z_G is the impedance at the gate node and $Z_{C_{gd}}$ the impedance associated to the gate-drain capacitance. For this doubler configuration, considering $Z_G = R_s//Z_{C_{gs}}$, with R_s signal source resistance, the loading impedance Z_p is:

$$Z_p = \frac{1}{\beta 2 g_{m,1}} = R_p + \frac{1}{sC_p} \tag{2}$$

where $R_p = (1/2g_{m,1})(1 + C_{gs}/C_{gd})$ and $C_p = 4C_{gd}(g_{m,1}R_s)$. For frequencies close to f_0, $\beta \approx C_{gd}/(C_{gd} + C_{gs}) = \beta_0$ and $Z_p \approx R_p$. Notice that C_{gd} capacitors are connected between the inputs and the output of the push-push pair, which is a virtual ground for the signal at f_0. Hence, they appear virtually in parallel to the C_{gs} capacitors in the calculation of β. This low Z_p impedance limits the maximum output swing to much less than the supply (0.5 V). Hence, the maximum power to the load corresponds to the conjugate matching condition, i.e. the real part of Y_{opt} is roughly equal to $1/R_p$. Optimizing device sizing and biasing, the undesired effects generated by the feedback can be minimized. Nonetheless, the doubler efficiency remains limited. The "PPFD" column of Table I summarizes the simulated results, where power conversion gain is expressed as: $CG = P_{out}(2f_0)/P_{in}(f_0)$ and power efficiency is expressed as $\eta_d = P_{out}(2f_0)/P_{DC}$.

III. Push-Push Frequency Doubler (PPFD) Design

To improve power conversion gain and power efficiency, an harmonic reflector (HR) can be introduced at the frequency doubler input. The reflector makes Z_G as small as possible around $2f_0$, ideally short-circuiting the common-mode component of signals at the gates around the second-harmonic to ground, thereby eliminating the feedback. The short is usually achieved adding a series-resonant LC network or a transmission line stub (either a $\lambda/2$ short stub or a $\lambda/4$ open stub [18]) in parallel to the matching network. The HR lumped implementations are reported in Fig. 1. A differential inductor (L_{in}) with a capacitor (C_{cm}) connected to its center-tap (Fig. 1.b) or two capacitors ($C_{s,cm}$) and one common-mode inductor (L_{cm}) (Fig. 1.c) can be used, with nearly identical results at f_0 = 20 GHz. The optimum impedance for maximum power transfer has been evaluated with a load-pull analysis. The simulation results, reported in Fig. 4, show an optimum load

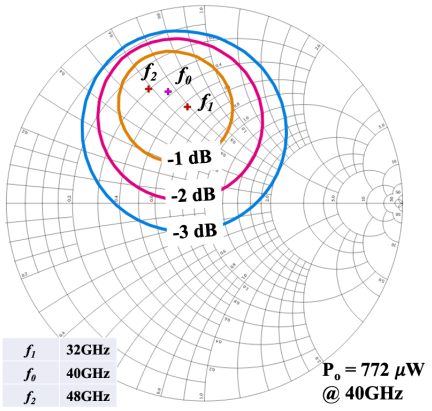


Fig. 4. Constant output power contours on the Smith Chart (LC resonator-based harmonic reflector). The dots beside f_0, f_1 and f_2 are the impedances at which the maximum power transfer to the load is achieved at the corresponding frequencies. The input signal has a peak voltage of $V_{in} = 450mV_p$ (single-ended) at 20 GHz

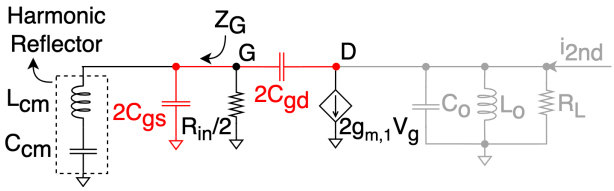


Fig. 5. Push-push doubler common mode equivalent model.

impedance given by $Z_{opt} = 18.8 + j32.8\Omega$, corresponding to a 173.6 pH inductance in parallel with 76.2Ω resistance. It is worth noticing that, thanks to the higher output impedance, the optimum load resistance is almost doubled compared to the case without the HR and this enables a larger output voltage swing. The "LC resonator-based" column of Table I contains the main simulation results of this configuration. Compared to the PPFD structure, output power and DC-RF efficiency are improved by a factor of three, while the DC power consumption doesn't change significantly.

A. LC-Based Harmonic Reflector PPFD

The introduction of the reflector, however, results in an increase of area occupation and a reduction of the maximum achievable bandwidth. In fact, if the HR implementation in Fig. 1.c is chosen, the differential capacitance increases due to the capacitors $C_{s,cm}$, resulting in a smaller matching bandwidth. The implementation in Fig. 1.b looks more promising, since the same inductor L_{in} can be used for both the input matching network and the HR, leaving the differential input matching bandwidth unchanged (compared to the circuit without HR). Hence, we assume that L_{in} is chosen accordingly such that it resonates the differential input capacitance $C_{diff} = (C_{gs}/2 + C_{gd}/2)$ (around 12.5fF + 15fF = 27.5fF in our first doubler) at the desired center frequency f_0. The design and operation of the HR are illustrated with reference to the equivalent common-mode circuit in Fig. 5, where R_{in} models the source resistance and the losses of the passive components. To create a common-mode short at $2f_0$,

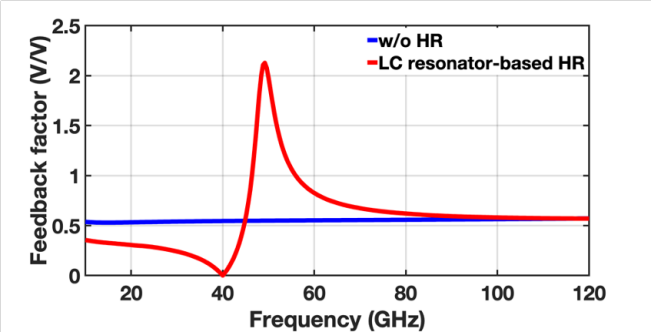


Fig. 6. Simulated feedback factor β using (8) in the case without harmonic reflector (blue curve) and with LC-base harmonic reflector (red curve).

the common-mode capacitance C_{cm} must resonate with the common-mode inductance ($L_{cm} = L_{in}/4$). This, however, leads to a small C_{cm}, roughly equal to C_{diff}, an high network quality factor, and a narrow frequency range of effectiveness of the HR. This can be verified by comparing the β factor with and without LC-resonator-based HR, as reported in Fig. 6. For the PPFD without the harmonic reflector, β remains equal to about 0.5 over the entire frequency range, meaning that half of the second harmonic output voltage appears at the gates of the PPFD transistors. The HR makes β nearly zero around $2f_0$ (here 40 GHz). For frequencies below $2f_0$, the HR impedance can be approximated as a capacitor C_{cm}, hence the feedback factor is only slightly reduced with respect to β_0:

$$\beta \simeq \frac{C_{gd}}{C_{gd} + C_{gs} + \frac{C_{cm}}{2}} \tag{3}$$

For frequencies well above $2f_0$, the HR impedance can be approximated as an inductance $L_{in}/4$, whose impedance will be much higher than the doubler input capacitance. Hence β is close to β_0, i.e. the same as the one of the circuit without reflector. However, the circuit presents a parallel resonance at a frequency only slightly higher than the series resonance, where the HR resonates with the doubler input common-mode capacitance $2C_{gs} + 2C_{gd}$, leading to a sharp peak in β (at around 49 GHz in Fig. 6). This peak corresponds to a minimum in the output loading impedance Z_p, which is responsible for a reduced doubler bandwidth. To enlarge the frequency range where the HR is effective, a much larger C_{cm} is required, but this would require a much smaller L_{in} and, hence, a larger differential capacitance, thus reducing the bandwidth of the differential matching network circuit.

B. Transformer-Based Harmonic Reflector PPFD

To overcome the limitations of LC-based reflectors, a step-up transformer can be used to efficiently implement both the input matching network and the HR, as shown in Fig. 7. Using a step-up transformer the voltage at the secondary is increased, thus improving the harmonic conversion efficiency. It will be shown that using the transformer to also implement the HR improves the performance compared to prior works [22] where a transformer and a separate LC-based HR are used. The transformer-based matching network can be modeled for differential and common-mode signals as shown in Fig. 8. It

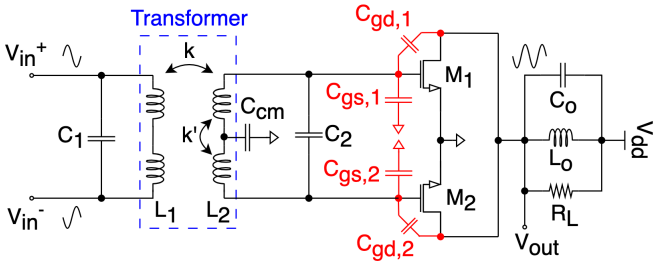


Fig. 7. Proposed transformer-based frequency doubler. The input signal has a peak voltage of $V_{in} = 450mV_p$ (single-ended) at 20 GHz

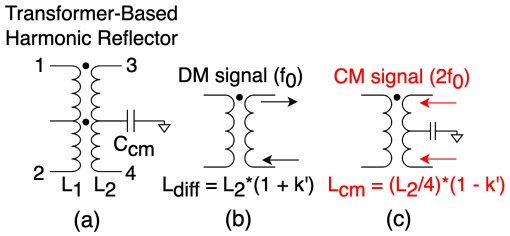


Fig. 8. Proposed transformer-based harmonic reflector (a) and equivalent circuit for (b) differential-mode and (c) common-mode signals.

is assumed here that the transformer secondary has multiple windings, with mutual coupling coefficient k'. The differential secondary inductance ($L_{diff} = L_2(1+k')$) is much larger than the common-mode inductance ($L_{cm} = L_2(1-k')/4$). This allows to independently maximize the matching bandwidth as well as the HR bandwidth. Imposing resonance of the differential capacitance C_{diff} with L_{diff} at f_0 and of the common-mode capacitance C_{cm} with L_{cm} at $2f_0$, results in a common-mode capacitance C_{cm} that is roughly equal to $C_{diff}(1+k')/(1-k')$, a much larger value compared to the LC-based HR. The maximum output power has been found out from the load-pull analysis, as reported in Fig 4. The optimum output impedance is around $Z_{opt} = 18.8 + j32.8\Omega$, which is the same as the one with the HR implemented through an LC resonator. The bandwidth where the HR is effective, however, is much greater than with the LC-based HR. For frequencies above $2f_0$ the HR impedance can be approximated as a small inductance L_{cm}. As a consequence, the peak of the β factor is reduced and pushed to higher frequencies. Fig. 9a shows the simulated β as a function of frequency for the three configurations. The dashed curve reports the calculations based on the equivalent common-mode circuit of Fig. 5 using the expressions reported in Appendix A and the component values extracted from the transformer-based circuit, which closely matches the actual circuit simulations. The HR has an inductive impedance above the series resonance, which is responsible for a sharp peak in the β factor, leading to a reduction of the doubler bandwidth in the LC-based HR case. The proposed transformer-based solution pushes the parallel resonance at a much higher frequency, since the equivalent common-mode inductance is very low. As a result, the HR is effective for a much broader bandwidth, spanning more than two octaves.

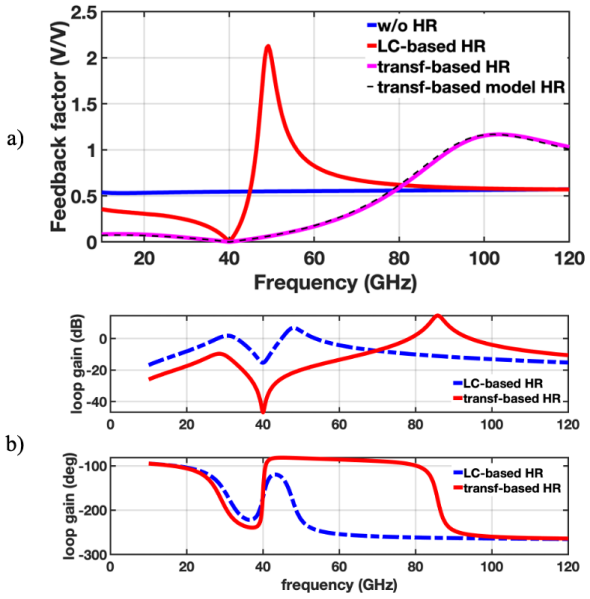


Fig. 9. Feedback factor β simulations (solid line) and calculations (dashed line) using (8) of the feedback factor β in various cases; and (b) loop gain (magnitude and phase) as a function of frequency of the push-push frequency doubler with HR.

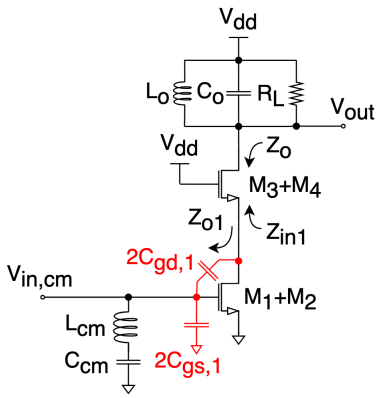


Fig. 10. Common mode equivalent circuit of the frequency doubler with CG amplifier stage.

C. Stability Considerations

We can analyze stability in a push-push frequency doubler with reference to Fig. 9b and Fig. 10. Let us initially consider the frequency doubler without common-mode HR, i.e. the gate impedance Z_G is simply given the gate capacitance $2C_{gs}$. In this case, gate-drain and gate-source capacitance form a simple capacitive attenuator and the feedback factor β is a positive real number. The circuit around the push-push transistors forms a negative feedback loop with a phase margin of at least 90 degrees, ensuring stability. Let us now consider the effect of the HR and assume, for simplicity, that its impedance dominates with respect to the gate-source capacitance. At frequencies below the HR series resonance, the HR impedance is capacitive and the circuit forms again a negative feedback loop. Above the HR series resonance frequency the feedback loop reverts its phase, becoming positive and potentially unstable. It can be easily shown that the input impedance seen at the gate of the transistors through the feedback capacitance has a negative (positive) real part when the impedance at their drain is inductive (capacitive). Hence, if the impedance at the gate is inductive and the impedance at the drain is also inductive, self-oscillations are possible. In fact, a transistor with an inductance L_g at the gate, an inductance L_d at the drain and a capacitive feedback C_{gd} between gate and drain forms an Hartley oscillator, with oscillation frequency given by $\omega_{osc} = 1/\sqrt{C_{gd}(L_g + L_d)}$. In a push-push doubler, however, the HR and the load impedance resonate at the same frequency. Below their resonance frequency the gate impedance is capacitive and the drain impedance is inductive. Above their resonance frequency the situation is reversed, hence the conditions for self-oscillations are never met. Analysing the circuit, it can be seen that the loop gain (see Fig. 9.b) shows two peaks, one below and one above the HR resonance frequency (40 GHz in Fig. 9.b). The low frequency resonance is formed between the load inductance and the sum of the load capacitance with the series of the gate-drain and gate-source capacitance. The high frequency resonance is formed between the gate inductance and the series of the gate-source, gate-drain and load capacitors. In Fig. 9.b both an LC and a transformer-based HR are considered. In the case of the transformer-based HR, due to the smaller HR inductance, the high frequency peaks occurs at a much higher frequency. In all cases the loop creates a positive real part impedance at the gate and the phase of the loop at resonance is 180 degrees. When a cascode is added, as in Fig. 10, the load impedance becomes resistive and stability improves. In summary, a PPFD with an LC-based or a transformer-based HR behave similarly from the stability point of view and are not prone to self-oscillation.

D. Transformer-Based Harmonic Reflector PPFD Stacked with Common-Gate Amplifier

The PPFD with HR still suffers from a limited output power, mainly because second-harmonic generation is a process with lower current efficiency compared to a simple amplifier. Moreover, the PPFD, even with HR, has a low output impedance. In fact, due to the low current efficiency, to obtain a given signal current, a larger device is required, leading to a lower output impedance and a low maximum voltage swing. Using a transformer-based HR, improved efficiency is obtained for a relatively low supply voltage (0.5 V for the design in Fig. 7), but the output power remains limited. A cascode transistor, Fig. 11, can be added to boost the available output power and improve power efficiency thanks to current reuse. A matching network could be added between the push-push and the CG stage to further extend the bandwidth and enhance the power efficiency as in [23], at the price of increased area occupation. Analyzing the common-mode equivalent circuit, Fig. 10, the CG lowers the impedance seen by the PPFD (Z_{in1}) and increases the output impedance (Z_o) by the CG self-gain, thus reducing the effect of the limited PPFD output impedance (Z_{o1}) and allowing the use of a larger load resistance R_L. All the second-harmonic current coming from the push-push cell flows into the CG stage and then into the load R_L, generating a larger output voltage swing. The push-push core

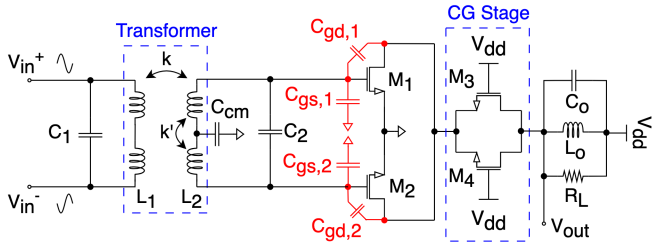


Fig. 11. Transformer-based frequency doubler with the Common-Gate stage stacked on top. The input signal has a peak voltage of $V_{in} = 450mV_p$ (single-ended) at 20 GHz

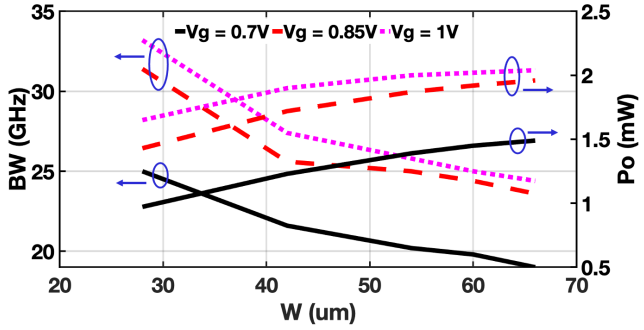


Fig. 12. Simulated bandwidth and output power of the first doubler with Transformer-Based HR as a function of the CG transistor width, W, for a different gate bias voltages.

and the associated feedback factor β due to the gate-drain capacitance remains essentially the same, hence the use of a transformer-based HR gives similar advantages as with the push-push doubler without CG. The CG device sizing and biasing need to be optimized with respect to output power and bandwidth. A large device transconductance is desirable to increase the output impedance and available power, but this comes at the cost of an increased output capacitance. The gate voltage biasing must be sufficiently high to leave enough voltage headroom to the push-push core, while keeping all transistors in saturation. Fig. 12 shows how the output power increases and the bandwidth decreases as the CG transistor width, W, is made larger for a fixed push-push core. In addition, the larger the CG gate voltage V_g, the higher the output power and efficiency. Hence, V_g was set to the supply voltage of 1V and the transistor width was set to $42\mu m$ as a compromise between bandwidth and output power (Fig. 12) Based on the load-pull analysis, the constant output power contours on the Smith Chart are reported in Fig. 13. In this design, the optimum output impedance is $Z_{opt} = 50\Omega + j84\Omega$, corresponding to a 452 pH inductance in parallel with a 191.3Ω resistance. Table I reports the performance summary to compare the four cases. Here, as expected, the optimum load resistance and the corresponding output voltage swing are further increased compared to the previous configurations. Due to the stacked transistor configuration, the supply voltage has been increased to 1V. The presence of the CG stage improves the performances of the frequency doubler in terms of output

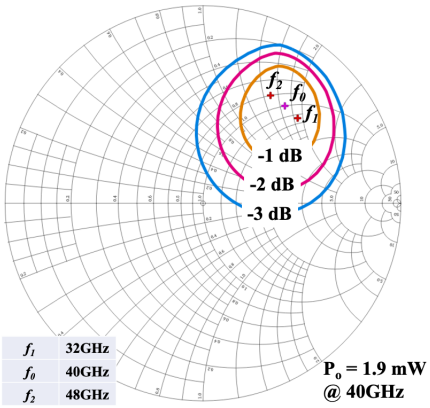


Fig. 13. Constant output power contours of the PPFD with Transformer-based HR with Common-Gate amplifier. The dots beside f_0, f_1 and f_2 are the impedances at which the maximum power transfer to the load is achieved at the corresponding frequencies. The input signal has a peak voltage of $V_{in} = 450mV_p$ (single-ended) at 20 GHz.

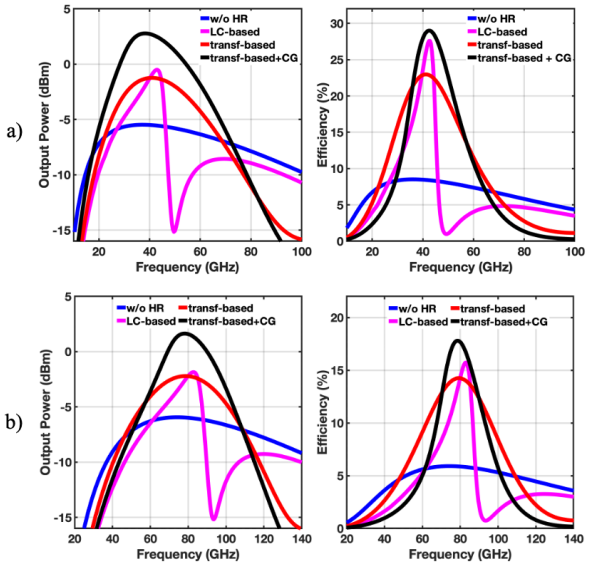


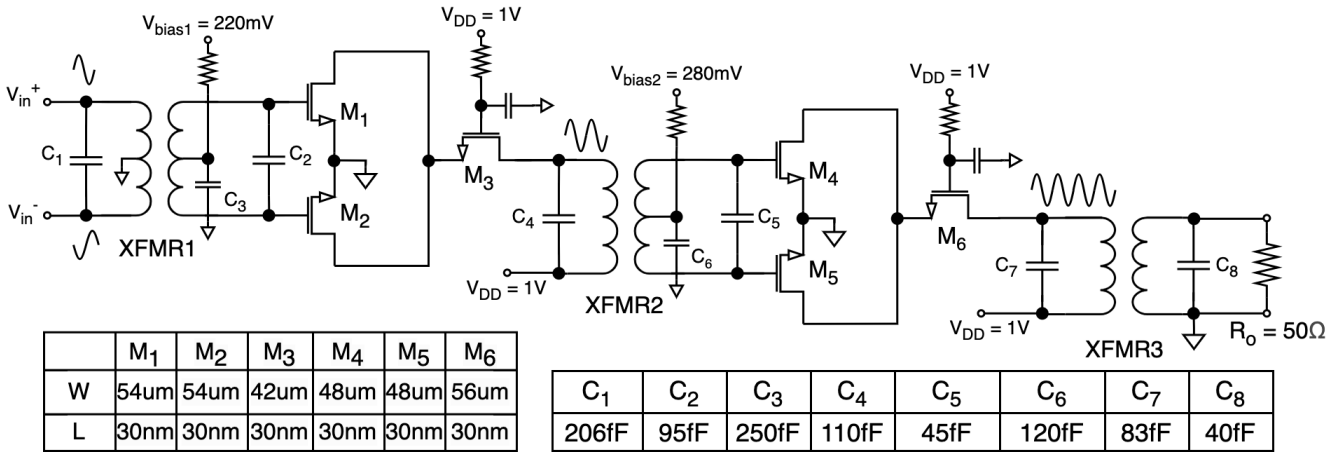
Fig. 14. Simulation of a) the first doubler saturated output power (left) and efficiency (right) and b) the second doubler saturated output power (left) and efficiency (right) as a function of output frequency of the four cases for a fixed input voltage of $450mV_p$ single-ended at 20 GHz and 40 GHz the first and second doubler respectively.

power and drain efficiency. The high output voltage swing is enough to directly drive the second doubler of the quadrupler chain. Fig. 14 compares the output power and efficiency as a function of frequency for the four designs analyzed above. The PPFD without HR has the broadest bandwidth, but a very low peak output power and efficiency. Using the LC-based HR, peak output power and efficiency are improved at the price of a much reduced bandwidth. The transformer-based HR improves the bandwidth, while keeping the peak power and efficiency nearly unchanged. Introducing the cascode stage in the PPFD with transformer-based HR improves both peak output power and efficiency, with a small bandwidth improvement.

TABLE I
COMPARISON BETWEEN PPFD, LC RESONATOR-BASED PPDF, TRANFORMER-BASED PPDF AND TRANFORMER-BASED PPDF WITH CG.

Parameter	PPFD	LC resonator-based PPFD	Transformer-based PPFD	Transformer-based PPFD with CG
W/L	$54\mu m/30nm$	$54\mu m/30nm$	$54\mu m/30nm$	$54\mu m/30nm$
V_{DD}	0.5 V	0.5 V	0.5 V	1 V
V^*_{bias}	220 mV	220 mV	220 mV	220 mV
R_L	40.5Ω	76.2Ω	76.2Ω	191.3Ω
i_{out}	$3.7mA$	$4.5mA$	$4.4mA$	$4.4mA$
v_{out}	$151mV_p$	$342mVp$	$338mV_p$	$844.7mV_p$
P_{out}	$282.8\mu W$	$771.5\mu W$	$760\mu W$	$1.9mW$
P_{DC}	$3.3mW$	$3.3mW$	$3.3mW$	$6.2mW$
η	8.5%	23.6%	23%	28%
BW	70 GHz	11 GHz	34 GHz	27 GHz

* Bias voltage of the push-push doubler common-source stage.



	M_1	M_2	M_3	M_4	M_5	M_6
W	54um	54um	42um	48um	48um	56um
L	30nm	30nm	30nm	30nm	30nm	30nm

C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
206fF	95fF	250fF	110fF	45fF	120fF	83fF	40fF

Fig. 15. Complete schematic of the frequency quadrupler.

IV. FREQUENCY QUADRUPLER DESIGN

The complete schematic of the proposed frequency quadrupler is reported in Fig. 15. The frequency quadrupler was designed to operate in E-band, with an input frequency range centered around 20 GHz, driven by a differential oscillator with a phase noise of -114 dBc/Hz at 1 MHz offset [29]. The quadrupler consists of two cascaded PPFD with transformer-based HR that are directly connected, without interstage amplification stages, driving directly a 50Ω output load without additional power amplification stages. The transistors sizing and bias were optimized so that the second doubler would deliver a peak output power of 0 dBm. The design is implemented in a bulk 28 nm CMOS technology and has a single 1V supply voltage. All the capacitors at the primary and secondary windings of each transformer are intended to be equivalent capacitances at the corresponding nodes considering the parasitics as well. The quadrupler input connects through a 100Ω differential transmission line to the input pads. In this test chip the inputs of the first doubler are matched to 50Ω for testing purposes, but the input transformer is not designed and operated as a balun (with single-ended input) since in the complete system it is driven differentially by an on-chip oscillator.

A. Push-push Frequency Doubler Sizing and Biasing

In the push-push frequency doubler the transistors are excited such that they generate an output current which is rich of even harmonics of the input frequency. To better appreciate the design trade-offs involved in the transistors sizing and bias, a push-push pair driven by ideal voltage generators and loaded by a low impedance was simulated. Fig. 16 reports the simulated current efficiency (I_2/I_{DC}) (a) and second harmonic output current (b) as a function of input signal voltage amplitude for different bias voltages. Reducing the bias voltage the current efficiency increases(a), while the output current gets smaller (b). Biasing the transistors in deep class-C (e.g. with a 0 V gate bias as in [21]) maximizes the current efficiency, but the second harmonic current generated is quite small. This means that, to generate the desired output current, a very large transistor is required, which would increase the capacitance and reduce the bandwidth. If, instead, the transistor is biased near its threshold voltage more second harmonic current is generated, at the price of a much higher current consumption and lower current efficiency. On the other hand, a larger input amplitude is beneficial for both current efficiency and output signal level. In practice, the optimal transistor sizing and bias depends on the input voltage swing. Our quadrupler was optimized to be driven by an oscillator, providing an input amplitude of $450mV_p$ single-ended. In our design, the first doubler is biased with $220mV$, close to the

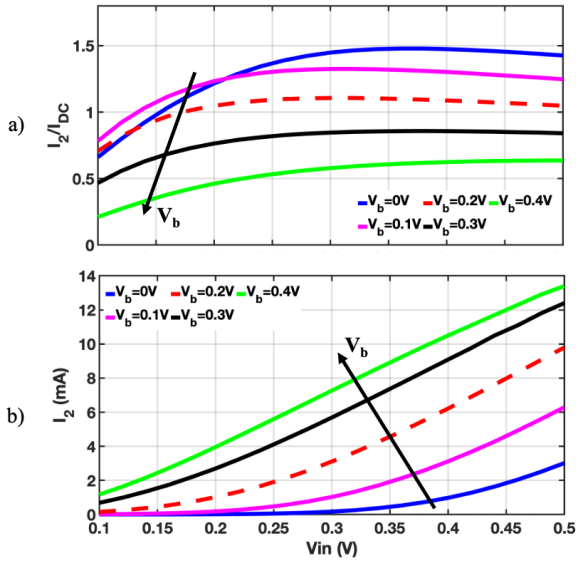


Fig. 16. Simulation of the a) current efficiency (I_2/I_{DC}) and b) second harmonic output current as a function of input voltage (peak single-ended) for different gate bias voltages V_b.

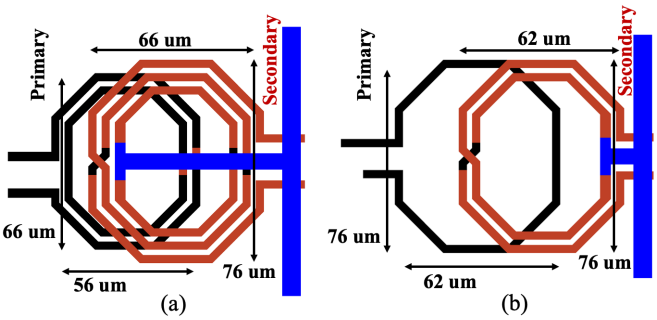


Fig. 17. Physical layout of the transformers used for the input matching network of (a) the first frequency doubler and (b) the second frequency doubler. The T-shaped lines in blue connect the secondary center-tap to the reflector capacitors.

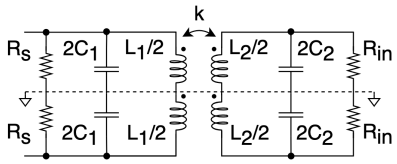


Fig. 18. Differential point of view of the transformer.

dashed curve in Fig. 16a, resulting in a current efficiency close to one. Transistors were sized based on the input power required by the following doubler, also taking into account for the losses and non-idealities of the transformer-based inter-stage matching network and HR, as discussed in the next sub-section. The second doubler bias voltage is a bit higher ($280mV$), allowing for an higher current density and a reduced device size considering the higher operating frequency, at the price of a slight reduction in current efficiency. The push-push core was sized to deliver a peak power of 1.8 mW at 80 GHz with an optimal load, as shown in Fig. 14. A coplanar transformer with single-turn inductors is used for the output matching network, that transforms the 50Ω load in a frequency-dependent impedance that is close to the optimum load impedance at 80 GHz, resulting in a PPFD core output power of 1.2 mW with a power dissipation of 11 mW. The power loss of the matching network, evaluated using the maximum available gain of the two-port is -1.4 dB, resulting in a 0.85 mW output power and an overall efficiency of the second PPFD, including all the losses and non-idealities, of 7.8%.

B. Transformer Differential Mode Analysis and Design

Transformer-based input matching networks and harmonic reflectors are implemented for the two doublers, as reported in Fig. 17. In both cases a step-up transformer is used in order to boost the effective voltage swing driving the push-push doubler gates. In Fig. 18, the differential equivalent circuit of the transformers is shown. From the transformers characterization, post-layout parameters have been derived, as reported in Table II. For the first transformer (XFMR1), R_s is the input port resistance and is set to 50Ω single-ended, while the differential capacitances, C_1 and C_2, resonate with the primary and secondary winding inductance at the input frequency of the doubler. For the second transformer (XFMR2), R_s represents the output resistance of the first PPFD, while the differential capacitances, C_4 and C_5, resonate with the primary and secondary winding inductance at the input frequency of the second doubler which is 40 GHz. R_{in} is the doubler input resistance. In both doublers, since R_{in} is big (in the order of $k\Omega$), the quality factor of the resonator at the secondary is much greater than one. The network shows two parallel resonances (f_L and f_H) and a series resonance (f_s) in-between. The resonances are sufficiently far from each other, such that, in the neighborhood of each resonance frequency, the network can be approximated as a parallel and a series LC resonator respectively [30]. Assuming $\omega_1^2 = (L_1C_1)^{-1}$ to be equal to $\omega_2^2 = (L_2C_2)^{-1}$ (as in our design), the two parallel resonances are:

$$\omega_L = \frac{\omega_1}{\sqrt{1+k}} \tag{4}$$

$$\omega_H = \frac{\omega_1}{\sqrt{1-k}} \tag{5}$$

TABLE II
TRANSFORMER PARAMETERS AT THE INPUT OF FIRST AND SECOND DOUBLER AND AT THE OUTPUT THE OF THE SECOND DOUBLER.

Parameter	First Transformer (@ 20 GHz)	Second Transformer (@ 40 GHz)	Third Transformer (@ 80 GHz)
$L_{diff,1}$	$307pH$	$138pH$	$93pH$
$L_{diff,2}$	$660pH$	$355pH$	$99pH$
k	0.4	0.25	0.7
Q_1	7.8	10.7	9.1
Q_2	12.2	17.4	8.1
L_{cm}	$60pH$	$31pH$	-
k'	0.45	0.48	-
G_{max}	$-2.8dB$	$-3dB$	$-1.4dB$

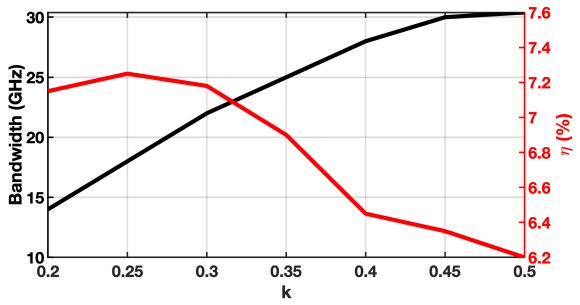


Fig. 19. Simulated second doubler output bandwidth and average efficiency as a function of the coupling coefficient of the input transformer.

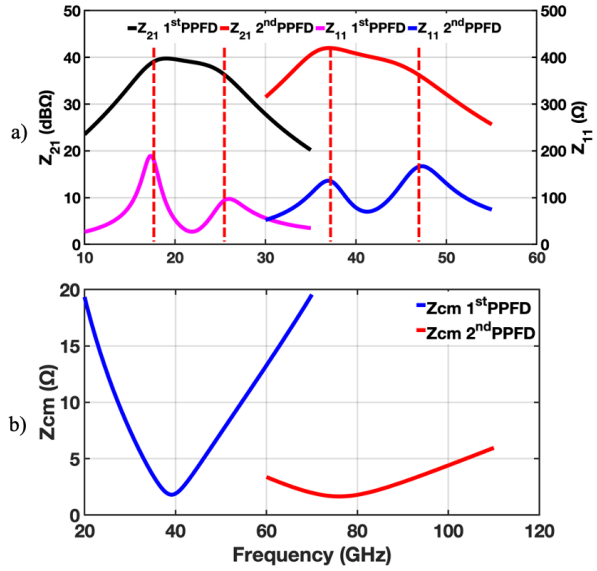


Fig. 20. Simulation of the a) first and second doubler transformer Z_{21} and Z_{11} as function of frequency and b) common-mode impedance Z_{cm} reported at half of the frequency.

The series resonance angular frequency ω_s is given by:

$$\omega_s = \sqrt{\omega_L \omega_H} \tag{6}$$

Offset between the primary and secondary windings of the transformers is used to control their coupling coefficient. By adjusting the coupling coefficient (k), the two parallel resonances can be made sufficiently close to each other in order to have broadband matching with reasonable in-band ripple, as shown by the simulated Z_{21} reported in Fig. 20. A small k results in a smaller bandwidth, but with a more flat gain and, therefore, an higher power efficiency averaged over the band. As opposite, a larger k leads to a wider bandwidth, but a lower average power efficiency. This sets a design trade-off between average efficiency and bandwidth, as reported in Fig. 19, which refers to the second doubler. We chose to favor bandwidth in the input transformer of the first doubler and efficiency in the second one. For the first transformer, the chosen k factor (0.4) enables to have $f_L = 17.5GHz$ and $f_H = 25GHz$, whereas for the second transformer, the k factor is 0.25 and $f_L = 36GHz$ and $f_H = 46GHz$. The series resonance frequencies are 21.8 GHz and 41 GHz for the first and second transformers, respectively. Fig. 20 shows the simulations of transimpedance, Z_{21}, and input impedance, Z_{11}, (a) and of the common-mode impedance Z_{cm} (b) of the first and second transformer as a function of frequency. The transimpedance gain remains almost constant in the 17.5 - 25 GHz and 36 - 46 GHz frequency range respectively. A 3-dB bandwidth of about 8 GHz is achieved around the center frequency of 21 GHz and 10 GHz around 40 GHz (a). Transformer losses were minimized following the detailed design procedure reported in [30]. The power loss of the first, second and third transformer was estimated using the two-port maximum available gain, which is -2.8 dB, -1.4 dB and -3 dB at 20 GHz, 40 GHz and 80 GHz respectively. The input impedance, Z_{11}, reported in Fig. 20a, shows a minimum at the series resonance frequency and peaks at the parallel resonance frequencies. As the frequency separation between the two parallel resonances is increased to widen the bandwidth, the variation of Z_{11} across the band increases. This makes it difficult to provide an optimum load impedance to the first PPFD, thus reducing its power efficiency. Adding to this, the first doubler was designed to exceed the saturation level of the following doubler in order to keep the quadrupler output power constant over a wider bandwidth. Table I shows the simulated results considering an optimum load for each doubler. If the doublers are loaded with the real load provided by the transformer, the output power level becomes 0.54 mW and 0.85 mW for the first and second doubler respectively (transformer losses included). The first doubler power dissipation increases from 6.2 mW in Table I to 7.3 mW and, for the second doubler, from 10 mW to 11 mW, leading to an efficiency of 7.4% and 7.8% for the first and second doubler respectively. The combination of the two results in an overall efficiency of 4.7%.

C. Transformer Common-Mode Analysis

From the common-mode point of view, the transformers were designed in order to implement an efficient HR. With reference to Fig. 7, the multi-turn secondary winding configuration sets the self-coupling coefficient k'. In this design, k', can be adjusted by changing different parameters such as spacing between the coil turns, width and number of turns. In particular, decreasing the distance between the turns, k' gets stronger; increasing the width and the number of turns, k' gets stronger due to the greater mutual induction. In the proposed transformers, the aim was to find a reasonably high value of k' that enable us to minimize the common-mode inductance, L_{cm} (and maximize the differential inductance), while keeping the layout of the transformer as compact as possible:

$$L_{cm} = \frac{L_2}{4}(1 - k') \tag{7}$$

The k' value has been verified with the aid of EM simulations. The value of k' is also quite stable versus process and temperature, which helps ensuring that the HR series resonance tracks the differential mode resonance frequency. The first transformer has a differential secondary inductance of 660 pH and a common-mode inductance of 60 pH (Table II). The second transformer has a differential secondary inductance of 355 pH and a common-mode inductance of 31 pH (Table II). The small common-mode secondary inductance resonates

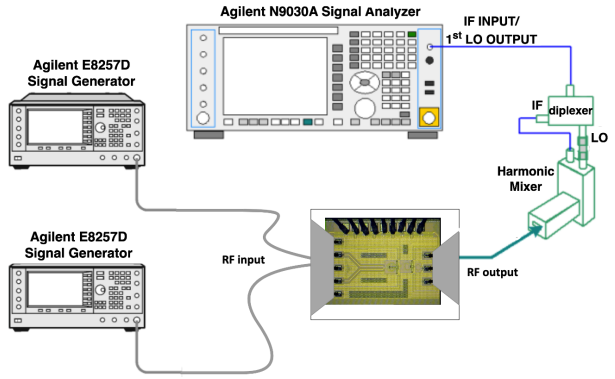


Fig. 21. Measurement setup for measuring the desired 2^{nd} harmonic and suppression of the spurious harmonics.

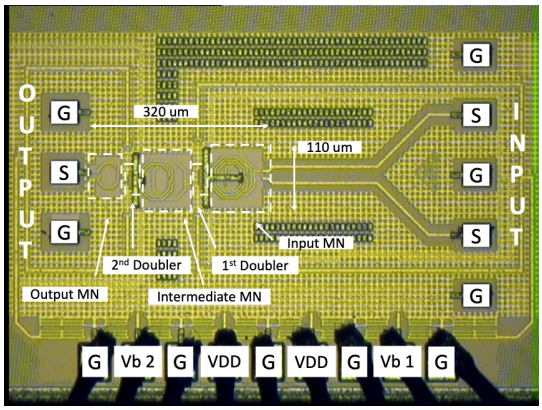


Fig. 22. Chip microphotograph.

a bigger common-mode capacitance, enabling the reduction of the Q-factor of the HR, thus improving its bandwidth. In Fig. 20b the common-mode impedance Z_{cm} of the HR of the two frequency doublers is reported as a function of frequency. For both structures Z_{cm} has a minimum at the corresponding doubler output center frequency, i.e. 40 GHz and 80 GHz respectively, and it remains small over the whole band.

V. Measurement Results

The measurement setup is shown Fig. 21. The differential input signal to the quadrupler is provided by two signal generators (Agilent E8257D) that are locked to each other in order to generate a differential signal. The desired single-ended output signal at four times the input frequency is measured through a spectrum analyzer (Agilent N9030A, working up to 50 GHz) and an harmonic mixer used to down-convert the quadrupler output signal to a lower frequency. Two different harmonic mixers have been used: one covers 50 GHz - 75 GHz frequency range (Agilent 11970V for V-band) whereas the other one covers 75 - 110 GHz frequency range (Agilent 11970W for W-band). This enables to extend the operating bandwidth of the spectrum analyzer covering an overall frequency range from 50 to 110 GHz. The chip microphotograph is reported in Fig. 22. The chip area is 0.69 mm^2, whereas the core area (excluding the input transmission line and the bonding pads) only occupies 320 μm by 110 μm. The DC

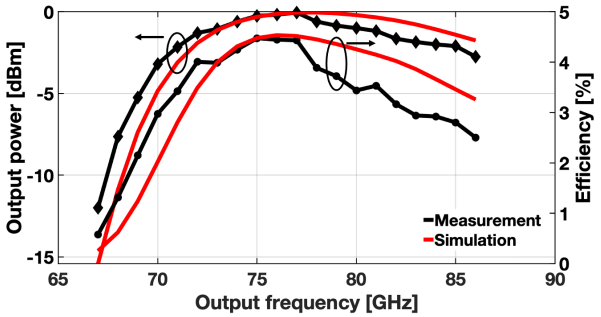


Fig. 23. Measured and simulated quadrupler fourth harmonic output power and efficiency as a function of frequency for P_{in} = 0 dBm.

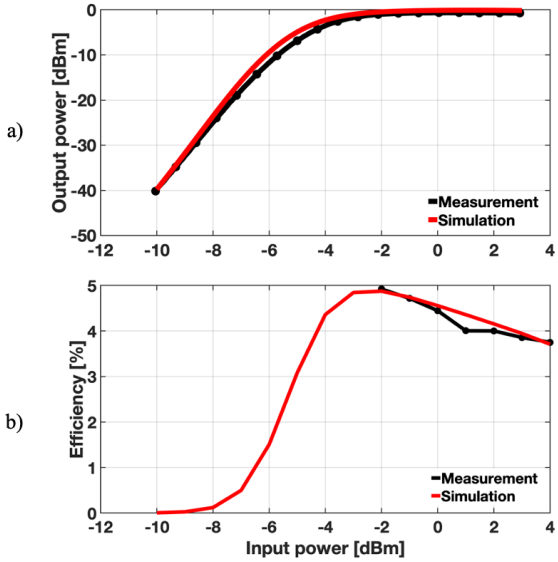


Fig. 24. Measured and simulated a) P_{out} as a function of P_{in} and b) efficiency as a function of P_{in} at 76 GHz.

pads are directly wire-bonded to the PCB whereas both the input and output high-frequency pads are accessed with on-wafer probing. The measured and simulated quadrupler output power (P_{out}) and efficiency as a function of output frequency for a fixed input power (P_{in}) of 0 dBm is reported in Fig. 23. P_{out} reaches a peak of 0 dBm at 77 GHz and is kept within 3-dB variation from 70 GHz up to 86 GHz. Measurements agree well with simulations, showing a down-shift of the characteristic by approximately 1 GHz. A peak quadrupler efficiency of 5% is achieved for P_{in} = -2 dBm. The measured and simulated P_{out} and efficiency at 76 GHz, as a function of P_{in} is reported in Fig. 24. The measurements agree very well with simulations showing less than 1 dB variation for P_{in} going from -2 dBm up to 4 dBm. Fundamental and second-harmonic output power levels are compared to the fourth harmonic power in Fig. 25. Better than 40 dB second harmonic rejection (SHR) and 60 dB fundamental rejection (FRR) was measured across the whole bandwidth, in good agreement with simulations. According to simulations, the quadrupler exhibits a phase noise in the range between -152 dBc/Hz and -158 dBc/Hz across the covered frequency band for an input power

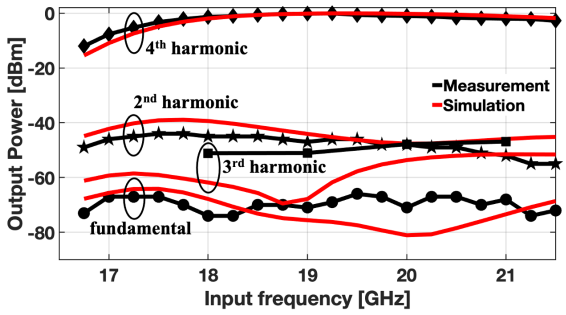


Fig. 25. Measured and simulated Pout at the fundamental, second, third and fourth harmonics as a function of output frequency for P_{in} = 0 dBm.

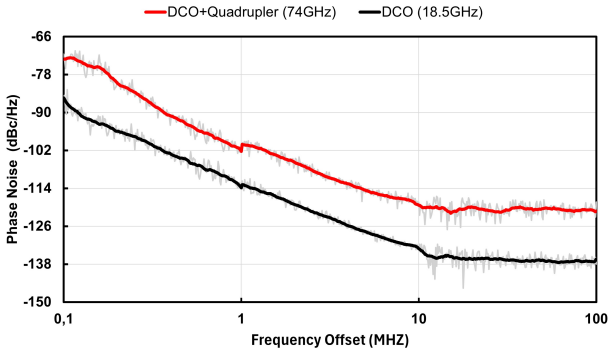


Fig. 26. Phase noise measurements of the DCO + Quadrupler at 74 GHz (red) and DCO at 18.5 GHz (black).

of 0 dBm. The phase noise of the quadrupler was tested when driven by an on-chip oscillator and the measurement results are reported in Fig. 26. More details on the oscillator design can be found in [29]. After frequency multiplication by four, the phase noise increases, as expected, by approximately 12 dB, confirming that the phase noise contribution of the quadrupler is negligible. Notice that, with a carrier power of -29 and -13 dBm for the quarupler and oscillator outputs respectively, at frequency offsets larger than 10 MHz the noise measurements are dominated by the spectrum analyzer own noise, i.e. -150 dBm/Hz. Considering the oscillator and the frequency quadrupler the overall power dissipation is 44 mW, resulting in a DC-to-RF power conversion efficiency of 2.3%. This compares favorably to other CMOS works with similar frequencies and phase noise level, such [31], reporting a peak DC-to-RF efficiency of 0.7%. A summary of the measured performance is reported in Table III and compared with state-of-the-art quadrupler implementations covering a similar frequency range. The proposed solution achieves a peak power efficiency of 5% and a fractional bandwidth of 20.8%, which is equal or better then prior CMOS implementations, except for [13]. However, [13] has limited 3rd and 5th harmonic rejection, and consumes a large power, two third of which are used in the output buffer. For a fair comparison, please notice that the other works in the table except for [32] and [33] have a single-ended input, which might negatively affect the reported harmonic rejection. [34] has the second highest reported efficiency in CMOS when considering the output buffer. Notice, however, that the power efficiency in [34] drops to 2.5% without the output buffer. Moreover, a much lower input power is required in our design, which is desirable since it saves power from the driving stage. In [15] a bipolar implementation reports a much wider bandwidth, but with poor power efficiency and very high power dissipation. Finally, the proposed design occupies the smallest die area.

VI. Conclusion

The design of a compact E-band frequency quadrupler implemented by cascading two frequency doublers without additional power amplification stages is proposed in this work. Both frequency doublers adopt a cascoded push-push structure with a second-harmonic reflector for power efficiency enhancement. The proposed reflector re-uses the secondary windings of the transformer used for the input matching network, resulting in 2.2 dB higher output power (66% higher power efficiency for a single push-push doubler) without area or bandwidth penalties. The quadrupler achieves an output power of 0 dBm at 76 GHz with 5% peak efficiency and has a 3-dB bandwidth from 70 to 86 GHz (20.8% fractional bandwidth), improving over prior CMOS implementations.

VII. Acknoledgement

This work was supported by Huawei Technology Co.

VIII. Appendix A

The calculation of the feedback factor is based on the equivalent common-mode circuit in Fig. 5. From inspection of the circuit we can directly calculate $\beta = v_g/v_d$:

$$\beta = \frac{2sC_{gd}(1+s^2L_{cm}C_{cm})}{sC_{cm}+[2s(C_{cm}+C_{gs})+\frac{2}{R_{in}}](1+s^2L_{cm}C_{cm})} \quad (8)$$

We assume that L_{cm} and C_{cm} resonate at $2\omega_0$, when the differential mode resonance is ω_0. For angular frequencies below $2\omega_0$ the HR can be approximated with C_{cm} ($Z_{HR} \simeq 1/sC_{cm}$), hence β is expressed as:

$$\beta = \frac{sR_{in}C_{gd}}{1+sR_{in}(\frac{C_{cm}}{2}+C_{gd}+C_{gs})} \simeq \frac{C_{gd}}{C_{cm}/2+C_{gd}+C_{gs}} \quad (9)$$

Well above $2\omega_0$ the HR can be approximated with L_{cm} ($Z_{HR} \simeq sL_{cm}$), hence β is expressed as:

$$\beta \simeq \frac{C_{gd}}{C_{gd}+C_{gs}} \quad (10)$$

The complex poles in (8) result from the parallel resonance between L_{cm} and the series between C_{cm} and $2(C_{gs}+C_{gd})$ at the angular frequency ω_p:

$$\omega_p = \sqrt{\frac{C_{cm}+2C_{gd}+2C_{gs}}{L_{cm}C_{cm}2(C_{gd}+C_{gs})}} \quad (11)$$

In the LC resonator-based HR (Fig. 1), C_{cm} = $C_{d,in}$ = (C_{gs} + C_{gd})/2 and ω_p is close to $2\omega_0$. In the transformer-based harmonic reflector (Fig. 7), the expressions of β remain the same, but with a smaller $L_{cm} = L_2(1-k')$ and a much larger $C_{cm} = C_{diff}(1+k')/(1-k')$, pushing ω_p well above $2\omega_0$.

TABLE III
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER WORKS.

	This Work	[32]	[34]	[16]	[15]	[33]	[13]
Multiplier Type	**x4 cascaded push-push**	x4	Single-stage push-push	Cascaded push-push	x4	x4 cascaded Gilbert multiplier	Odd-Harm. Recycling
PA stage	**NO**	NO	YES	YES	YES	NO	NO
Technology	**28nm CMOS**	22nm FDSOI	40nm CMOS	40nm CMOS	120nm SiGe	130nm SiGe	40nm CMOS
V_{dd} [V]	**1**	0.8		1.5	2	3.3	0.9
$f_{out}[GHz]$	**70-86**	71-81	65.6-75.2	74-82	70-110	72-80	62-92
$BW_{-3dB}[\%]$	**20.8**	14.8	13.6	10.2	44.4	10.5	39
$P_{out}@P_{in}[dBm]$	**0 @ 3**	3.1 @ 0	-0.2 @ 8.9	1.7 @ 3	3 @ 0	-4 @ 0	11 @ 13
$P_{DC}[mW]$	**20**	70	11.4	34	170-240	57	101.5
Peak $\eta^*_{DC}[\%]$	**5**	2.9	5 (2.5†)	4.4	1.2	0.7	12.4
Harmonic Rejection [dB]	**1st>60 2nd>40 3rd>47**	35	1st 45 2nd 30	1st 45 2nd 20	>30	N/A	1st> 44.5 2nd> 44.7 3rd> 26.3 5th> 28
Chip Area $[mm^2]$	**0.69 (0.03$^+$)**	0.38	0.1	0.92	1.9	0.2**	0.266

* $\eta_{DC} = P_{out}/(P_{DC} + P_{in})$; † without buffer; **estimate from chip photo; $^+$core chip area

REFERENCES

[1] Y. -S. Yeh, W. Wang and B. A. Floyd, "75–86 GHz Signal Generation Using a Phase-Controlled Quadrature-Push Quadrupler Driven by a QVCO or a Tunable Polyphase Filter," in IEEE Transactions on Microwave Theory and Techniques, vol. 69, no. 10, pp. 4521-4532, Oct. 2021.

[2] M. A. Shehata, V. Roy, J. Breslin, H. Shanan, M. Keaveney and R. B. Staszewski, "A 32–42-GHz RTWO-Based Frequency Quadrupler Achieving >37 dBc Harmonic Rejection in 22-nm FD-SOI," in IEEE Solid-State Circuits Letters, vol. 4, pp. 72-75, 2021.

[3] J. Zhang, Y. Peng and K. Kang, "Analysis and Design of High-Harmonic-Rejection Multi-Ratio mm-Wave Frequency Multipliers," in IEEE Journal of Solid-State Circuits, vol. 57, no. 1, pp. 260-277, Jan. 2022.

[4] Juo-Jung Hung, T. M. Hancock and G. M. Rebeiz, "High-power high-efficiency SiGe Ku- and Ka-band balanced frequency doublers," in IEEE Transactions on Microwave Theory and Techniques, vol. 53, no. 2, pp. 754-761, Feb. 2005.

[5] Y. Ding, Y. Shen, Z. Lin and S. Hu, "A Compact 24.5–32.6 GHz CMOS Frequency Doubler Based on Coupled Inductor," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 71, no. 5, pp. 2609-2613, May 2024.

[6] G. Liu, J. Jayamon, J. Buckwalter, and P. Asbeck, "Frequency doublers with 10.2/5.2 dBm peak power at 100/202 GHz in 45nm SOI CMOS," in 2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Phoenix, AZ, USA: IEEE, May 2015, pp. 271–274.

[7] Z. Yang, K. Ma, F. Meng and B. Liu, "A 120-GHz Class-F Frequency Doubler With 7.8-dBm POUT in 55-nm Bulk CMOS," in IEEE Journal of Solid-State Circuits, vol. 58, no. 8, pp. 2173-2188, Aug. 2023.

[8] X. Wu, Z. Kang, Y. Wang and L. Wu, "A 53–78 GHz Complementary Push–Push Frequency Doubler With Implicit Dual Resonance for Output Power Combining," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 70, no. 3, pp. 1202-1213, March 2023.

[9] J. Yoo and S. Hong, "Highly Efficient Differential Frequency Doubler With Output Resistance Boosting Feedback," in IEEE Journal of Solid-State Circuits, vol. 59, no. 2, pp. 414-423, Feb. 2024.

[10] W. Lee and A. Valdes-Garcia, "W-Band SiGe Frequency Doubler With Optimum Harmonic Termination for 14% Efficiency," in IEEE Microwave and Wireless Components Letters, vol. 31, no. 3, pp. 272-275, March 2021.

[11] S. G. Rao, M. Frounchi and J. D. Cressler, "Triaxial Balun With Inherent Harmonic Reflection for Millimeter-Wave Frequency Doublers," in IEEE Transactions on Microwave Theory and Techniques, vol. 69, no. 6, pp. 2822-2831, June 2021.

[12] K. Kim, K. Lee, K. Shin, G. Lee, S. Son, H. Cho, S. Song, Ho-Jin, "A 50-Gb/s Compact RadCom E-Band Transmitter With Phase-Controlled Push–Push Quadrupler and Stacked-FET Power Amplifier," in IEEE Solid-State Circuits Letters, vol. 4, pp. 150-153, 2021.

[13] Z. Lin, Y. Shen, Y. Ding and S. Hu, "19.2 A 12.4% Efficiency, 11dBm Psat, Odd-Harmonics-Recycling, 62-to-92GHz CMOS Frequency Quadrupler Using an Amplitude-Phase Coordinating Technique," 2024 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2024, pp. 350-352.

[14] W. Chung, C.-Y. Kim, S. S. Kim, and S. Hong, "Design of 94-GHz Highly Efficient Frequency Octupler Using 47-GHz Current-Reusing Class-C Frequency Quadrupler," IEEE Trans. Microwave Theory Tech., vol. 68, no. 2, pp. 775–784, Feb. 2020.

[15] B. -H. Ku, H. Chung and G. M. Rebeiz, "A Milliwatt-Level 70–110 GHz Frequency Quadrupler With >30 dBc Harmonic Rejection," in IEEE Transactions on Microwave Theory and Techniques, vol. 68, no. 5, pp. 1697-1705, May 2020.

[16] X. Liao, D. Zhao and X. You, "An E-Band CMOS Frequency Quadrupler with 1.7-dBm Output Power and 45-dB Fundamental Suppression," 2021 IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA), Zhuhai, China, 2021, pp. 119-120.

[17] Z. Wang, K. Ma, Z. Ma, H. Fu and M. Lu, "A Frequency Quadrupler in 130-nm SiGe With Stack Multiport-Driven Matching Achieving 37.4% Instantaneous Bandwidth," in IEEE Microwave and Wireless Technology Letters, vol. 33, no. 1, pp. 66-69, Jan. 2023.

[18] K. Wu, S. Muralidharan and M. M. Hella, "A Wideband SiGe BiCMOS Frequency Doubler With 6.5-dBm Peak Output Power for Millimeter-Wave Signal Sources," in IEEE Transactions on Microwave Theory and Techniques, vol. 66, no. 1, pp. 187-200, Jan. 2018.

[19] P. Ricco, G. Avitabile and D. Manstretta, "A Compact 70–86 GHz Bandwidth Frequency Quadrupler with Transformer-Based Harmonic Reflectors in 28nm CMOS," 2023 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), San Diego, CA, USA, 2023, pp. 169-172.

[20] Y. Ye, B. Yu, A. Tang, B. Drouin and Q. J. Gu, "A High Efficiency E-Band CMOS Frequency Doubler With a Compensated Transformer-Based Balun for Matching Enhancement," in IEEE Microwave and Wireless Components Letters, vol. 26, no. 1, pp. 40-42, Jan. 2016.

[21] S. Li, T. Chi, T. -Y. Huang, M. -Y. Huang, D. Jung and H. Wang, "A Buffer-Less Wideband Frequency Doubler in 45-nm CMOS-SOI With Transistor Multiport Waveform Shaping Achieving 25% Drain Efficiency and 46–89 GHz Instantaneous Bandwidth," in IEEE Solid-State Circuits Letters, vol. 2, no. 4, pp. 25-28, April 2019.

[22] Y. A. Mensah, S. G. Rao, J. W. Teng and J. D. Cressler, "A High-Efficiency W-Band Frequency Quadrupler With Current-Reusing Stacked Push–Push Stages," in IEEE Microwave and Wireless Technology Letters, vol. 33, no. 4, pp. 447-450, April 2023.

[23] N. -Z. Sun, H. -Y. Li, J. -X. Xu, L. Gao and X. Y. Zhang, "A 52–65 GHz Frequency Quadrupler With Low Conversion Loss and High Harmonic Rejection Ratio in 28-nm CMOS," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 70, no. 8, pp. 2784-2788, Aug. 2023.

[24] A. Aghighi, M. Essawy and A. S. Natarajan, "A Frequency Doubler With Second Harmonic Feedback for Wideband, Efficient Frequency Multiplication at Millimeter-Wave," in IEEE Transactions on Microwave Theory and Techniques, vol. 72, no. 5, pp. 2704-2715, May 2024.

[25] M. Kucharski, M. H. Eissa, A. Malignaggi, D. Wang, H. J. Ng and D. Kissinger, "D-Band Frequency Quadruplers in BiCMOS Technology," in IEEE Journal of Solid-State Circuits, vol. 53, no. 9, pp. 2465-2478, Sept. 2018.

[26] M. K. Ali, G. Panic and D. Kissinger, "A Broadband 110 – 170 GHz Frequency Quadrupler with 29 dBc Harmonic Rejection in a 130-nm SiGe BiCMOS Technology," 2022 17th European Microwave Integrated Circuits Conference (EuMIC), Milan, Italy, 2022, pp. 44-47.

[27] J. Romstadt, J. Zaben, A. Papurcu, H. Stadler, P. Welling, T. Aufinger, K. Pohl, Nils, "A 117.5–155-GHz SiGe ×12 Frequency Multiplier Chain

With Push-Push Doublers and a Gilbert Cell-Based Tripler," in IEEE Journal of Solid-State Circuits, vol. 58, no. 9, pp. 2430-2440, Sept. 2023.
[28] C. Ozdag, A. Paidimarri, M. Yoshiyama, Y. Yamaguchi, Y. Tojo and B. Sadhu, "A 21–27-GHz Frequency Quadrupler in 0.13 μm SiGe BiCMOS with 0-dBm POUT and 40-dBc HRR for Wideband 5G Applications," 2024 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Washington, DC, USA, 2024, pp. 55-58.
[29] I. Apostolina and D. Manstretta, "A 14.5-17.9 GHz Harmonically-Coupled Quad-Core P-N Class-B DCO with -117.3 dBc/Hz Phase Noise at 1 MHz Offset in 28-nm CMOS," 2022 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Denver, CO, USA, 2022, pp. 211-214.
[30] A. Mazzanti and A. Bevilacqua, "Second-Order Equivalent Circuits for the Design of Doubly-Tuned Transformer Matching Networks," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 12, pp. 4157-4168, Dec. 2018.
[31] A. Franceschin, F. Quadrelli, F. Padovan, M. Bassi, A. Mazzanti and A. Bevilacqua, "A 20-GHz Class-C VCO With 80-GHz Fourth-Harmonic Output in 28-nm CMOS," in IEEE Microwave and Wireless Components Letters, vol. 31, no. 10, pp. 1154-1157, Oct. 2021.
[32] S. Vehring, Y. Ding, P. Scholz and F. Gerfers, "A 3.1-dBm E-Band Truly Balanced Frequency Quadrupler in 22-nm FDSOI CMOS," in IEEE Microwave and Wireless Components Letters, vol. 30, no. 12, pp. 1165-1168, Dec. 2020.
[33] H. P. Forstner, F. Starzer, G. Haider, C. Wagner and M. Jahn, "Frequency quadruplers for a 77GHz subharmonically pumped automotive radar transceiver in SiGe," 2009 European Microwave Integrated Circuits Conference (EuMIC), Rome, Italy, 2009, pp. 188-191.
[34] K. Lee, K. Kim, G. Shin and H. J. Song, "65.6–75.2-GHz Phase-Controlled Push–Push Frequency Quadrupler With 8.3% DC-to-RF Efficiency in 40-nm CMOS," in IEEE Microwave and Wireless Components Letters, vol. 31, no. 6, pp. 579-582, June 2021.

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