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Silicon Photonic Waveguides and Devices for Near- and Mid-IR Applications

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Abstract—Silicon photonics has been a very buoyant research field in the last several years mainly because of its potential for telecom and datacom applications. However, prospects of using silicon photonics for sensing in the mid-IR have also attracted interest lately. In this paper, we present our recent results on waveguide based devices for near- and mid-infrared applications. The silicon-on-insulator platform can be used for wavelengths up to 4 μm , therefore different solutions are needed for longer wavelengths. We show results on passive Si devices such as couplers, filters and multiplexers, particularly for extended wavelength regions, and finally present integration of photonics and electronics integrated circuits for high speed applications.

Index Terms — silicon, infrared sensors, optical waveguides, optical filters, optical resonators, photonic integrated circuits

I. INTRODUCTION

MORE THAN A DECADE AGO silicon photonics was seen as a useful platform for passive photonic devices but there was skepticism about its viability for integrated optoelectronic circuits and systems. This skepticism mainly stemmed from silicon's limitations for light emission and high speed optical modulation in the telecommunication band. During the last decade, there have been numerous breakthroughs in the field, and today silicon photonics is seen as the leading candidate to circumvent the interconnect bottleneck problem. There are many research groups in the world, both in industry and academia, and several silicon photonics companies that offer commercial products on the market. Silicon photonics is one of the most buoyant research fields at the moment with a huge potential for applications in telecommunications and data communications, but also in sensing.

Historically, much of the research was focused on telecommunication wavelength bands, however silicon and germanium are transparent up to 8 μm and 15 μm , respectively,

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thus offering a range of application in biochemical and environmental sensing, medicine, astronomy and communications [1]. The major problem with a transition to the mid-infrared (MIR, 2-20 μm) is that the most dominant platform, that of silicon-on-insulator (SOI), can be used only up to 4 μm due to the high absorption loss of silicon dioxide, and therefore alternative material platforms have to be utilized for longer wavelengths [1]. However, even in the near-infrared (NIR), where many groups use a 220 nm SOI platform, research teams have reported devices and integrated circuits based on different thickness' of both Si and buried oxide (BOX) layer. Xu *et al.* argue that there is a reason to revisit the choice of the SOI thickness because several Si photonic devices can perform better if thicker SOI is used rather than 220 nm SOI [2]. For example, ~300 nm overlayer thicknesses are preferable for supporting TM polarization and hence for sensing applications. Directionality of grating couplers is found to be optimized for silicon thickness of 350 nm, whilst for optical modulators the authors have found thickness of 360 nm to give a maximum figure of merit [2]. To fully exploit the transparency range of SOI, 400 or 500 nm thick overlayers need to be used. In addition, photonic SOI platforms usually have rather thick BOX to isolate the optical mode from the substrate, a structure that is not compatible with microelectronics. Therefore, C. Sun *et al.*, have developed a solution with integrated electronic circuits and suspended silicon waveguides in bulk silicon [3]. Zimmerman *et al.* reported integration of an optical modulator and driver in a BiCMOS process which combined both SOI, for optical devices, and bulk Si for electronics [4].

In this paper we present our recent results on waveguides, splitters, interferometers, and filters designed for the MIR. We investigate different material platforms, such as 400 and 500 nm SOI, and also suspended Si, and Ge-on-Si that offer extended transmission range in the MIR. Furthermore, for the more established NIR silicon photonics, we show grating couplers suitable for wafer scale testing, record low loss echelle grating multiplexers and a cost effective realization of photonic-electronic integrated circuits via wire bonding.

II. GROUP IV WAVEGUIDES AND DEVICES FOR THE MID-IR

A. SOI strip waveguides and passive devices

The most dominant platform in silicon photonics has been silicon-on-insulator (SOI). A buried oxide layer with typical

thickness of 1-2 μm is sandwiched between the top guiding Si layer and Si substrate. Different SOI thicknesses have been reported in literature and used by foundries. Established silicon photonics foundries such as IMEC and IME, have converged to using SOI wafers with 220 nm thick Si for their multi-project wafer (MPW) runs [5]. Passive components, modulators and Ge photodetectors are offered on this platform. The propagation losses as low as 0.6 dB/cm have been reported for 220 nm thick strip SOI waveguides at 1550 nm and ~ 2000 nm. For shallow rib waveguides with 70 nm etch depth, the loss can be only 0.1-0.2 dB/cm [6]. Commercially available optical transceiver cables from Luxtera/Molex are based on SOI with 300-310 nm thick Si, which was chosen to accommodate low loss compact passive devices and for a bulk-like transistor process [7, 8]. Silicon photonics developments at Oracle and STMicroelectronics are also based on this platform [9,10]. We have already reported losses of ~ 1.5 dB/cm for 400 nm rib SOI waveguides with 220 nm etch depth at a wavelength of 3800 nm [11].

Here, we report results for 500 nm strip SOI waveguides at the same wavelength. The waveguides were fabricated by electron beam (e-beam) lithography and inductively coupled plasma (ICP) etching. Waveguides with different lengths but the same number of bends had surface grating couplers at both the input and output. A propagation loss of 1.28 ± 0.65 dB/cm was measured for 1.3 μm wide waveguides using the cut back method. For 1.1 μm -wide strip waveguides the propagation loss was higher at 2.72 ± 0.57 dB/cm, due to larger optical mode-sidewall interaction. These results are lower than previously reported results for 400 nm SOI waveguides [11], which is expected as the mode is more confined in silicon.

Microfluidic channels can be integrated with waveguides for controlled interaction of a fluid analyte with a waveguide. Polydimethylsiloxane (PDMS) is a polymer that is widely used for the fabrication of microfluidic channels, and so may be placed directly on top of waveguides. To estimate the loss that PDMS would introduce at 3.8 μm , the propagation loss section on the chip was covered with PDMS. The losses were 5.44 and 3.89 dB/cm for 1.1 μm and 1.3 μm wide waveguides, respectively. In other words, additional loss of 2.72 and 2.61 dB/cm were introduced for 1.1 μm and 1.3 μm wide waveguides, respectively. That means, that a careful design of chips needs to be carried out to minimise the interaction of the optical mode with PDMS. In our future work, we will perform measurements at longer wavelengths to assess viability of PDMS for sensing in the MIR.

We have also developed multimode interference (MMI) splitters on this platform. The MMIs were 22.81 μm long and 8 μm wide, and were connected via tapers with 1.3 μm and 1.1 μm wide input and output waveguides. Insertion losses of 0.151 ± 0.024 and 0.225 ± 0.022 dB/MMI were measured for structures connected to 1.3 and 1.1 μm -wide waveguides (Fig. 1), respectively, similar to previously reported results based on 400 nm SOI [11].

Asymmetric Mach-Zehnder interferometers (MZIs) with a range of arm length differences were also fabricated. Fig. 2 shows responses for MZIs with $\Delta L = 350$ μm and $\Delta L = 50$ μm ,

respectively. The extinction ratio is approximately 30 dB, although clipping of the response can be seen due to mode-hopping in the QCL used for characterization. The free spectral range (FSR) was ~ 10 nm and ~ 75 nm in these two cases, respectively (Fig. 2).

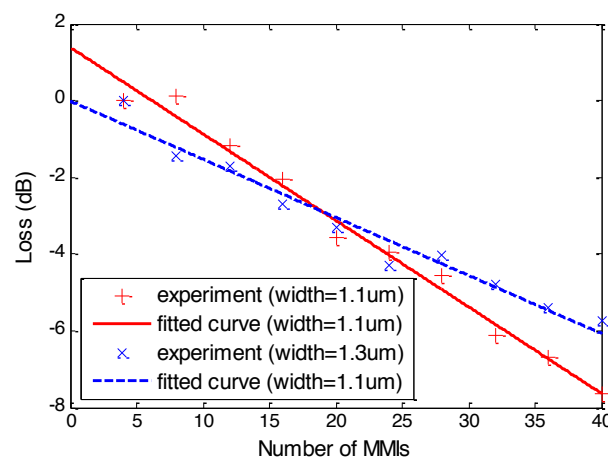


Fig. 1. Insertion loss measurement at the wavelength of 3.8 μm of MMIs fabricated on 500 nm SOI with 1.1 μm and 1.3 μm wide input/output waveguides.

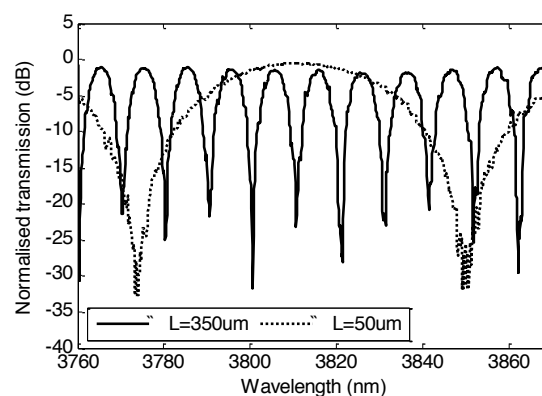


Fig. 2. MIR asymmetric Mach-Zehnder interferometers based on 500 nm SOI strip waveguides with arm length difference of 350 and 50 μm . By increasing the arm length difference, the free spectral range is reduced.

SOI ring and racetrack resonators are suitable photonic devices for sensing and optical signal processing (e.g., filtering, multiplexing) [12]. Cascade-coupled ring and racetrack resonators in a Vernier configuration have been used as an efficient solution for improving performance of photonic devices. Such architectures have been designed and fabricated as reconfigurable thermo-optical switches [13], tunable lasers [14, 15] and filters suitable for advanced multiplexing and demultiplexing in dense wavelength division multiplexing (DWDM) optical systems with FSR of 38 nm and interstitial peak suppression (IPS) of 25.5 dB [16, 17]. Furthermore, quadruple SOI Vernier racetrack resonators have been proposed for enhancing filter performance, exhibiting a FSR of 37.52 nm with a IPS of ~ 40 dB [18]. In addition, thermally tunable microring optical filters using p-i-p type microheaters have been proposed for enlarging the FSR up to ~ 95 nm [19] and grating assisted-couplers have been used to completely

eliminate the FSR in the drop and through port of the cascaded architecture [20].

The Vernier effect has been widely used for the design and fabrication of high performance sensors in the NIR [e.g. 21]. For example, experimental sensitivity of 24,300 nm/RIU and 2430 dB/RIU (RIU=refractive index unit) have been achieved for wavelength and intensity interrogation, respectively [22]. The Vernier effect has been also investigated by cascading a ring resonator with a MZI [23], and by exploring different technology platforms such as silicon nitride microring resonators, [24] and MZIs based on slot waveguides revealing a surface detection limit as low as 0.155 pg/mm² [25].

Here, we present MIR Vernier configurations based on racetrack resonators fabricated on the 500 nm SOI platform with a 2 μm BOX. A sophisticated algorithmic procedure based on the Finite Element Method (FEM) and Coupled Mode Theory (CMT) was implemented for the design of waveguides, directional couplers as well as single and cascade-coupled racetrack resonators. The strip waveguides were 1300 nm wide.

Two Vernier devices (V#1 and V#2), were fabricated in an architecture similar to that proposed in [26]. Table I lists the geometrical dimensions such as the racetrack lengths ($L_{\#1}$ and $L_{\#2}$), radii ($R_{\#1}$ and $R_{\#2}$), interaction lengths of the symmetric directional couplers ($L_{i,\#1}$ and $L_{i,\#2}$) and directional coupler gap, g_0 .

TABLE I

DIMENSIONS OF FABRICATED SOI VERNIER DEVICES

Device	$L_{\#1}$ (μm)	$L_{\#2}$ (μm)	$R_{\#1}$ (μm)	$R_{\#2}$ (μm)	$L_{i,\#1}$ (μm)	$L_{i,\#2}$ (μm)	g_0 (nm)
V#1	919.1	965.7	130	138	51.1	49.3	400
V#2	600.9	636.3	80	85	49.1	51.1	400

Subwavelength grating couplers were used to couple light from a QCL to the chip via MIR optical fibres. The FSR of racetrack resonators in V#1 were around 3.7 nm (i.e., $FSR_{\#1} = 3.79$ nm, $FSR_{\#2} = 3.60$ nm, $\Delta FSR = 190$ pm), insertion loss ~ 1.2 dB, extinction ratio > 22 dB and Q factors 3,000-4,400. Fig. 3(a) shows the overall Vernier spectrum of the configuration labeled as V#1 plotted on dB scale. Two entire Vernier patterns made of close resonance peaks separated by a spectral distance $\Delta\lambda_{\text{Vernier}} \approx 4$ nm, were achieved in the 3.72 μm to 3.88 μm spectral window. An overall FSR_{Vernier} equal to 71.81 nm was measured.

In Fig. 3(b), the overall Vernier spectrum of the V#2 configuration is plotted on dB scale. As listed in Table I, Ring#1 and Ring#2 of this configuration were characterized by shorter lengths, i.e. 600.9 μm and 636.3 μm , respectively. Consequently, the FSRs of both resonators were larger than FSRs of single microcavities of the configuration V#1. In fact, $FSR_{\#1}$ was equal to 5.8 nm and $FSR_{\#2}$ to 5.48 nm, giving $\Delta FSR = 320$ pm. By using shorter racetrack resonator lengths, parameters $\Delta\lambda_{\text{Vernier}}$ and FSR_{Vernier} became larger, being equal to ~ 6 nm and 99.32 nm, respectively. This effect can be easily appreciated by comparing Vernier spectra in Figs. 3(a) and 3(b), plotted in the same spectral window.

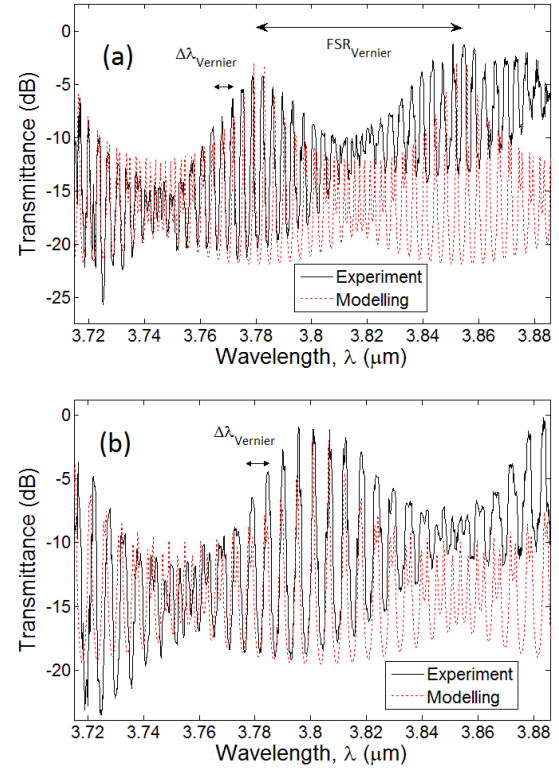


Fig. 3. Normalized experimental and simulated transmittances of the Vernier architectures (a) V#1 and (b) V#2.

It is worth highlighting that in both spectra plotted in Fig. 3, good agreement between the experimental and simulated spectra was achieved. Moreover, the shape of the resonances constituting the Vernier peaks was not constant throughout the overall experimental wavelength range. This effect was mainly due to wavelength dependence of input/output gratings and chromatic dispersion affecting the operation of directional couplers as well as of cascade-coupled racetrack resonators. In conclusion, average insertion loss IL_{avg} , maximum extinction ratio ER_{max} and the Vernier gain G of the Vernier configurations V#1 and V#2, are listed in Table II.

TABLE II

EXPERIMENTAL OPTICAL PARAMETERS OF FABRICATED SOI VERNIER

Device	FSR_{Vernier} (nm)	IL_{avg} (dB)	ER_{max} (dB)	G
V#1	71.81	3.85	16.97	19.94
V#2	99.32	2.39	18.19	18.12

Using these configurations we have also demonstrated a Vernier sensor [27].

B. Slot waveguides

Slot waveguides (Fig. 4) can enhance the electric field amplitude in the gap region (up to 50 times higher [28]) compared to standard waveguide structures and thus can provide increased sensitivity in future MIR silicon photonics sensors. Recent results for this waveguide type in the NIR include SOI slot waveguides with loss of 2.28 ± 0.03 dB/cm at 1064nm [29] and 2dB/cm at 1550nm [30]. In the MIR, a

propagation loss of 11dB/cm at 3.4 μ m was reported for silicon-on-sapphire (SOS) slot waveguides [31]. In this subsection we report a significant improvement compared to our work described in [11] where the reported loss at 3.8 μ m was 9 dB/cm.

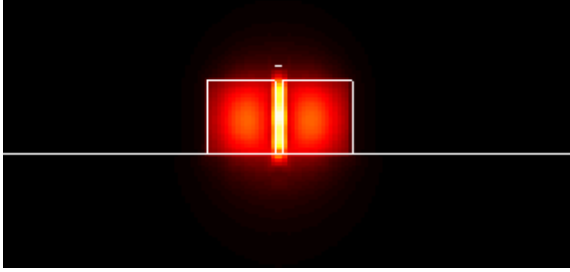


Fig. 4. Mode profile of a SOI slot waveguide. A significant part of the mode is in the air gap.

The simulation of the structure was performed using Photon Design Fimmprop FMM solver. The devices were fabricated using e-beam lithography and ICP etching on 150 mm SOI wafers with a 2 μ m BOX and 400 nm silicon overlayer. The slot waveguides were 1.47 μ m wide with a 70 nm slot width. Light from a QCL is coupled to rib waveguides via surface grating couplers and then from rib to slot waveguides via a taper termination proposed in [30]. The width of the rib waveguides was 1.35 μ m and etch depth 220 nm. The slot waveguides were not fully, but partially etched to the same etch depth as the rib waveguides.

The propagation loss of the slot waveguides measured was 2.6 ± 0.24 dB/cm whilst the rib-slot transition loss was 0.03 dB/interface. Bends with 60 μ m radius had loss of 0.082 dB/90° bend. Further reduction of the loss could be achieved by sidewall smoothing using thermal oxidation, although this may also change the geometry of the interface and thus impact transmission.

C. Suspended waveguides

It has been shown that the loss of SOI waveguides increases for wavelengths longer than 3.7-3.8 μ m [32]. In order to use the full transparency region of Si, the SiO₂ cladding needs to be replaced by a cladding with suitable transparency region, or the buried oxide layer should be removed leaving suspended Si waveguides.

The latter approach was implemented by Cheng *et al.* [33]. They demonstrated rib waveguides with etched holes in the slab region that served for HF removal of the buried oxide cladding. These holes were placed approximately 3 μ m from the rib waveguide so as not to disturb the mode propagation. The minimum propagation loss measured at a wavelength of 2.75 μ m was around 3 dB/cm. The fabrication involved two etch steps, one for the formation of the rib waveguide and one for the holes in Si slab used for under-etching the BOX.

We have developed a novel design that requires one etch step for the formation of lateral holes (Fig. 5). These subwavelength holes have a twofold purpose: to create a lateral cladding and for removal of the buried oxide layer by HF etching. The design is also more robust than the one

reported in [33] since the thickness of the Si overlayer is constant on the chip. The waveguides were 1.1 μ m wide, the holes were 3-5 μ m wide and we varied their duty cycles (hole/silicon width ratios). For a 150 nm/150 nm ratio, liquid HF could not be used as the holes were too small. We used vapour phase HF instead, but the oxide etch was too slow. To solve this problem, we increased the subwavelength grating period to 550 nm, and increased the air/Si ratio to 450/100 nm. Liquid HF could then be used and we demonstrated propagation of MIR light through these suspended structures, with a minimum loss of 3.6 dB/cm at a wavelength of 3.8 μ m [34]. Light was coupled from MIR optical fibres via fully etched and suspended subwavelength grating couplers. Future work will include development of other passive structures in this platform.

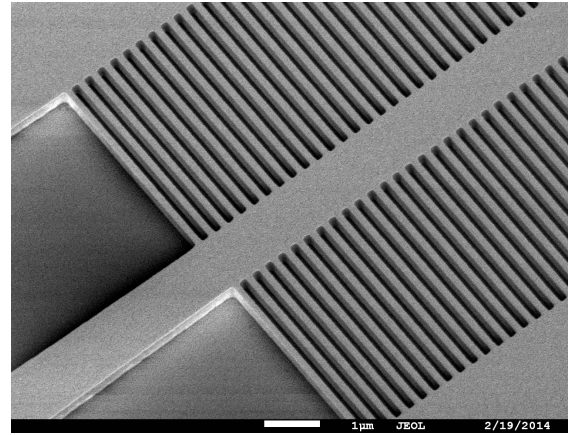


Fig. 5. SEM of a suspended Si waveguides with subwavelength lateral gratings which act both as lateral claddings and access points for buried oxide removal.

D. Ge on Si waveguides

To increase transparency of a group IV photonic platform further into the MIR, Ge can be used. Its transparency extends to 15 μ m [1]. Two micrometer thick strip Ge-on-Si waveguides with losses of ~ 3 dB/cm were first reported in [35]. Similar losses for the same structure, at a similar wavelength range, were also reported by Malik *et al.* [36]. These waveguides have also been characterised at a wavelength range of 2-2.6 μ m [37]. The waveguides were fabricated by CVD growth and reactive ion etching (RIE) using a metal mask.

We have designed Ge-on-Si rib waveguide platform for a wavelength of 3.8 μ m (Fig. 6). The starting Ge-on-Si wafers were fabricated by epitaxially depositing a 2 μ m thick Ge layer onto a Si substrate using chemical vapour deposition (CVD). To fabricate the rib waveguides a SiO₂ hard mask was defined, which was deposited via plasma enhanced CVD (PECVD), then patterned via contact lithography and RIE using an Ar/CHF₃ plasma. The photoresist was subsequently stripped and a further RIE step performed (SF₆/CHF₃ plasma) to form the waveguides. Finally, the SiO₂ mask was removed using a HF bath and the samples were cleaned and cleaved. The waveguides used in this work were designed to have an etch depth of 1.2 μ m and a core width of 2.25 μ m. To facilitate

coupling, input and output tapers were fabricated at each end with a maximum width of 10 μm . Waveguides of different lengths were incorporated on the chip by introducing four identical bends with radius of 100 μm .

The propagation loss of these waveguides was measured by the cut back method giving a loss of 2.4 ± 0.2 dB/cm at a wavelength of 3.8 μm . We believe that this is the lowest reported loss for Ge on Si waveguides. Our future work will include the development of other passive and active devices on this platform, including grating couplers, splitters, interferometers, modulators and detectors.

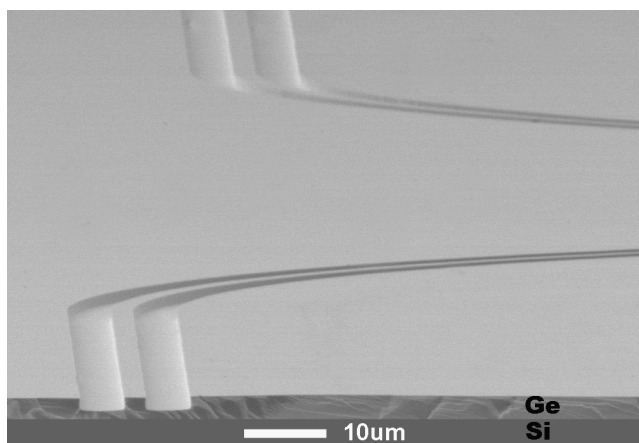


Fig. 6. Ge-on-Si rib waveguide fabricated in the Southampton Nanofabrication Centre.

III. ERASABLE GRATING COUPLERS

Coupling of light into a sub-micron waveguide to be used alongside electronics is a non-trivial task. Planar waveguides are around two orders of magnitude smaller than a standard fibre based waveguide leading to a large mode mismatch. The most popular approach is a surface grating coupler, first demonstrated by Dakss *et al.* [38]. Grating couplers do not require time consuming preparation such as polishing or antireflective coatings and can be measured before dicing the wafer, potentially allowing time and cost savings. They are formed by a periodic change in the effective index of the waveguide, typically by utilising an etch process [39, 40]. Light is then coupled in or out through the surface at an angle.

Gratings couplers have moved on significantly since their inception by Dakss *et al.* [38]. Key optimisations can be made to increase the outcoupling efficiency of a grating coupler such as the addition of an overlayer to the grating region, which improves efficiency by increasing the directionality of the output field as shown by Roelkens *et al.* [41]. Although only 55% efficiency was demonstrated empirically it was suggested that 80% efficiency should be attainable in such structures. Coupling efficiency can also be increased by adding a substrate reflector or by improving the mode overlap between the Gaussian optical fibre mode and the outcoupled grating mode. This can be achieved using apodization. Taillaert *et al.* provided an insightful publication on these enhancements [39]. A numerical optimisation was used to achieve a Gaussian output field profile from the grating

coupler and a Bragg reflector was added to the substrate. The simulated results showed that for a 13 μm device length, an efficiency of 61% was achievable in SOI without the substrate Bragg reflector and up to 92% with the Bragg reflector. The etch profile was still rectangular and without the Bragg mirror the complexity of the fabrication process was no different to typical uniform gratings, though the critical feature size would be smaller in the apodized design. Chen *et al.* provided some more recent apodized devices [42] claiming a coupling loss of only -1.2 dB per coupler in the best devices corresponding to an efficiency of 75.9% with a substrate reflector, with devices without the reflector achieving a coupling performance better than -2 dB (63.1%). They also noted that apodization reduces back reflection into the waveguide, which is highly desirable to reduce noise experienced by other integrated devices. Further work into this style of device has demonstrated the best grating coupling performance available in SOI to date, Zaoui *et al.* [43] demonstrated coupling loss results of only 0.62 dB (87% efficiency) per coupler empirically using an apodized design along with an aluminium bottom reflector.

Grating couplers also offer the ability to couple light into or out from a waveguide at intermediate points along the optical circuit, allowing for autonomous testing at a component level. However, grating couplers in the SOI platform are traditionally fabricated using a surface relief approach which is not easily removable. Grating couplers formed using ion implantation however, can be removed after measurement using laser annealing [44]. The ion implantation process introduces disorder into the silicon lattice, typically in the form of vacancy and self-interstitial defects, which results in an increase in the refractive index of the material. The magnitude of the refractive index increase is dependent on the level of disorder introduced to the lattice but can be an increase of almost 0.6. Energy provided via a thermal processes such as oven based or laser annealing allows order to be restored to the lattice, and hence removing the associated refractive index change. Here, we describe the fabrication of gratings utilising the implantation technique and give experimental evidence of their performance.

The waveguide sections comprised a 220 nm thick Si wire waveguide with a 400 nm width to ensure single mode operation; the buried oxide layer had a thickness of 2 μm . The waveguide width was increased to 10 μm for the grating test point via a dual step taper to maximise the overlap integral between the fibre mode and grating mode.

The first stage of the process was to fabricate waveguides on the Si layer. Subsequently an e-beam resist (ZEP 520A) was spun onto the wafer at 2000 rpm in order to achieve a 500 nm resist thickness. E-beam lithography was used to pattern the grating into the resist, which was then developed, before the entire structure was implanted with germanium ions using a dose of 1×10^{15} ions cm^{-2} to ensure amorphization [44]. The implantation energy is varied depending on the required depth of amorphization, in this case an energy of 100KeV was used. Following implantation the resist was removed using a three stage solvent clean of acetone, isopropanol and deionised water for 2 minutes per bath in the listed order, followed by a

10 minute O₂ plasma ashing process.

Following successful fabrication, the amorphous grating can be tested an unlimited number of times during other manufacturing stages of the optical circuit. However, exposure to high temperatures (above 500°C) may reduce coupling efficiency [45]. After testing has been completed, the grating can be erased from the optical circuit via an annealing process. Annealing can either be carried out in an oven at a minimum temperature of 500°C or by a laser. Using oven annealing is not desirable as the heat applied may cause damage to other fabricated devices and therefore to the whole circuit. Laser annealing offers an advantageous localised annealing method which does not affect other fabricated devices.

It may be logical to assume that there is a drastic difference between implanted and surface relief grating couplers due to the significant difference in both the refractive index contrast, and the differing profiles between the two fabrication methods, but this is not the case. Five variations of the implanted grating were tested in total with grating periods of 580 nm, 590 nm, 600 nm, 610 nm, and 620 nm. All structures consisted of uniform gratings with a ZEP e-beam resist implant mask, with a duty cycle of 50%. Germanium at an energy of 100 keV with a dose of 1×10^{15} ions cm⁻² was implanted into Si. Surface relief grating couplers were also fabricated alongside the implanted couplers for use as a comparison to the implanted couplers. The period used for the surface relief gratings was 700 nm and the etch depth used was 70 nm. Simulation data suggested that the outcoupling efficiencies of the implanted gratings and surface relief gratings used in this work were 45% and 52%, respectively.

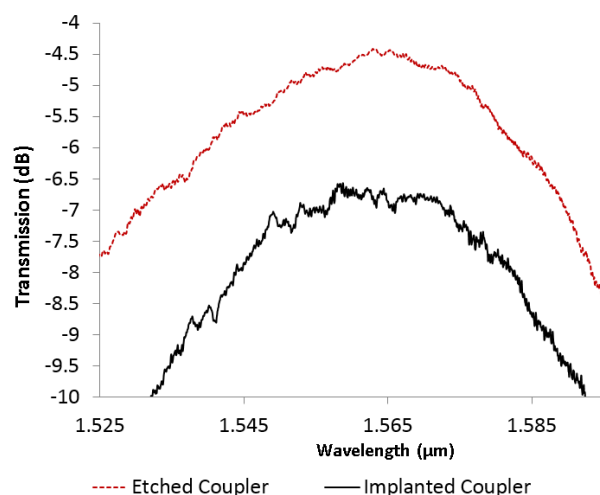


Fig. 7. Comparison between the etched and implanted surface grating couplers.

Before characterisation, the optical characteristics of the measurement setup were accounted for by normalising all of the results to a transmission measurement of the setup, using an optical fibre to bypass the grating couplers and optical device under test. The best implanted grating coupler demonstrates a loss of only 5.5 dB (28% coupling efficiency) compared with a loss of 4.5 dB (35% coupling efficiency) shown for a comparable surface relief grating coupler, a

difference of only 7%. Although the efficiency demonstrated is likely to be sufficient for wafer scale testing, it is expected that performance obtained from the uniform implanted grating couplers could be improved significantly using either apodization or by the addition of a bottom reflector if necessary. The measured efficiency value is lower than the simulated value in both implanted and surface relief grating coupler cases, this is dominantly due to the difference in the modal overlap between the fibre mode and the mode exiting the grating coupler, though the difference between the measured results is in agreement with the difference expected from simulations. This suggests that the implanted grating coupler does not possess any unexpected loss mechanisms compared with the surface relief fabrication method.

To enable a more detailed comparison between the implanted and the surface relief grating coupler's characteristics we consider transmission data of both fabrication methods with the same central wavelength, as shown in Fig 7. At this central wavelength, the coupling loss of the implanted device increases to 6.6dB. Interestingly at the peak of the output performance (within 0.25dB of the maximum) the implanted coupler displays a wider bandwidth than the surface relief grating coupler, with peak performance bandwidths of 16 nm and 8 nm, respectively. Typically the performance metric used for grating couplers is the bandwidth at 1 dB below peak performance. The 1 dB bandwidth of the implanted and surface relief couplers are almost identical at 32 nm and 30 nm, respectively. A 1 dB bandwidth of 30 nm is comparable to uniform surface relief gratings published in the literature. This technology can in principle be translated into the MIR, however an investigation of the refractive index of ion implanted amorphous silicon would need to be measured at longer wavelengths.

IV. PLANAR CONCAVE GRATINGS

Wavelength division (de)multiplexers on SOI platform are important devices for integrated photonic circuits and can be realized by various structures, such as arrayed waveguide gratings (AWGs) [46, 47], cascaded Mach-Zehnder interferometers (cMZIs) [46, 48], angled multimode interferometers (AMMIs) [49, 50], cascade ring resonators (cRRs) [46, 51], and planar concave gratings (PCGs) [46, 52] etc. Recent progress in silicon photonics has demonstrated AWGs, cMZIs and cRRs with low insertion loss, low cross talk, and flat-top spectral response. However, these WDM structures have phase shifters formed by sub-micron single mode waveguides, which require precise control of the waveguide width during fabrication. AMMIs have also been demonstrated as WDM structures in various configurations. They are less sensitive to fabrication errors in waveguide width, whilst their channel count is limited to a small number (≤ 4) [49] unless extra single mode waveguide based structures (e.g. MZI) are used for interleaving [50]. PCGs can have more channels than MMIs and use micron-scale echelle gratings instead of submicron waveguides as dispersive structures. They have an advantage that waveguide width control is not required. The main challenge to achieve high-performance

PCGs for low-insertion-loss and low-cross-talk operation is to minimise phase errors at both grating facets and slab areas. Here, we demonstrate a 4-channel PCG with a thin slab waveguide on the SOI platform for the integration with a silicon modulator. An insertion loss of <1dB and a cross-talk of <-20dB have been achieved.

The PCG was designed in a Roland circle configuration and had a footprint of 380 μm by 180 μm excluding input/output waveguides. The PCG had 41 grating facets and each facet was a 4-period Bragg reflector with a period of 340 nm and a duty cycle of 50%, (Fig. 8) which gave >95% reflectivity over a wavelength band of 100 nm centred at 1550 nm. The silicon modulator to be integrated with the PCG had a 400 nm-wide rib shaped waveguide structure with a silicon overlay thickness of 400 nm and a slab thickness of 180 nm. Hence, we designed a PCG with a 180 nm-thick free propagation region (FPR), 400 nm by 180 nm stripe shaped input/output waveguides, and a waveguide transition structure to bridge the modulator's rib waveguides and the PCG's stripe waveguide with low-loss power transfers (Fig. 9).

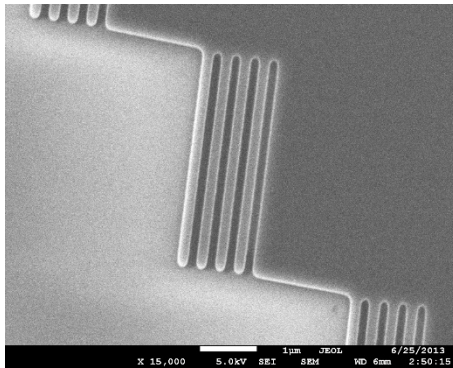


Fig. 8. SEM image of the fabricated Bragg reflectors at the PCG mirrors.

At the interfaces between the waveguide transitions and PCG's input/output waveguides, the rib waveguide had a width of 100 nm, which was small enough and almost no mode power was contained in the 100 nm by 220 nm rib area. It was designed to smoothly "squeeze" the mode power from the rib area into the 400 nm by 180 nm slab area.

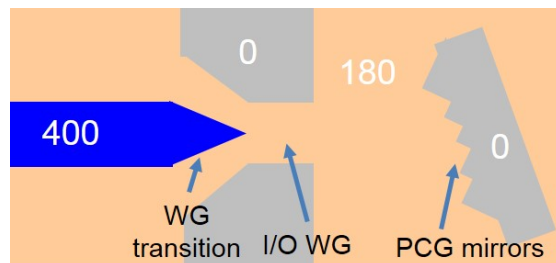


Fig. 9. The schematic drawing of the fabrication process: step 1 - definition of the waveguide for the modulator; step 2 - definition of waveguide transition structure, input/output waveguides and Bragg mirrors of the PCG.

After the waveguide transition, the 400 nm wide input/output stripe waveguides were tapered up to a width of 2 μm before entering the FPR in order to suppress mode mismatch at the interfaces. In our design, the FPR had a

thickness of only 180 nm, which was thin enough to guarantee single slab mode in the FPR and to make the Bragg mirror's reflectivity even more tolerant to the variation of vertical dimensions than that reported in [52].

Surface grating couplers with a period of 570 nm and a duty cycle of 50% were used in the design to couple light from/to the single mode 400 nm/180 nm rib waveguides. The surface grating couplers had a width of 10 μm and were connected to the single mode rib waveguides by adiabatic tapers.

The fabrication process is shown in the schematic drawing of Fig. 9. Two lithography/etching steps were used. In the first step, the 400nm/180 nm rib waveguide was patterned. In the second step, the waveguide transition structure and the PCG mirrors with DBR reflectors were patterned. In both steps, the structures were patterned by deep UV lithography and ICP etching.

The measured transmission spectra of a fabricated PCG is shown in Fig. 10. The cross-talk across the 4 channels is approximately -20dB and the insertion loss for the 4 channels are 1.0dB, 0.7dB, 1.7dB and 1.7dB respectively. To the best of our knowledge, this is the lowest insertion loss achieved in PCGs on the SOI platform.

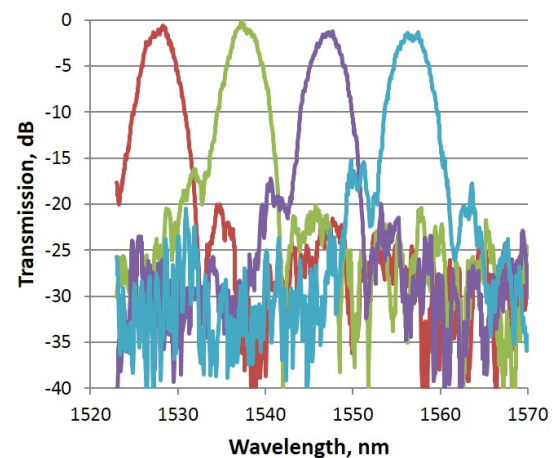


Fig. 10. Normalised transmission spectrum measured from a fabricated PCG.

V. INTEGRATION

Finally, after reporting various silicon photonics devices operating in the NIR and MIR, we show our results on integration of photonic and electronic circuits. In recent years, researchers have demonstrated silicon photonic transceiver links based on a vertical cavity surface emitting laser (VCSEL) [53], ring resonator modulator [54] and a Mach-Zehnder modulator (MZM) [55, 56]. Although the MZM approach has lower power efficiency compared to the other two approaches [57], the relatively large bandwidth and improved tolerance to process and temperature variations make it attractive for low cost silicon photonic transceivers.

While it has been demonstrated that voltage mode transmitters generally have better power efficiency compared to current mode drivers [58], previous MZM drivers [56, 59, 60] are based on the current mode logic (CML) approach. The only voltage mode driver that is integrated with MZM was used with a forward biased p-i-n diode and formed a 2Gb/s

silicon photonic switch [61]. Here, we present a transmitter PCB, which consists of a carrier depletion based Si MZM and a voltage mode 10 Gb/s driver in a standard 130 nm CMOS process. To the best of our knowledge, this is the first voltage mode driver that is designed to be integrated with the reverse biased PN MZM. In addition, a separate receiver PCB consisting of a Ge-on-Si photodetector (PD) and a 130 nm CMOS transimpedance amplifier (TIA) has also been implemented. The full link operation is also demonstrated up to 10 Gb/s.

The proposed design was fabricated using the IBM 8RF 130 nm CMOS process in bulk Si. The layout was designed for 4 parallel channels. The main circuit blocks were evenly distributed along the length of the chip, so as to fit the requirements of I/O pads with a 150 μm pitch. A photograph showing the wire bonds between the driver chip, MZM chip and the PCB is shown in Fig. 11. The input differential electrical signal was connected onto the FR4 printed circuit board via two SMA connectors and microstrip lines routed to the input side of the CMOS driver chip. Wire bonds were then used to connect onto the CMOS driver chip. On the output side of the driver chip wire bonds were again used to connect the amplified differential electrical data to the input of the MZM modulator. DC power was also applied to the printed-circuit board (PCB) where it was regulated before being passed to the driver chip again via wire bonds. Input and output light was coupled to and from the modulator using surface grating couplers.

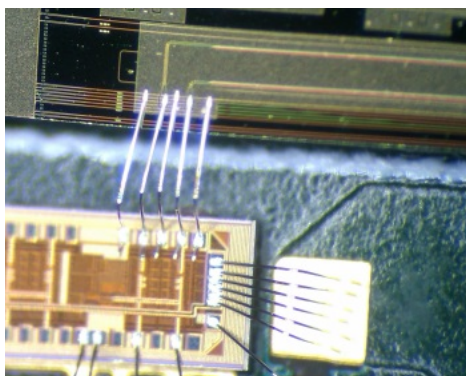


Fig. 11. Image of wire bonds between the CMOS driver amplifier and the Mach-Zehnder modulator

The optical modulator was fabricated in 220 nm SOI and has been described previously [62]. The waveguide dimensions were 400 nm width, 220 nm height and 100 nm slab height. The device was based upon free carrier depletion of a pn junction which is self-aligned with one edge of the rib waveguide. The phase modulator was formed in both arms of a Mach-Zehnder interferometer to balance the losses and to allow for push-pull operation. Coplanar waveguide electrodes were used to propagate the high speed data signal along the phase modulators. At the inputs of the CPW electrodes the signal lines were widened to allow wire bonding.

The receiver side was developed using a similar approach. Fig. 12 shows the wire bonds between the TIA chip and the PD chip and PCB. The input optical signal was launched onto the PD chip via a surface grating and propagated to a Ge based PD via a Si wire waveguide. The PD itself was based on a

standard epixfab design. Wire bonds were then used to connect between the PD chip and the CMOS TIA chip. On the output side of the TIA wire bonds were used to connect the differential electrical data signal to the PCB where it propagated along microstrip lines to two output SMA connectors. DC power was again applied to the PCB where it was regulated and then connected to the TIA via further wire bonds.

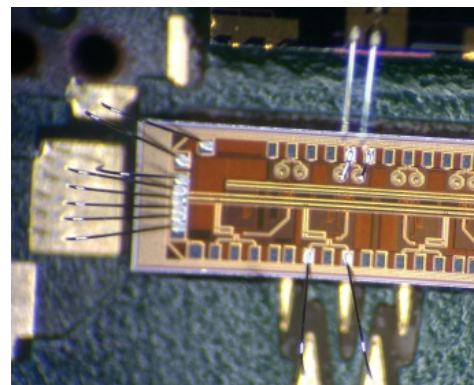


Fig. 12. Image of wire bonds between the CMOS transimpedance amplifier and the photodetector.

The CMOS inverter TIA structure was adopted, with the advantages of higher gain and relative lower noise [63]. Some modifications made were that NMOS and PMOS transistors were seen with different feedback resistors, due to the transconductance of these devices being inherently different. The total receiver circuit consisted of a TIA, a 10 stage limiting amplifier (LA), a single to differential converter and an output buffer. They were fabricated using the same IBM 8RF 130 nm process as the driver, with a 4 parallel channel configuration. The power consumption of each channel was ~ 97.4 mW.

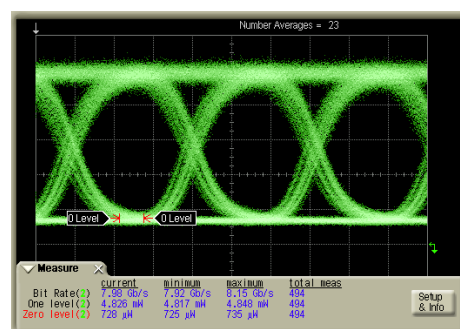


Fig. 13. Eye diagram for integrated optical driver at 8Gb/s

In order to test the optical performance of the driver board, the light from a tunable laser was passed via optical fibre to the input coupler on the MZM chip. High speed data signals of up to 10 Gb/s were passed via COAX cable from the generator to the transmitter board. Electrical phase shifters were used to counter electrical timing mismatches introduced by the COAX cables. Light was coupled from the output of the MZM to another optical fibre which was passed to an erbium doped fibre amplifier (EDFA). The light was then passed to the DCA via a tunable band pass optical filter. Open optical eye diagrams up to 10Gb/s were observed. An eye diagram at 8 Gb/s can be seen in Fig. 13 showing an extinction ratio of 11

dB. A power consumption of 465mW per channel was measured. This compares favourably with previously reported integrated transmitters based upon Si MZM where the power consumption has been stated. In [64] front end integration of a silicon MZM and driver in BiCMOS was reported with operation at 10Gbit/s and a power consumption of 830mW. In [56] a power consumption of 575mW was reported from a 10Gbit/s transmitter based upon the front end integration of a Si MZM in CMOS. In [65] a wire bond integrated driver and QPSK modulator operating at 28Gbaud with a power consumption of 500mW was reported. In this case a SISCAP modulator was used rather than a carrier depletion based device and as a result a lower drive voltage is required. Transmitters with lower power consumption are possible when driver amplifiers are integrated with ring resonator based modulators, however the optical bandwidth of the device is much reduced. In addition to this tuning is required to correctly position the resonance which shifts significantly due to high fabrication and temperature sensitivities. This adds complexity and would also contribute to the power consumption of the transmitter.

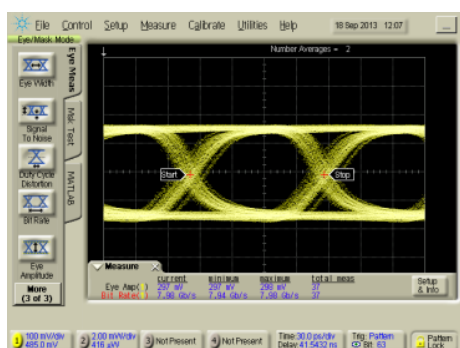


Fig. 14. Results of testing TIA at 8 Gb/s

The receiver board was tested by applying an optical data signal directly to the photodetector chip. The optical data signal was generated by passing CW laser light through a commercial LiNbO₃ modulator driven by a pseudorandom binary sequence (PRBS) generator and commercial driver amplifier. The light was then passed via an optical fibre to the photodetector chip. The electrical output data was passed via COAX cable to the electrical input of the DCA. Open electrical eye diagrams were obtained at 8 Gb/s and 10 Gb/s. Fig. 14 shows an 8 Gb/s open eye diagram. The amplitude of the output electrical signal was approximately 290 mV. The supply voltage to the TIA was 1.5 V, drawn current 64.2 mA and therefore power consumption 96.3 mW.

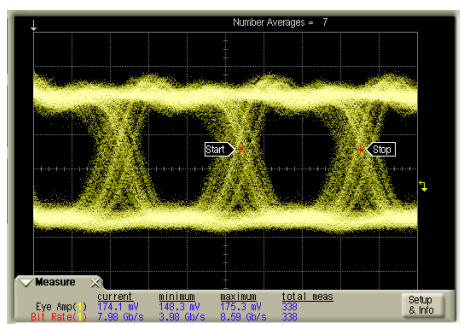


Fig. 15. Eye diagram for full link operating at 8 Gb/s

Finally the full link was tested by connecting the amplified optical output of the transmitted board to the optical input of the receiver board. The electrical data from the receiver board was passed to the DCA again via COAX cables. The resulting electrical eye diagram at 8Gb/s is shown in Fig. 15.

VI. CONCLUSION

We have briefly reviewed our recent results on waveguides for both near- and mid-IR wavelength bands. We have shown that low loss mid-IR waveguides, splitters and interferometers can be realised in SOI, suspended Si, and Ge-on-Si material platforms. Ge-on-Si has the largest transparency range of the three and with other advantages of Ge compared to Si, it has a lot of promise for high speed communications and sensing applications in the mid-IR. We have also presented erasable gratings in Si that can find application in wafer scale testing, record low loss echelle gratings with a minimum insertion loss of 0.7 dB, and cost-effective integration of photonic and electronic chips using wire bonding. The modulator/detector chips were optimised and fabricated separately from the driver/TIA chips and the two were wire bonded. The maximum speed of an optical link comprising an integrated transmitter and an integrated receiver was 10 Gb/s.

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